# Electronic Devices

## Final Term
## Lecture - 06

Reference book:

**Electronic Devices and Circuit Theory (Chapter-7)**

Robert L. Boylestad and L. Nashelsky , (11th Edition)

# OBJECTIVES

- Be able to perform a dc analysis of JFET, MOSFET, and MESFET networks.
- Become proficient in the use of load-line analysis to examine FET networks.
- Develop confidence in the dc analysis of networks with both FETs and BJTs.
- Understand how to use the Universal JFET Bias Curve to analyze the various FET configurations.

# GENERAL RELATIONSHIPS

- For all FETs: $I_G \approx 0A$ $I_D = I_S$
- For JFETs and Depletion-Type MOSFETs: $I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$
- For Enhancement-Type MOSFETs: $I_D = k(V_{GS} - V_T)^2$
- BJT: Linear Relationship between $I_B$ and $I_C$
- FET: Non-linear Relationship between $V_{GS}$ and $I_D$.

# COMMON FET BIASING CIRCUITS

- JFET
  - Fixed – Bias
  - Self-Bias
  - Voltage-Divider Bias
- Depletion-Type MOSFET
  - Self-Bias
  - Voltage-Divider Bias
- Enhancement-Type MOSFET
  - Feedback Configuration
  - Voltage-Divider Bias

# FIXED-BIAS JFET

- The simplest biasing arrangements:

$$I_G \approx 0A \qquad I_D = I_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- For the DC analysis,
  - Capacitors are open circuits

$$I_G \cong 0A \qquad V_{RG} = I_G R_G = (0A)R_G = 0V$$

- The ***zero-volt drop across $R_G$*** permits ***replacing $R_G$ by a short-circuit.***

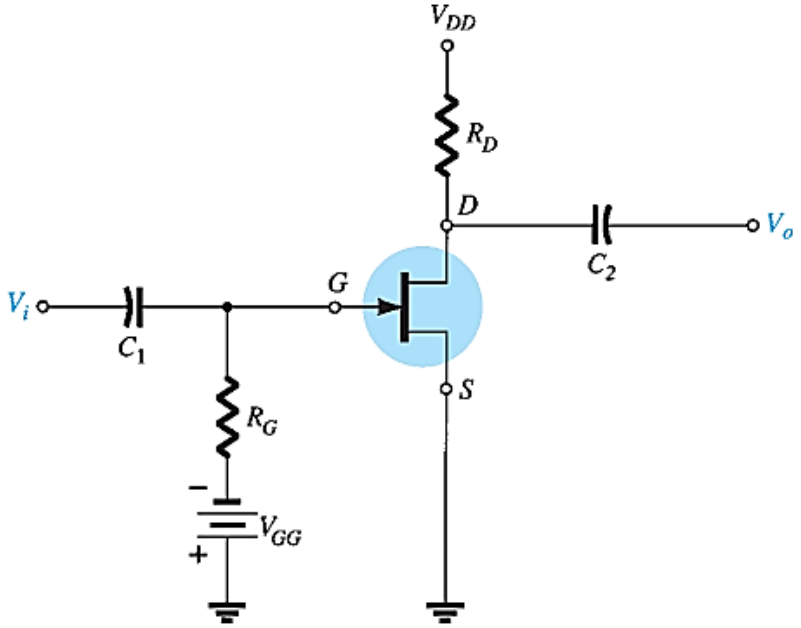


**FIG. 7.1**
*Fixed-bias configuration.*

# FIXED-BIAS JFET

- Can be solved using either Mathematical Approach or Graphical Approach:

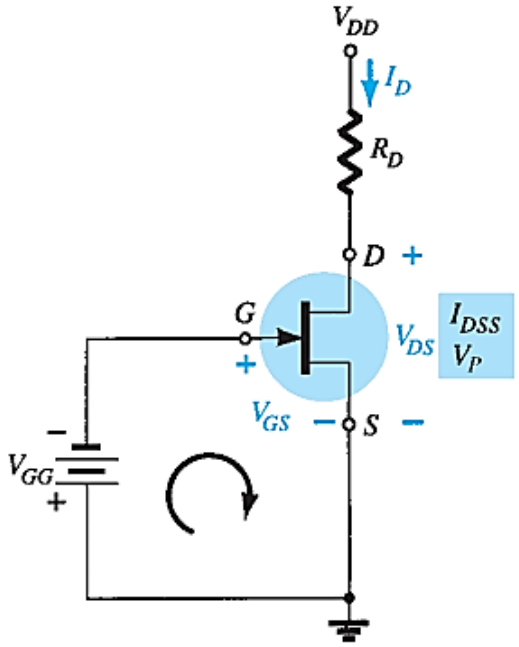


**FIG. 7.2**
*Network for dc analysis.*

## Mathematical Approach

$$V_{GS} = -V_{GG}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0$$

$$V_D = V_{DS}$$

$$V_G = V_{GS}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

## Graphical Approach

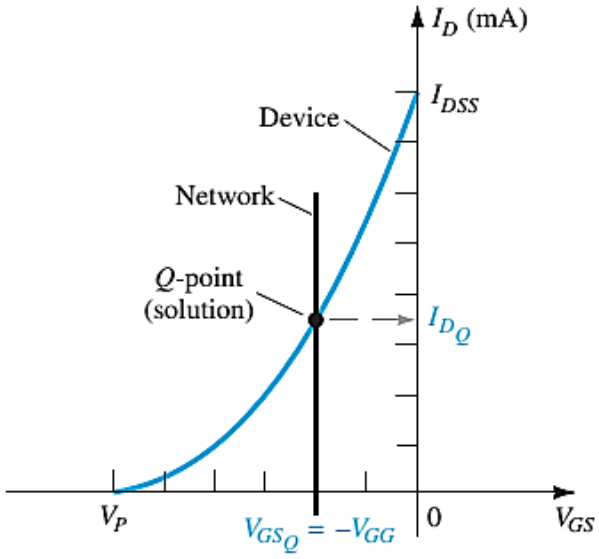


**FIG. 7.4**
*Finding the solution for the fixed-bias configuration.*

# FIXED-BIAS JFET EXAMPLE

- Determine $V_{GSQ}$, $I_{DQ}$, $V_{DS}$, $V_D$, $V_G$, $V_S$.

## Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\ \text{mA}\left(1 - \frac{-2\ \text{V}}{-8\ \text{V}}\right)^2$$
$$= 10\ \text{mA}(1 - 0.25)^2 = 10\ \text{mA}(0.75)^2 = 10\ \text{mA}(0.5625)$$
$$= \mathbf{5.625\ mA}$$

c. $$V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.625\ \text{mA})(2\ \text{k}\Omega)$$
$$= 16\ \text{V} - 11.25\ \text{V} = \mathbf{4.75\ V}$$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

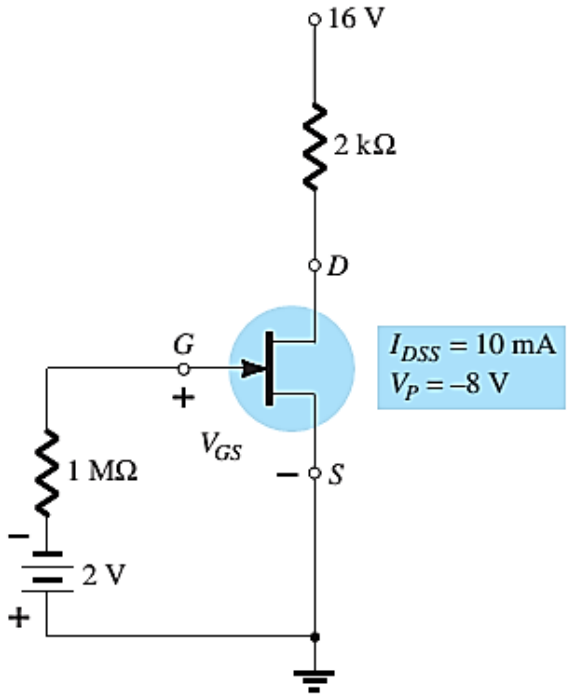


**FIG. 7.6**
*Example 7.1.*

# FIXED-BIAS JFET EXAMPLE

## Graphical Approach

$$V_{GS_Q} = -V_{GG} = -2\,\text{V}$$

$I_{D_Q} = 5.6\,\text{mA}$

$V_{DS} = V_{DD} - I_D R_D = 16\,\text{V} - (5.6\,\text{mA})(2\,\text{k}\Omega)$
$= 16\,\text{V} - 11.2\,\text{V} = 4.8\,\text{V}$

$V_D = V_{DS} = 4.8\,\text{V}$

$V_G = V_{GS} = -2\,\text{V}$

$V_S = 0\,\text{V}$

| $V_{GS}$ | $I_D$ |
|---|---|
| 0 | $I_{DSS}$ |
| $0.3V_P$ | $I_{DSS}/2$ |
| $0.5V_P$ | $I_{DSS}/4$ |
| $V_P$ | 0mA |

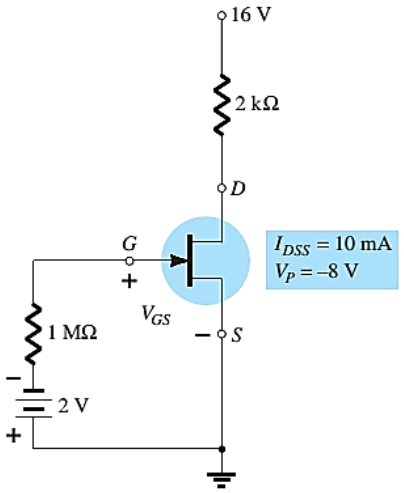


**FIG. 7.6**
*Example 7.1.*

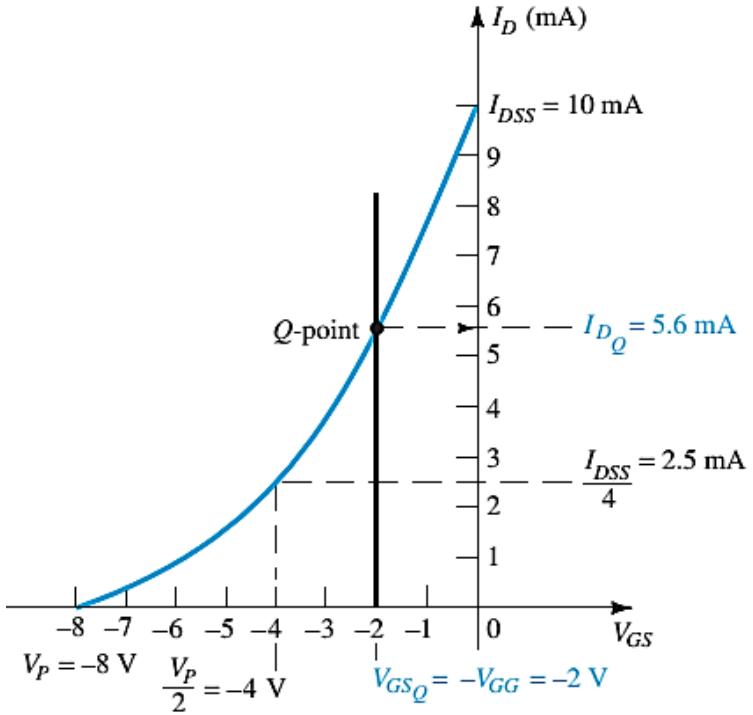


**FIG. 7.7**
*Graphical solution for the network of Fig. 7.6.*

# JFET: SELF-BIAS CONFIGURATION

- The self-bias configuration ***eliminates the need for two dc supplies.***

$$I_G \approx 0A$$

$$I_D = I_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

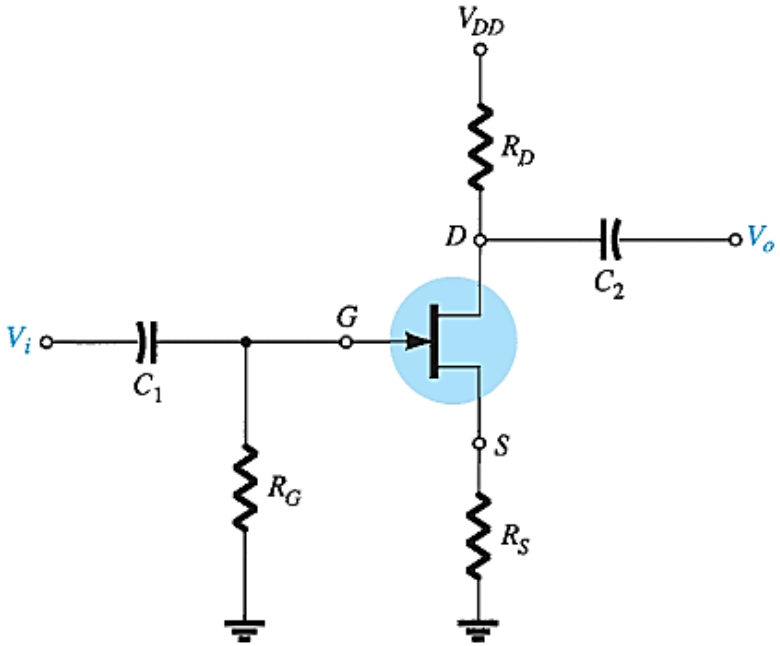


**FIG. 7.8**
*JFET self-bias configuration.*

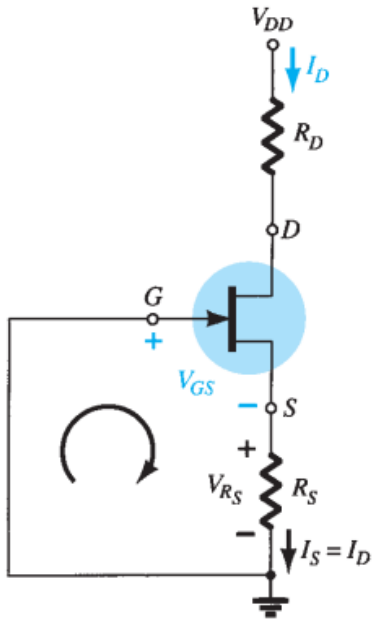


**FIG. 7.9**
*DC analysis of the self-bias configuration.*

# SELF-BIAS CONFIGURATION

- Can be solved using either Mathematical Approach or Graphical Approach:

## Mathematical Approach

$$V_{GS} = -I_D R_S$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

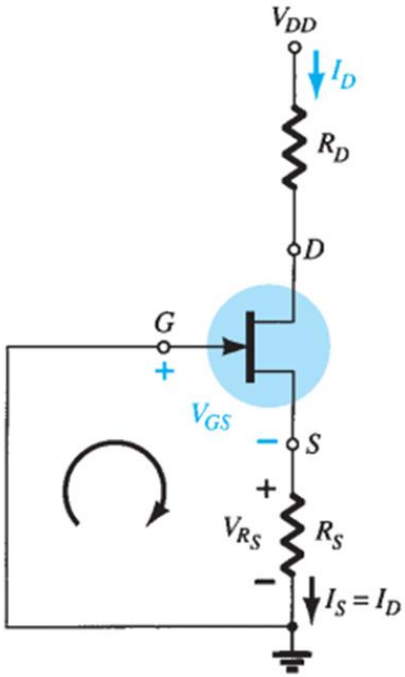


**FIG. 7.9**
*DC analysis of the self-bias configuration.*

# SELF-BIAS CONFIGURATION

## Graphical Approach

- Draw the device transfer characteristic using shorthand method.
- Draw the network load line
  - Use $V_{GS} = -I_D R_S$ to draw straight line.
  - First point, $I_D = 0, \quad V_{GS} = 0$
  - Second point, any point from $I_D = 0$ to $I_D = I_{DSS}$. Choose

$$I_D = \frac{I_{DSS}}{2} \; then$$

$$V_{GS} = -\frac{I_{DSS} R_S}{2}$$

- The Q-point obtained at the intersection of the straight line plot and the device characteristic curve.
- The quiescent value for $I_D$ and $V_{GS}$ can then be determined and used to find the other quantities of interest.

# SELF-BIAS CONFIGURATION

## Graphical Approach

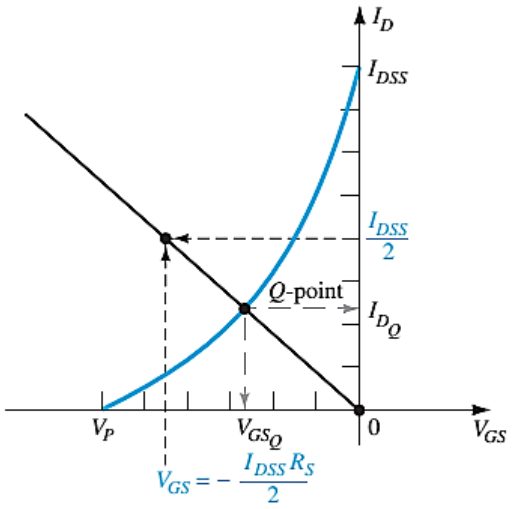


**FIG. 7.11**
*Sketching the self-bias line.*

# SELF-BIAS EXAMPLE

- Determine $V_{GSQ}$, $I_{DQ}$,$V_{DS}$,$V_S$,$V_G$ and $V_D$.

$$V_{GS} = -I_D R_S$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$V_{GS_Q} = -2.6\ \text{V}$

$V_S = I_D R_S$
$= (2.6\ \text{mA})(1\ \text{k}\Omega)$
$= \mathbf{2.6\ V}$

$V_{DS} = V_{DD} - I_D(R_S + R_D)$
$= 20\ \text{V} - (2.6\ \text{mA})(1\ \text{k}\Omega + 3.3\ \text{k}\Omega)$
$= 20\ \text{V} - 11.18\ \text{V}$
$= \mathbf{8.82\ V}$

$V_G = \mathbf{0\ V}$

$V_D = V_{DS} + V_S = 8.82\ \text{V} + 2.6\ \text{V} = \mathbf{11.42\ V}$

$V_D = V_{DD} - I_D R_D = 20\ \text{V} - (2.6\ \text{mA})(3.3\ \text{k}\Omega) = \mathbf{11.42\ V}$

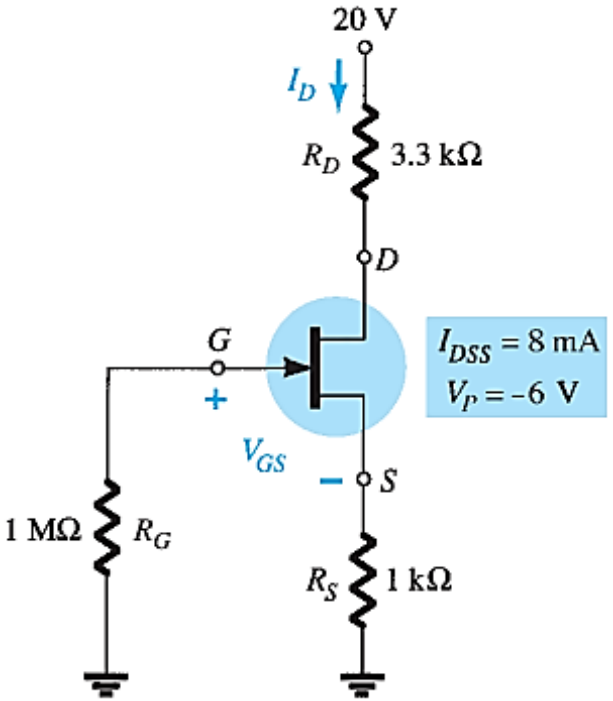


**FIG. 7.12**
*Example 7.2.*

# SELF-BIAS EXAMPLE Contd.

- Plot $I_D$ vs $V_{GS}$ and draw a line from the origin of the axis.

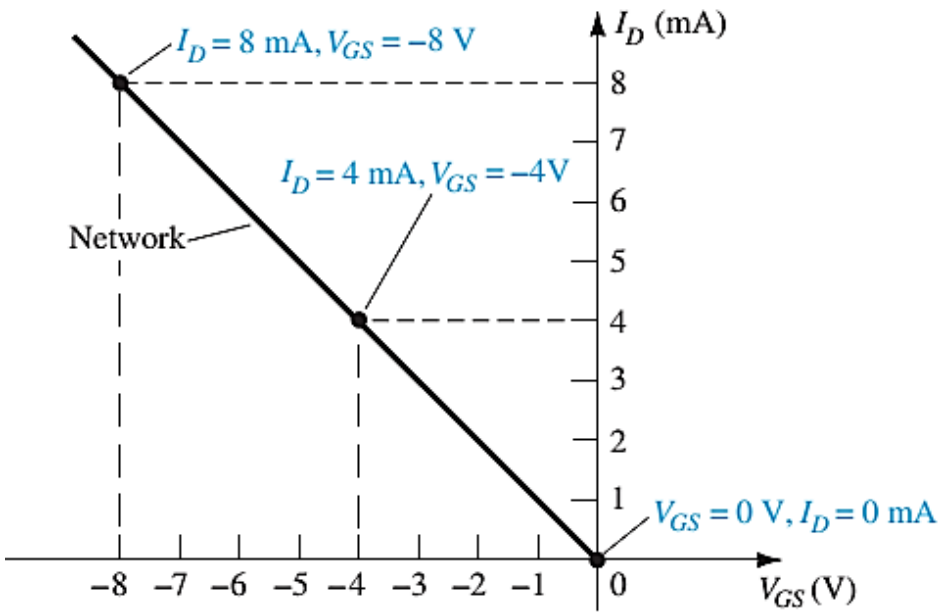


**FIG. 7.13**
*Sketching the self-bias line for the network of Fig. 7.12.*

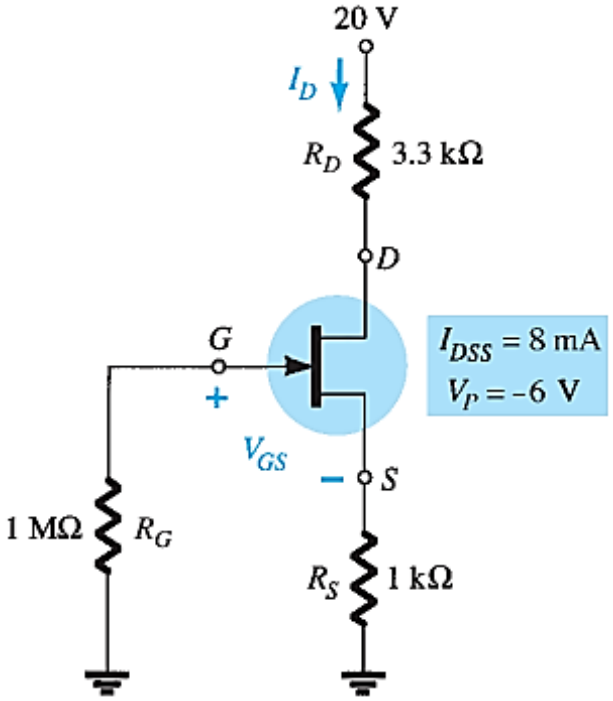


**FIG. 7.12**
*Example 7.2.*

# End of Lecture-6