# Electronic Devices

## Final Term
## Lecture - 10

Reference book:

**Electronic Devices and Circuit Theory (Chapter-8)**

Robert L. Boylestad and L. Nashelsky , (11th Edition)

# JFET Small Signal Model

## JFET Input Impedance $Z_i$

The input impedance of all commercially available JFETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i\,(\text{JFET}) = \infty\,\Omega \tag{8.10}$$

For a JFET a practical value of $10^9\ \Omega$ (1000 M$\Omega$) is typical, whereas a value of $10^{12}\ \Omega$ to $10^{15}\ \Omega$ is typical for MOSFETs and MESFETs.

## JFET Output Impedance $Z_o$

The output impedance of JFETs is similar in magnitude to that of conventional BJTs. On JFET specification sheets, the output impedance will typically appear as $g_{os}$ or $y_{os}$ with the units of $\mu$S. The parameter $y_{os}$ is a component of an *admittance equivalent circuit*, with the subscript $o$ signifying an *o*utput network parameter and $s$ the terminal (*s*ource) to which it is attached in the model. For the JFET of Fig. 6.20, $g_{os}$ has a range of 10 $\mu$S to 50 $\mu$S or 20 k$\Omega$ ($R = 1/G = 1/50\ \mu$S) to 100 k$\Omega$ ($R = 1/G = 1/10\ \mu$S).

In equation form,

$$Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}} \tag{8.11}$$

# JFET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the JFET transistor in the ac domain can be constructed. The control of $I_d$ by $V_{gs}$ is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 8.8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

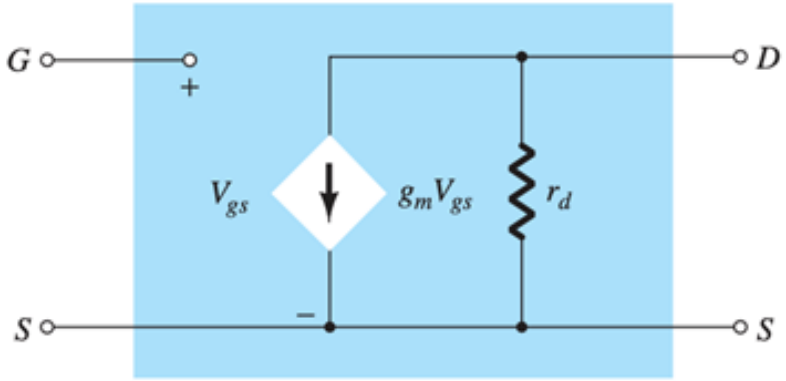


**FIG. 8.8**

*JFET ac equivalent circuit.*

# Example

**EXAMPLE 8.6** Given $g_{fs} = 3.8$ mS and $g_{os} = 20\ \mu$S, sketch the FET ac equivalent model.

***Solution:***

$$g_m = g_{fs} = 3.8\text{ mS} \qquad \text{and} \qquad r_d = \frac{1}{g_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

resulting in the ac equivalent model of Fig. 8.9.

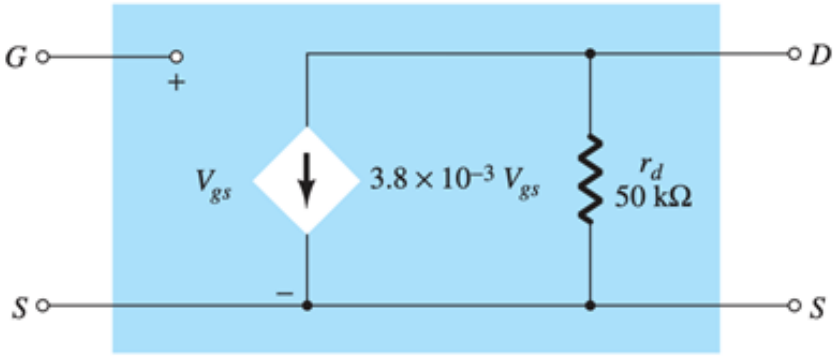


**FIG. 8.9**
*JFET ac equivalent model for Example 8.6.*

# FIXED-BIAS CONFIGURATION

Now that the JFET equivalent circuit has been defined, a number of fundamental JFET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of $Z_i$, $Z_o$, and $A_v$ for each configuration.

The *fixed-bias* configuration of Fig. 8.10 includes the coupling capacitors $C_1$ and $C_2$, which isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.

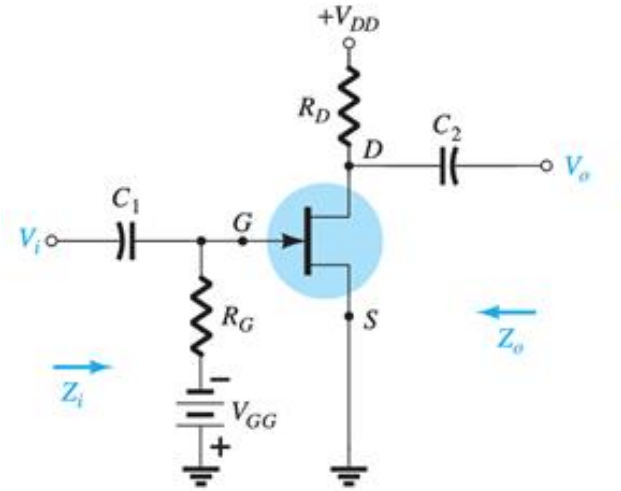


**FIG. 8.10**
*JFET fixed-bias configuration.*

# Continued.

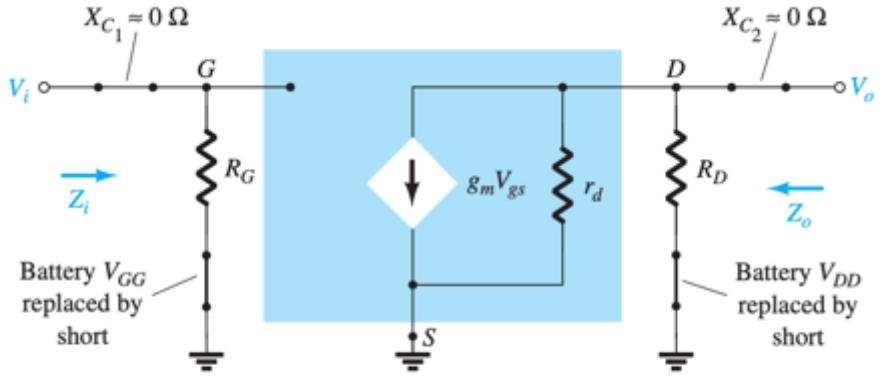


**FIG. 8.11**

*Substituting the JFET ac equivalent circuit unit into the network of Fig. 8.10.*

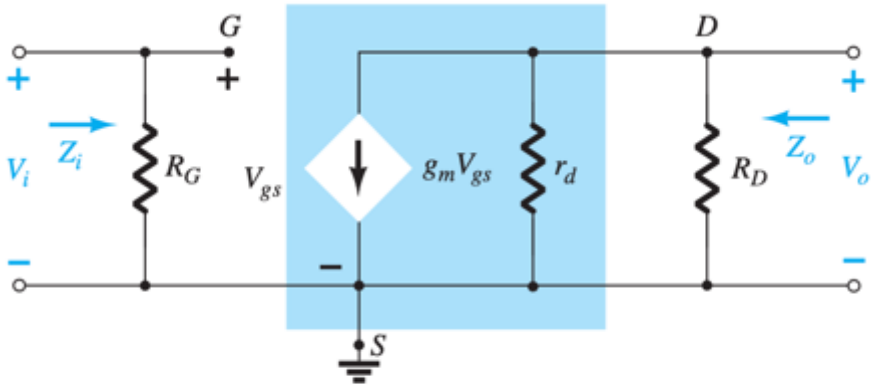


**FIG. 8.12**

*Redrawn network of Fig. 8.11.*

**$Z_i$** Figure 8.12 clearly reveals that

$$Z_i = R_G \tag{8.13}$$

because of the infinite input impedance at the input terminals of the JFET.

**$Z_o$** Setting $V_i = 0$ V as required by the definition of $Z_o$ will establish $V_{gs}$ as 0 V also. The result is $g_m V_{gs} = 0$ mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 8.13. The output impedance is

$$Z_o = R_D \| r_d \tag{8.14}$$

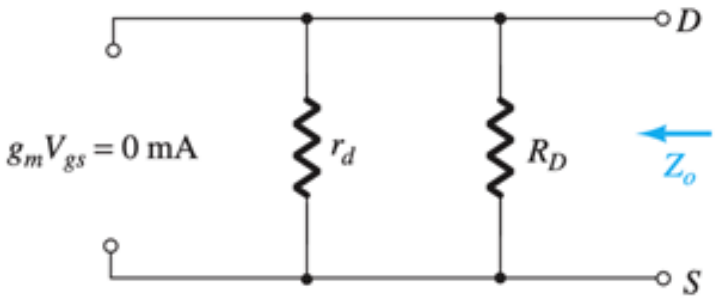


**FIG. 8.13**
*Determining $Z_o$.*

$$\boxed{Z_o \cong R_D} \quad r_d \geq 10R_D$$

**$A_v$** Solving for $V_o$ in Fig. 8.12, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but $$V_{gs} = V_i$$

and $$V_o = -g_m V_i(r_d \| R_D)$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)}$$

If $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m R_D} \quad r_d \geq 10R_D$$

**Phase Relationship** The negative sign in the resulting equation for $A_v$ clearly reveals a phase shift of 180° between input and output voltages.

**EXAMPLE 8.7** The fixed-bias configuration of Example 7.1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. 8.14 with an applied signal $V_i$. The value of $y_{os}$ is provided as 40 $\mu$S.

a. Determine $g_m$.
b. Find $r_d$.
c. Determine $Z_i$.
d. Calculate $Z_o$.
e. Determine the voltage gain $A_v$.
f. Determine $A_v$ ignoring the effects of $r_d$.

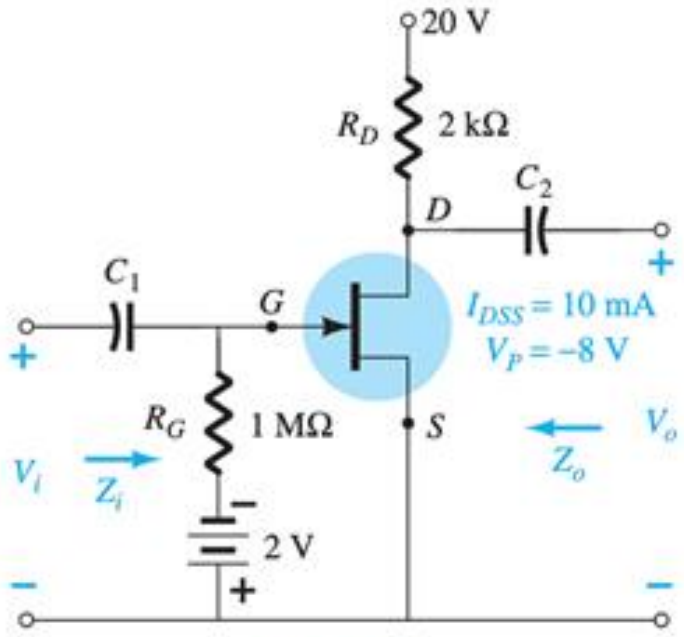


**FIG. 8.14**
*JFET configuration for Example 8.7.*

**Solution:**

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

b. $$r_d = \frac{1}{y_{os}} = \frac{1}{40\,\mu\text{S}} = \mathbf{25\,k\Omega}$$

c. $$Z_i = R_G = \mathbf{1\,M\Omega}$$

d. $$Z_o = R_D \| r_d = 2\,k\Omega \| 25\,k\Omega = \mathbf{1.85\,k\Omega}$$

e. $$A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\,k\Omega)$$
$$= \mathbf{-3.48}$$

f. $$A_v = -g_m R_D = -(1.88\text{ mS})(2\,k\Omega) = \mathbf{-3.76}$$

As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between $r_d$ and $R_D$ results in a difference of 8% in the solution.

# End of Lecture-10