# Electronic Devices

## Final Term
## Lecture - 05

Reference book:

**Electronic Devices and Circuit Theory (Chapter-6)**

Robert L. Boylestad and L. Nashelsky , (11$^{th}$ Edition)

# TRANSFER CURVE

- To determine $I_D$ given $V_{GS}$:

$$I_D = k(V_{GS} - V_T)^2$$

- where $V_T$ = threshold voltage or voltage at which the MOSFET turns on.

- k = constant found in the specification sheet
- k can also be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(on)}}{(V_{GS(ON)} - V_T)^2}$$

- $V_{DSsat}$ can also be calculated:

$$V_{Dsat} = V_{GS} - V_T$$

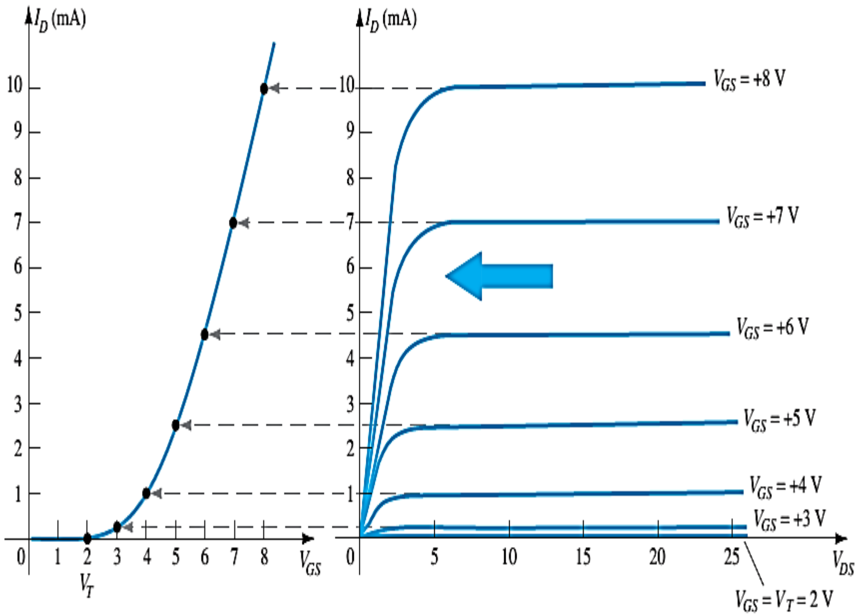



**FIG. 6.36**

*Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics.*

# P -CHANNEL ENHANCEMENT-TYPE MOSFETS

- The p-channel Enhancement-type MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.

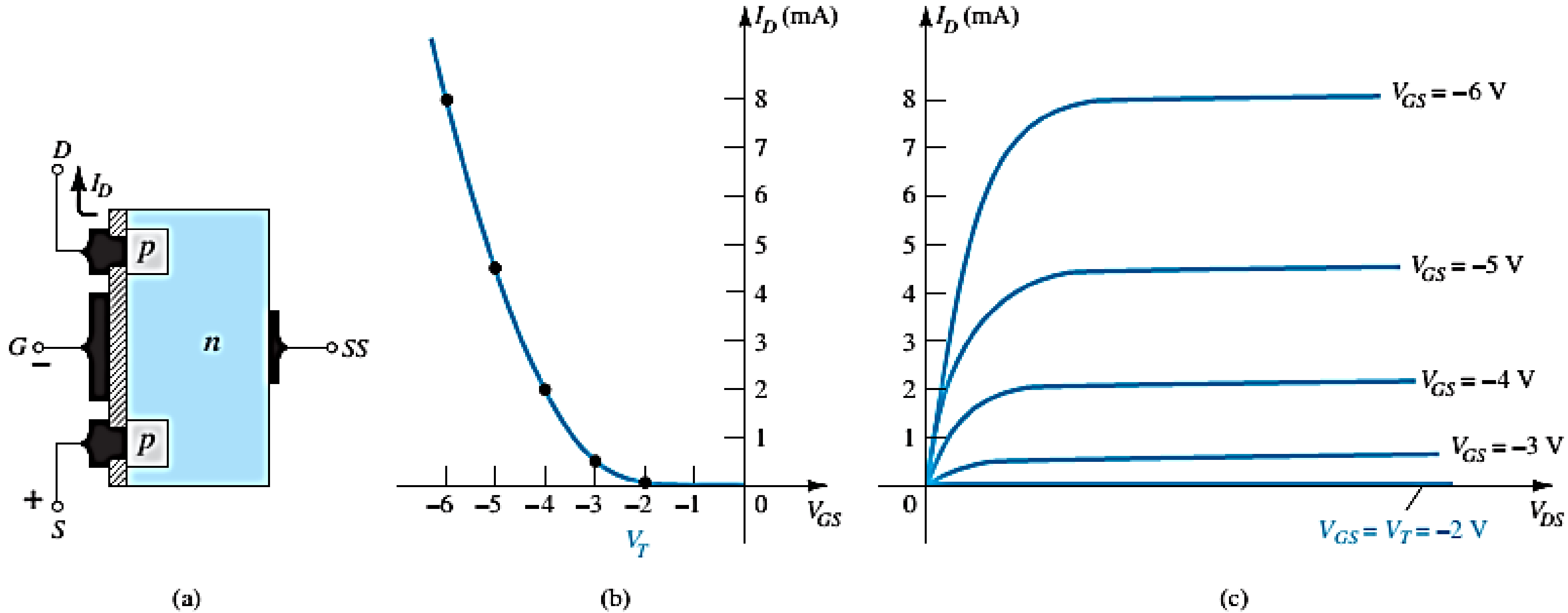



**FIG. 6.38**

*p-Channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.5 \times 10^{-3}$ A/V$^2$.*

# SYMBOLS

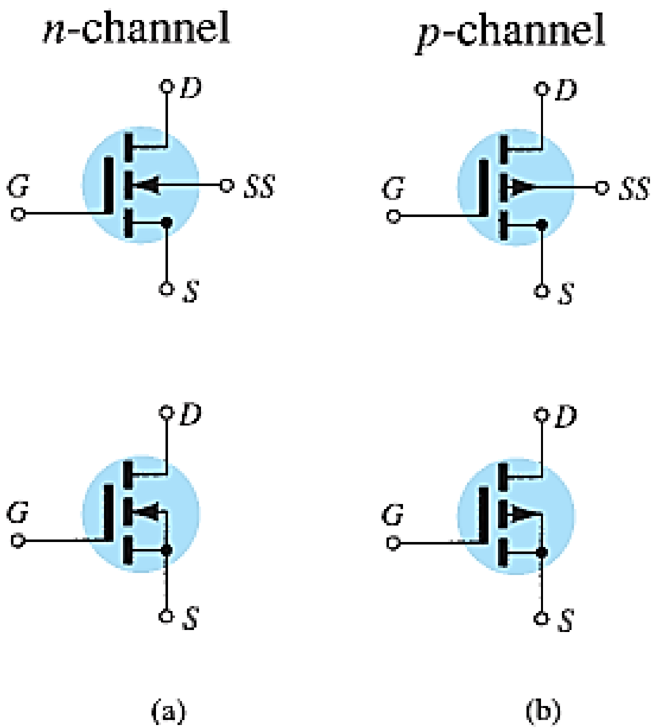



**FIG. 6.39**

*Symbols for: (a) n-channel enhancement-type MOSFETs and (b) p-channel enhancement-type MOSFETs.*

# DEPLETION-TYPE MOSFET CONSTRUCTION

- The Drain (D) and Source (S) connect to the to n-doped regions.
- These N-doped regions are connected via an n-channel. This n-channel is connected to the Gate (G) via a thin insulating layer of SiO2.
- The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS.

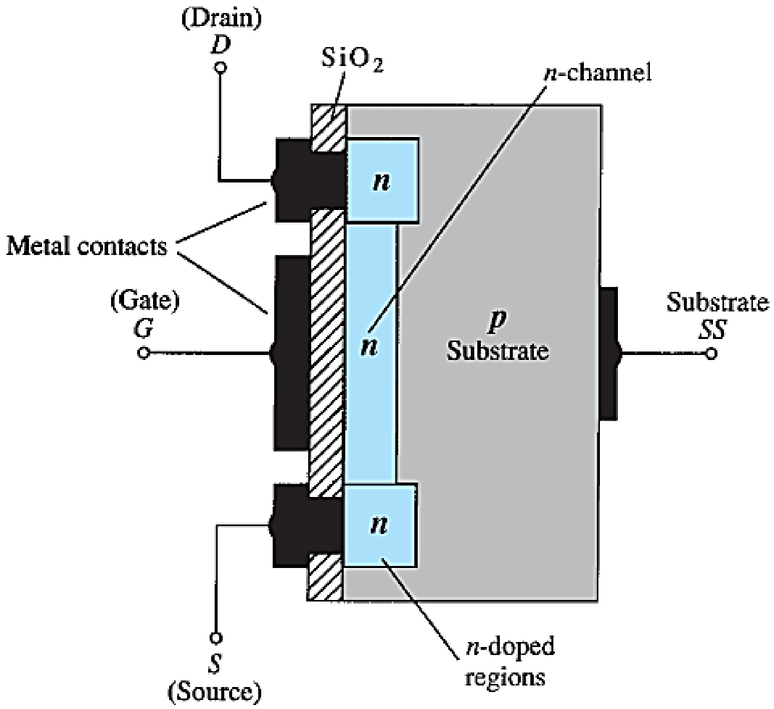



**FIG. 6.24**
*n-Channel depletion-type MOSFET.*

# BASIC OPERATION

- In Fig. 6.25 the gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage $V_{DD}$ is applied across the drain-to-source terminals.
- The result is an attraction of the free electrons of the n-channel for the positive voltage at the drain.
- The result is a current similar to that flowing in the channel of the JFET. In fact, the resulting current with $V_{GS}$ = 0 V continues to be labeled $I_{DSS}$.

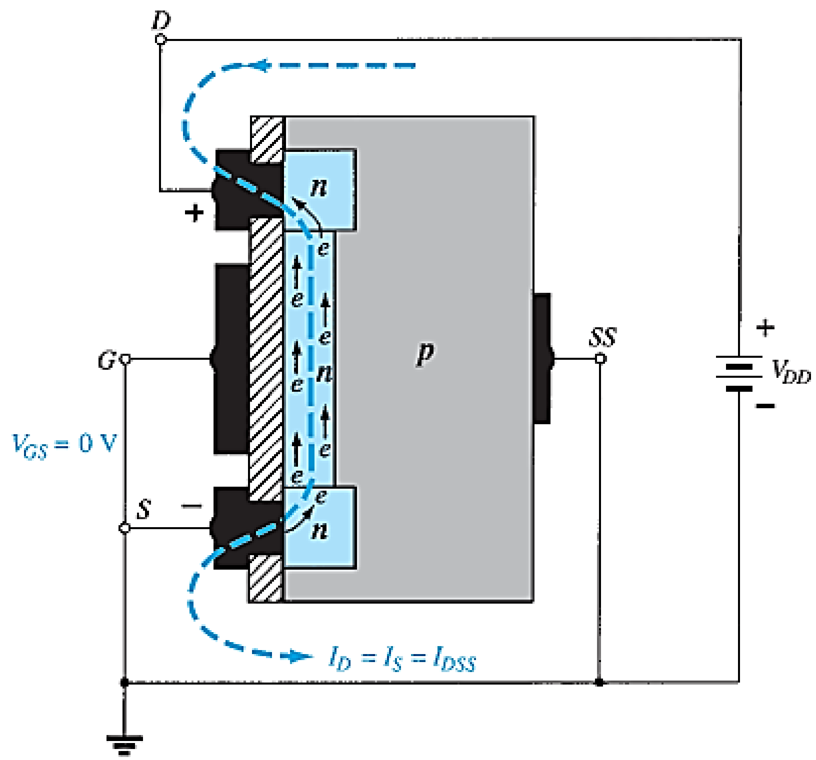



**FIG. 6.25**
*n-Channel depletion-type MOSFET with $V_{GS}$ = 0 V and applied voltage $V_{DD}$.*

# BASIC OPERATION

- A Depletion MOSFET can operate in two modes: Depletion or Enhancement mode.

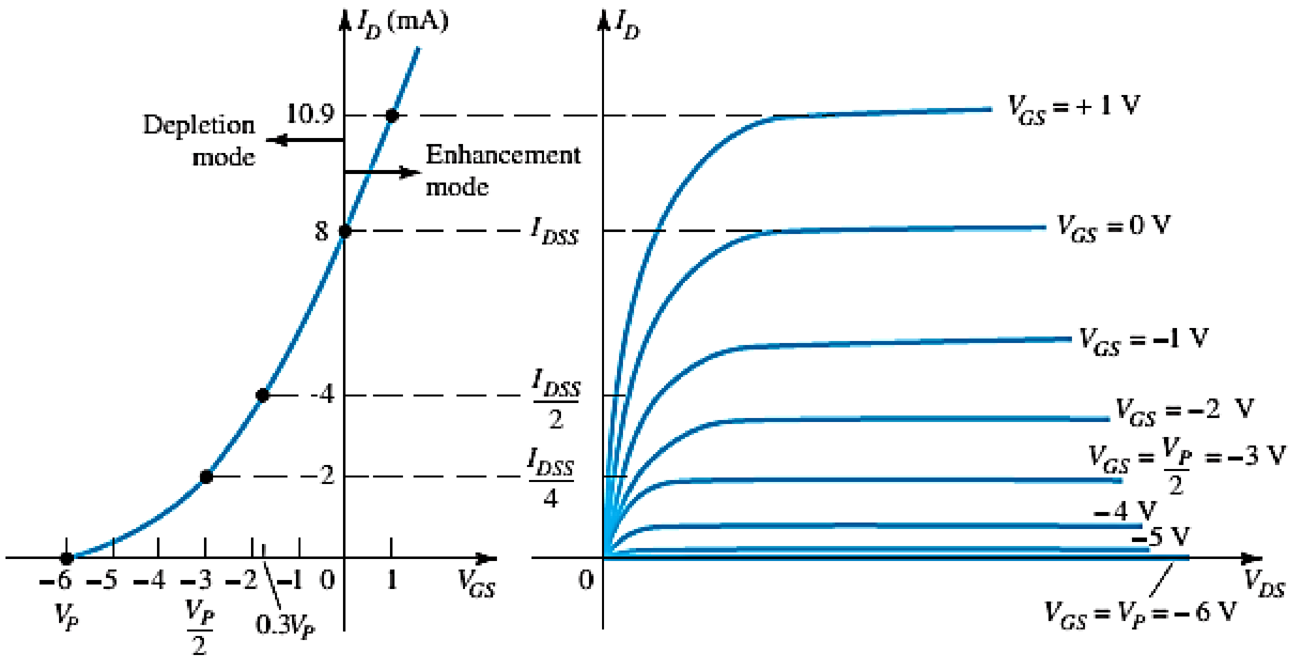



**FIG. 6.26**

*Drain and transfer characteristics for an n-channel depletion-type MOSFET.*

# BASIC OPERATION CONTD.

- In this figure $V_{GS}$ has been set at a negative voltage such as 1 V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract).

- Depending on the magnitude of the negative bias established by $V_{GS}$, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher the rate of recombination.

- The resulting level of drain current is therefore reduced with increasing negative bias for $V_{GS}$ for $V_{GS}$ =1 V, 2 V, and so on, to the pinch-off level of 6 V. The resulting levels of drain current and the plotting of the transfer curve proceeds exactly as described for the JFET.

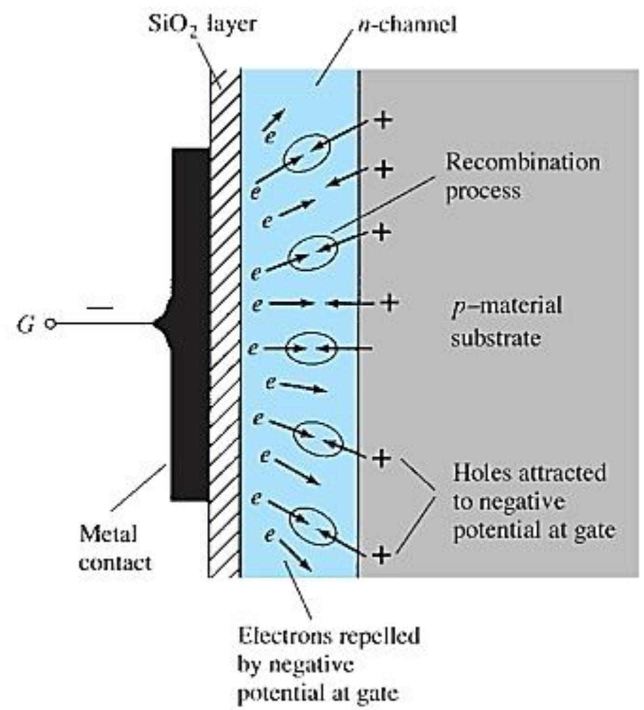



**FIG. 6.27**

*Reduction in free carriers in a channel due to a negative potential at the gate terminal.*

# DEPLETION-TYPE MOSFET IN *DEPLETION MODE*

- ***Depletion mode:***

- The characteristics are similar to the JFET.
- When $V_{GS}$ = 0V, $I_D$ = $I_{DSS}$
- When $V_{GS}$ < 0V, $I_D$ < $I_{DSS}$

- The formula used to plot the Transfer Curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

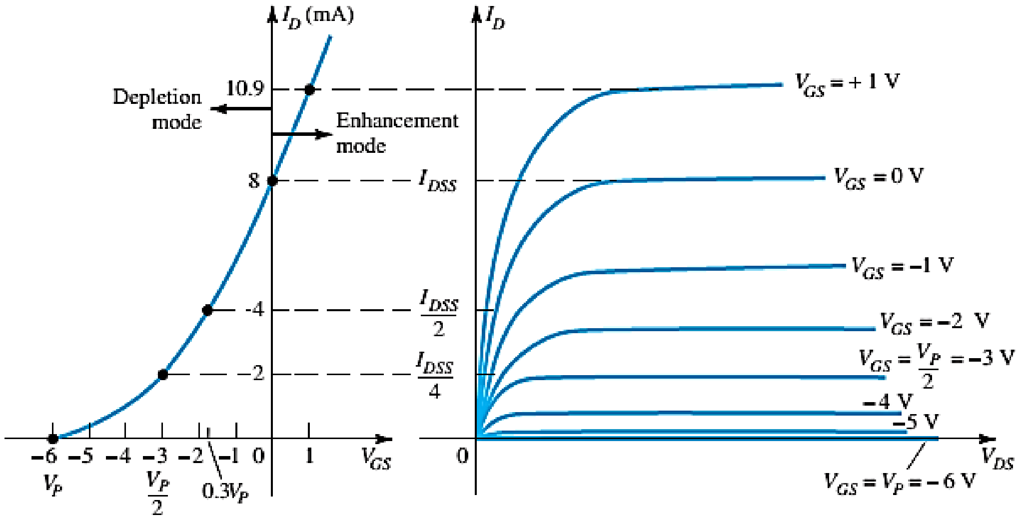



**FIG. 6.26**
*Drain and transfer characteristics for an n-channel depletion-type MOSFET.*

# ENHANCEMENT MODE

- For positive values of $V_{GS}$, the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles.

- As the gate-to-source voltage continues to increase in the positive direction, the drain current will increase at a rapid rate.

- The application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS}$ =0 V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the enhancement region,

- The region between cutoff and the saturation level of $I_{DSS}$ referred to as the depletion region.

# DEPLETION-TYPE MOSFET IN ***ENHANCEMENT MODE***

- ***Enhancement mode:***
- $V_{GS}$ > 0V, $I_D$ increases above $I_{DSS}$.
- The formula used to plot the Transfer Curve still applies:

(note that $V_{GS}$ is now a positive polarity)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

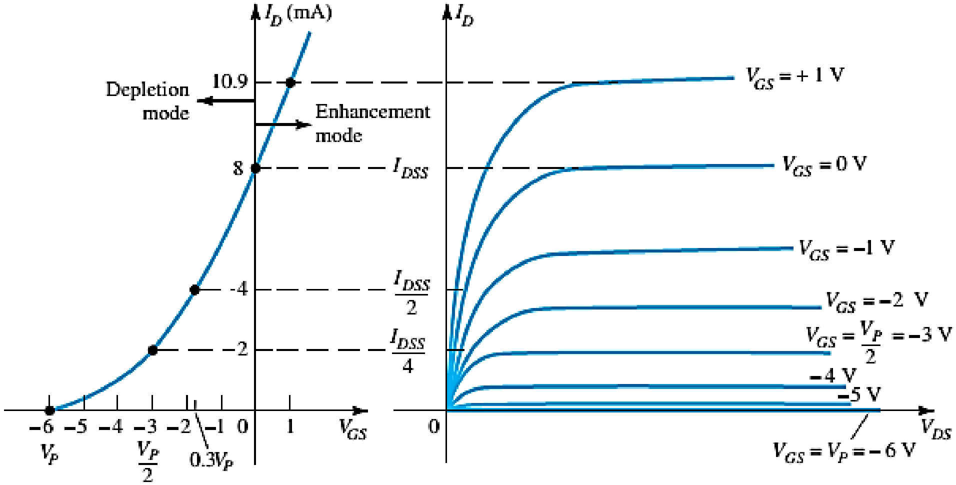



**FIG. 6.26**
*Drain and transfer characteristics for an n-channel depletion-type MOSFET.*

# P-CHANNEL DEPLETION-TYPE MOSFET

- The p-channel Depletion-type MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.

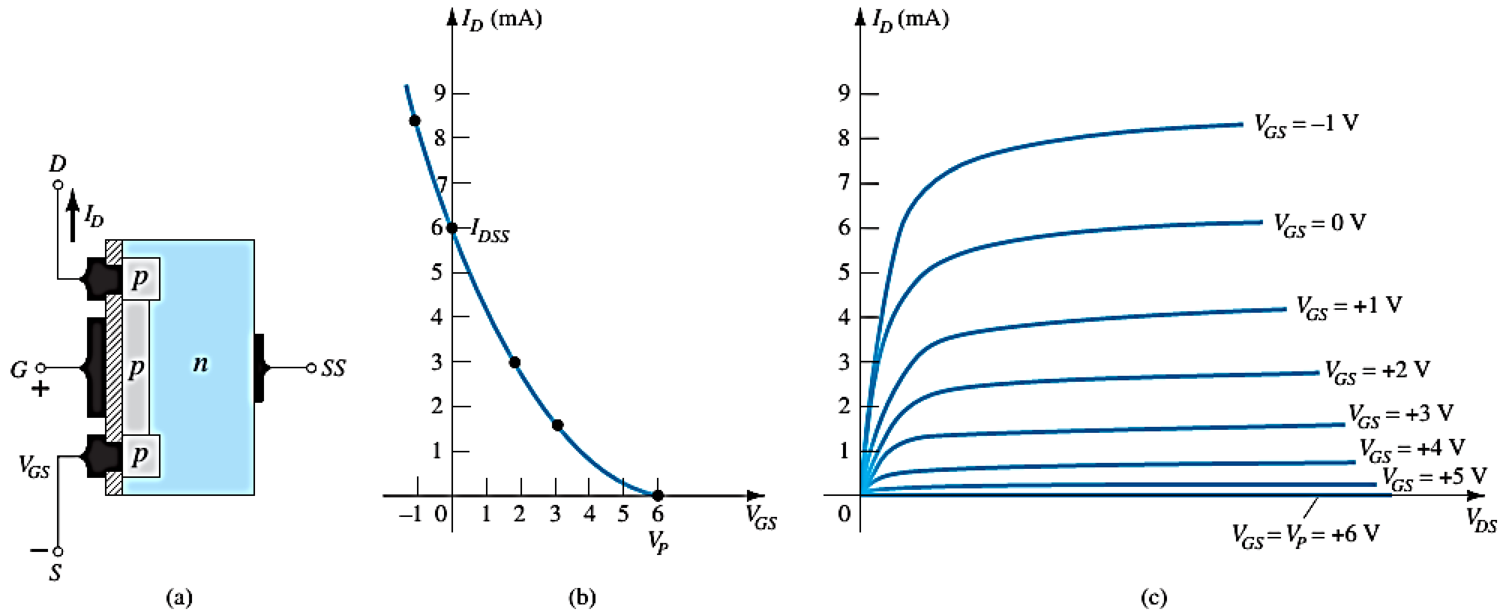



**FIG. 6.29**

*p-Channel depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = +6$ V.*

# SYMBOLS

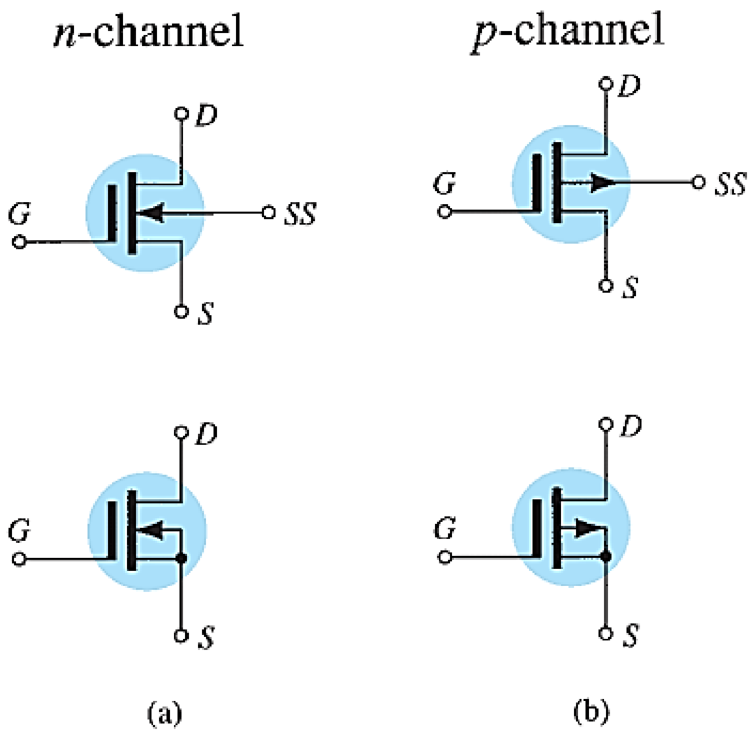
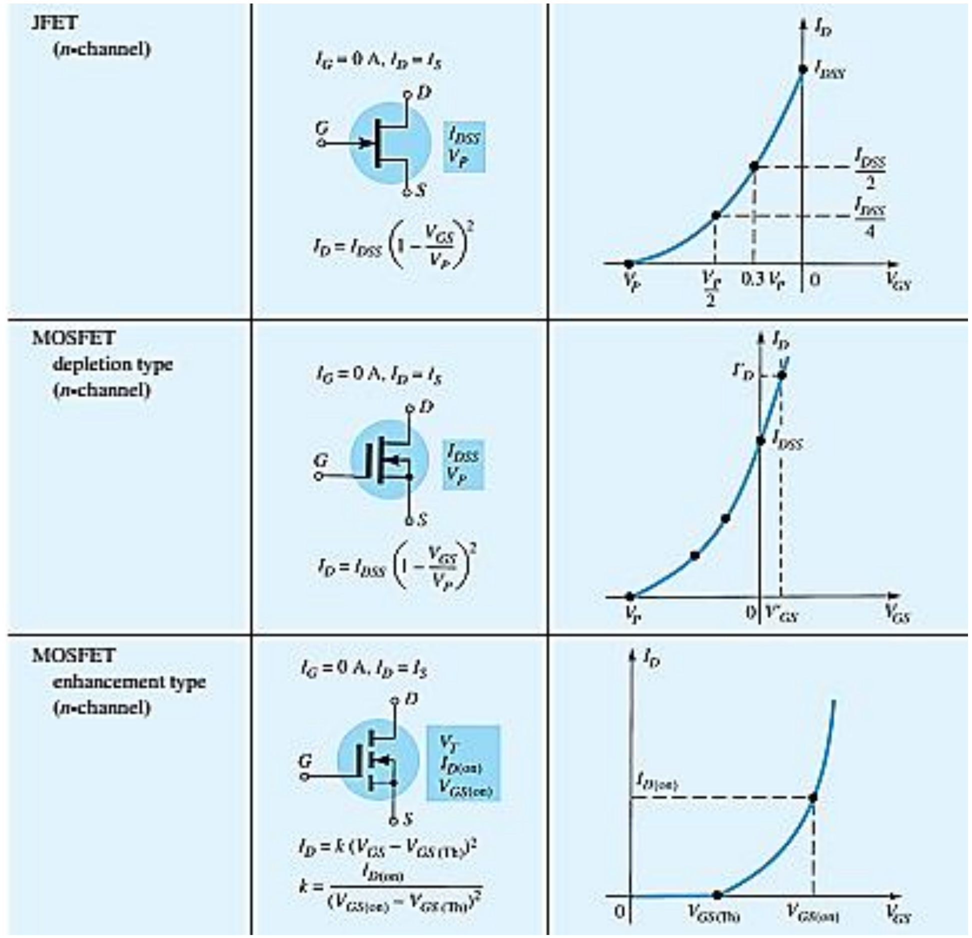



**FIG. 6.30**

*Graphic symbols for: (a) n-channel depletion-type MOSFETs and (b) p-channel depletion-type MOSFETs.*

# SUMMARY TABLE



# MOSFET HANDLING

- MOSFETs are ***very static sensitive***. Because of the very thin SiO2 layer between the external terminals and the layers of the device, any small electrical discharge can stablish an unwanted conduction.

- Protection:
  - Always transport in a static sensitive bag.
  - Always wear a static strap when handling MOSFETS.
  - Apply voltage limiting devices between the Gate and Source, such as back-to-back Zeners to limit any transient voltage.

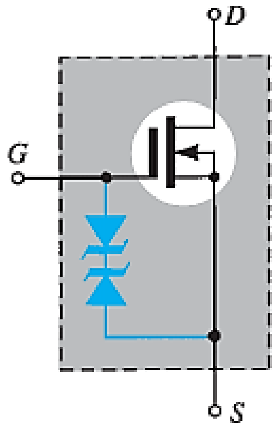



**FIG. 6.42**
*Zener-protected MOSFET.*

# CMOS

- CMOS – Complementary MOSFET p-channel and n-channel MOSFET on the same substrate.
- Advantage:
  - Useful in logic circuit designs
  - Higher input impedance
  - Faster switching speeds
  - Lower operating power levels
- **Application:**
  - CMOS Inverter

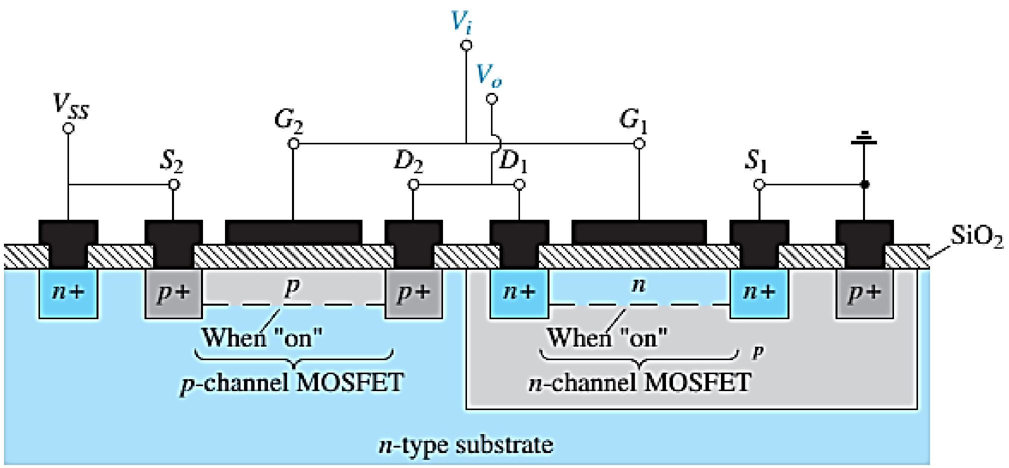



**FIG. 6.44**
*CMOS with the connections indicated in Fig. 6.45.*

# CMOS INVERTER

- An inverter is a logic element that "inverts" the applied signal. That is, if the logic levels of operation are 0V (0-state) and 5V (1-state), an input level of 0V will result in an output level of 5V, and vice versa.

- Here, ***both gates are connected to the applied signal*** and ***both drain to the output $V_o$***. *The* ***source of the p-channel MOSFET ($Q_2$)*** *is* ***connected*** directly to the ***applied voltage $V_{SS}$***, *while the* ***source of the n-channel MOSFET ($Q_1$)*** *is* ***connected to ground.***

- *Here, the application* of 5V at the input should result in approximately 0 V at the output. ***With 5V at $V_i$*** (with respect to ground), ***$V_{GS1}$ = $V_i$*** *and* ***$Q_1$ is "on,"*** *resulting in a relatively* ***low resistance between drain and source.***

- Since ***$V_i$ and $V_{SS}$ are at 5 V, $V_{GS2}$ = 0 V***, *which is* ***less than the required $V_T$*** *for the device, resulting in* ***an "off" state***. The resulting resistance level between drain and source is ***quite high for $Q_2$.***

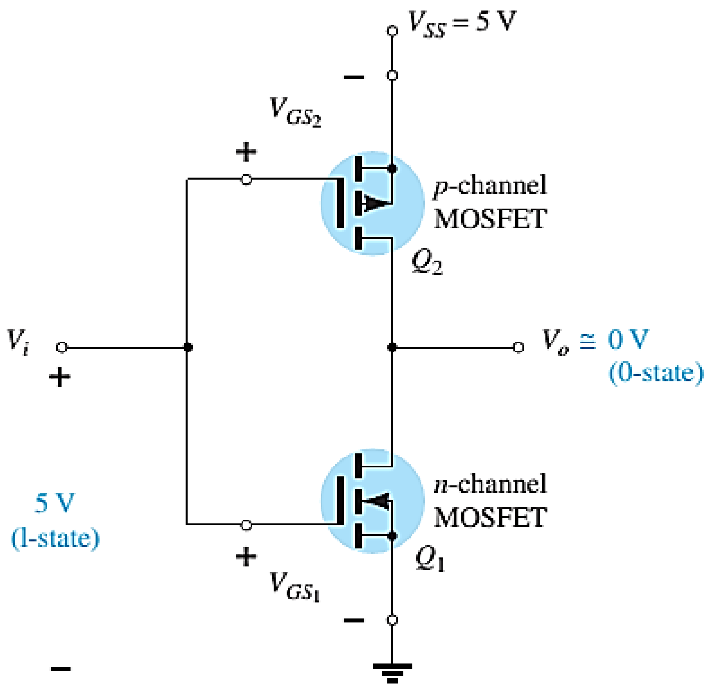



**FIG. 6.45**
*CMOS inverter.*

# CMOS INVERTER

- A simple application of the voltage-divider rule will reveal that ***$V_o$ is very close to 0 V or the 0-state, establishing the desired inversion process.***

- *For* an applied voltage ***$V_i$ of 0V (0-state), $V_{GS1}$ = 0V and $Q_1$ will be off with $V_{SS2}$ =-5V***, turning on ***the p-channel MOSFET. The result is that $Q_2$ will present a small*** resistance level, ***$Q_1$ a high resistance, and $V_o$ =$V_{SS}$ =5 V (the 1-state).***

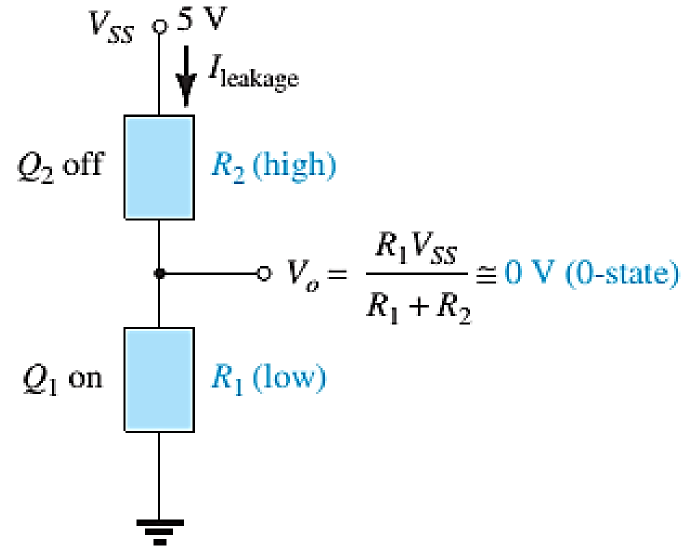



**FIG. 6.46**
*Relative resistance levels for $V_i = 5$ V (1-state).*

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