COMBINATIONAL LOGIC CIRCUITS

Digital Logic & Circuit Design

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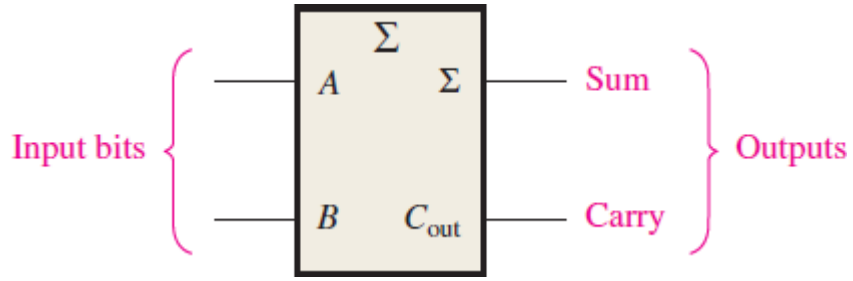
Steps for Digital System Designing

1. You need to draw a block diagram to identify how many inputs and outputs are there
2. Identify and write down the operation/behavior of the system.
3. From the operation/behavior develop a truthtable to relate the effects of input on the output
4. From the truthtable, write down the standard output expressions. (in class I discuss standard SOP expressions only.)
5. Minimize the standard output expression and find the simplified output expression using either rules of Boolean algebra or using k-map.
6. Draw the logic gate circuit diagram using the simplified output expressions.

HALF ADDER

1. **Block Diagram**



Operation & Basic Rules for Binary Addition

2. **Operation = A + B**

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 10$$

3. Half-adder truth table.

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

4. **STANDARD Output SOP Expression**

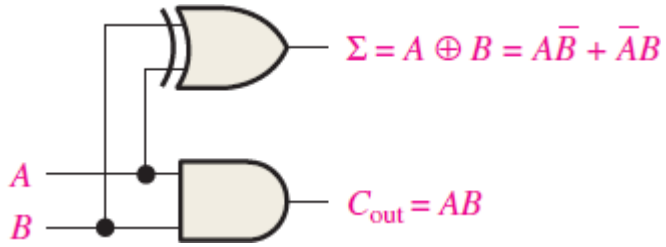
Sum=A'B+AB'

C_{out}=A.B

5. **Simplified Output SOP Expression**

$$\Sigma = A \oplus B \qquad C_{out} = AB$$

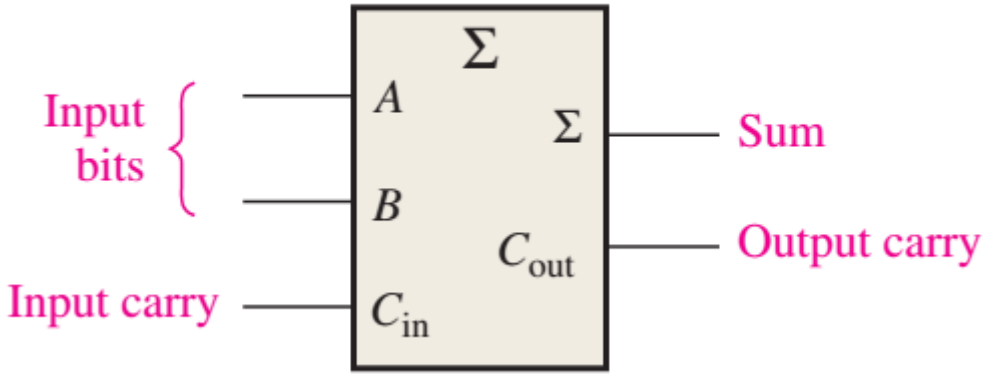
6. **Logic Gate Diagram**



FULL ADDER

1
11-A
+01-B
100

1. **Block Diagram**



2. **Operation = A + B + C_{in}**

3.

TABLE 6–2

Full-adder truth table.

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C_{in} = input carry, sometimes designated as *CI*
C_{out} = output carry, sometimes designated as *CO*
Σ = sum
A and B = input variables (operands)

(A⊕B)=Z
(A⊕B)'=Z'
$C_{in}Z'+C_{in}'Z$
$Z⊕C_{in}$

4. **STANDARD Output SOP Expression**

Sum= $A'B'C_{in}+A'BC_{in}'+A.B'.C_{in}'+A.B.C_{in}$
$=C_{in}(A'B'+AB)+C_{in}'(A'B+AB')$
$=C_{in}.(A⊙B)+C_{in}'(A⊕B)$
$=C_{in}.(A⊕B)'+C_{in}'(A⊕B)$
$=[(A⊕B)⊕C_{in}]$

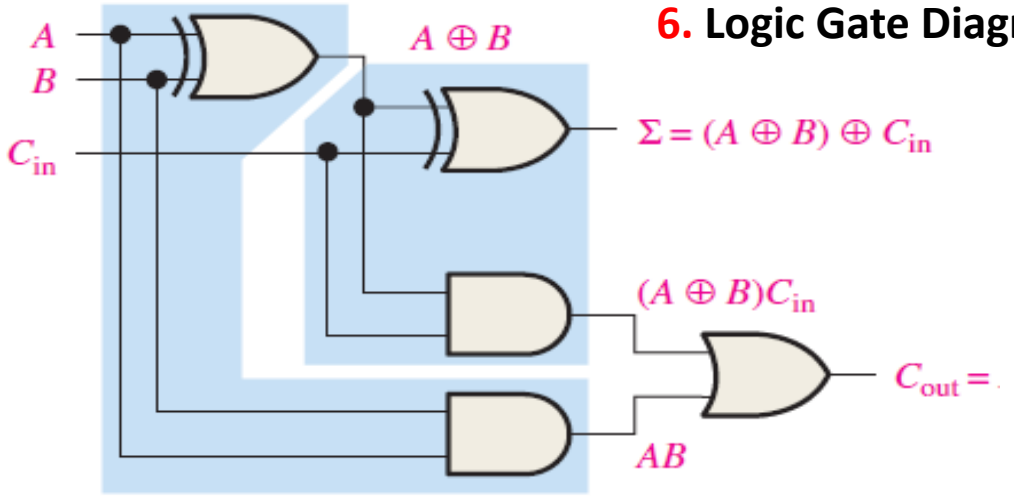
$C_{out}= A'BC_{in}+AB'C_{in}+A.B.C_{in}'+A.B.C_{in}$
$=C_{in}(A'B+AB')+AB(C_{in}'+C_{in})$
$=C_{in}.(A⊕B)+AB$

5. **Simplified Output SOP Expression**

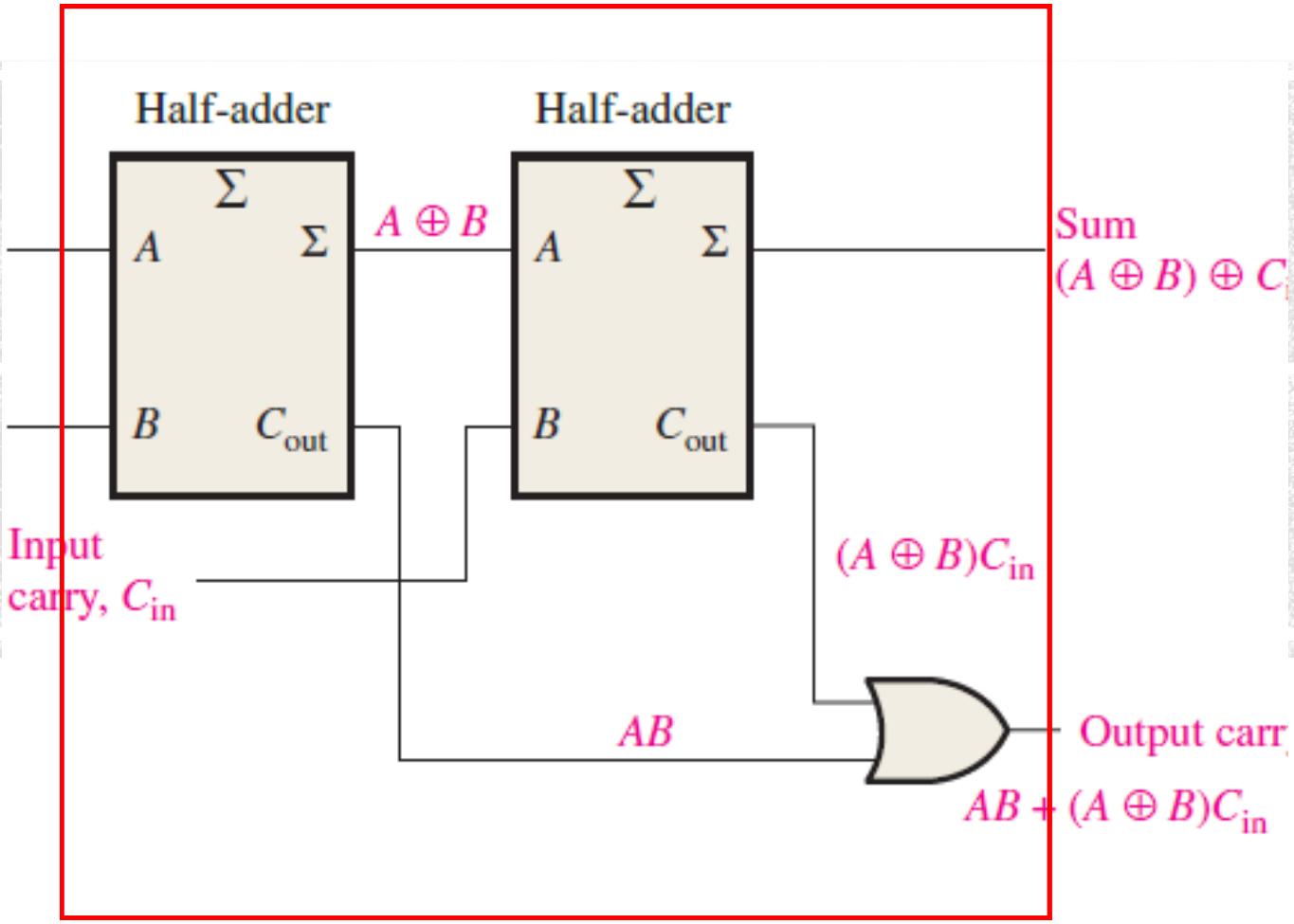
$$\Sigma = (A \oplus B) \oplus C_{in}$$

$$C_{out} = AB + (A \oplus B)C_{in}$$

6. **Logic Gate Diagram**



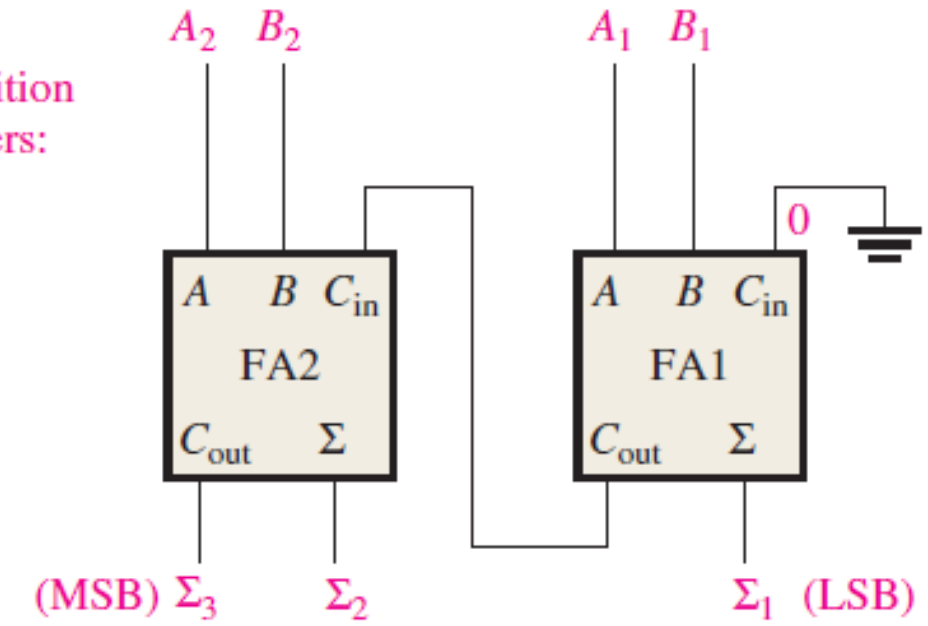
FULL ADDER WITH HALF ADDERS

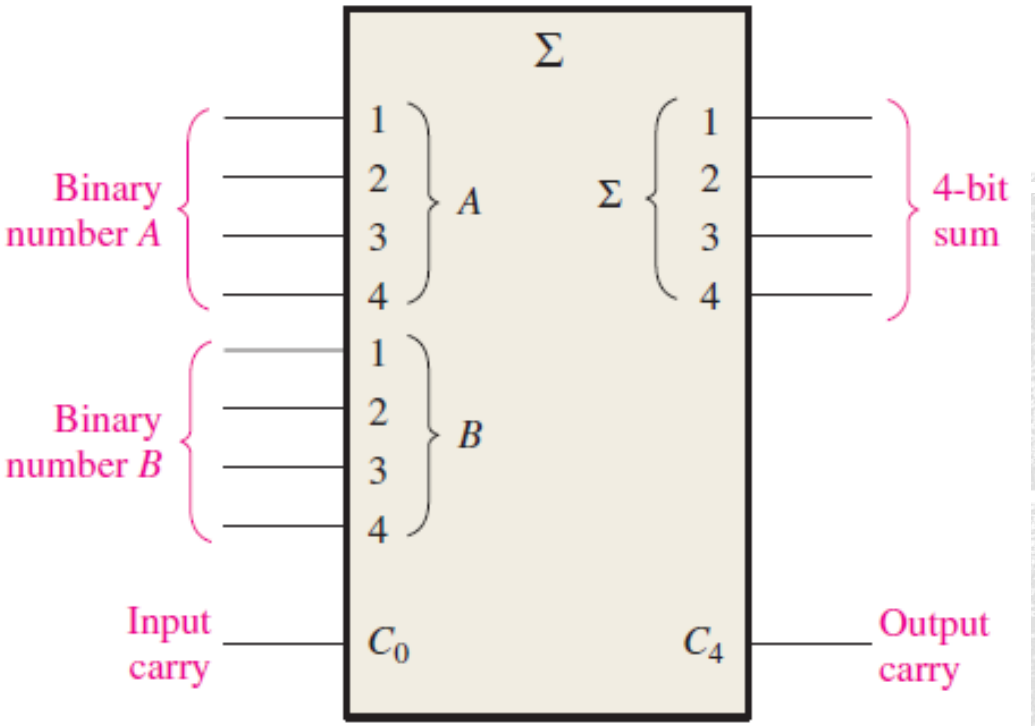


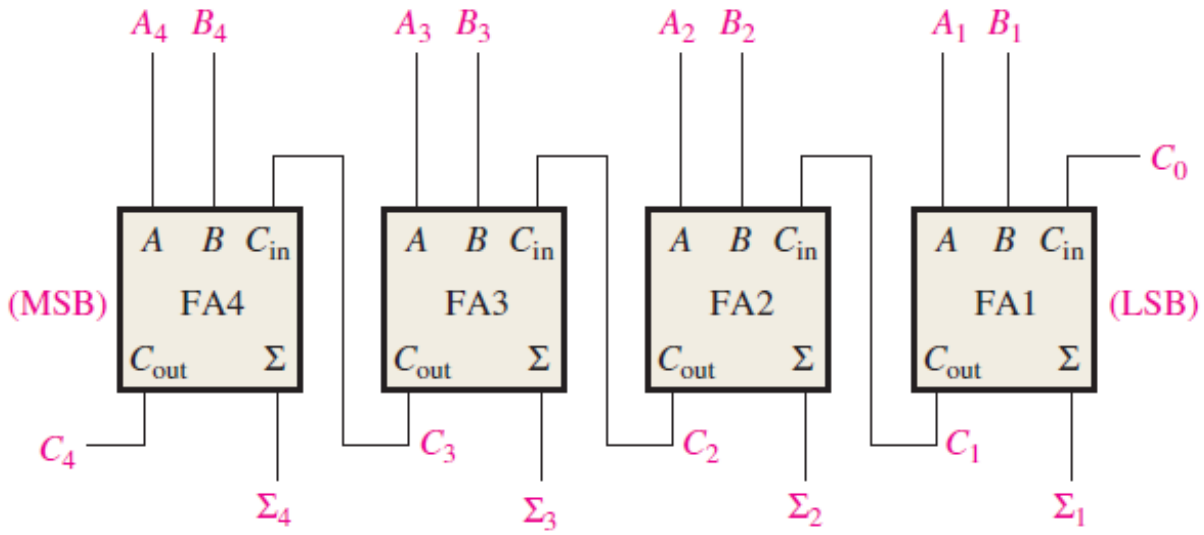
2-BIT PARALLEL ADDER

General format, addition of two 2-bit numbers:

$$\begin{array}{r} A_2A_1 \\ +\ B_2B_1 \\ \hline \Sigma_3\Sigma_2\Sigma_1 \end{array}$$

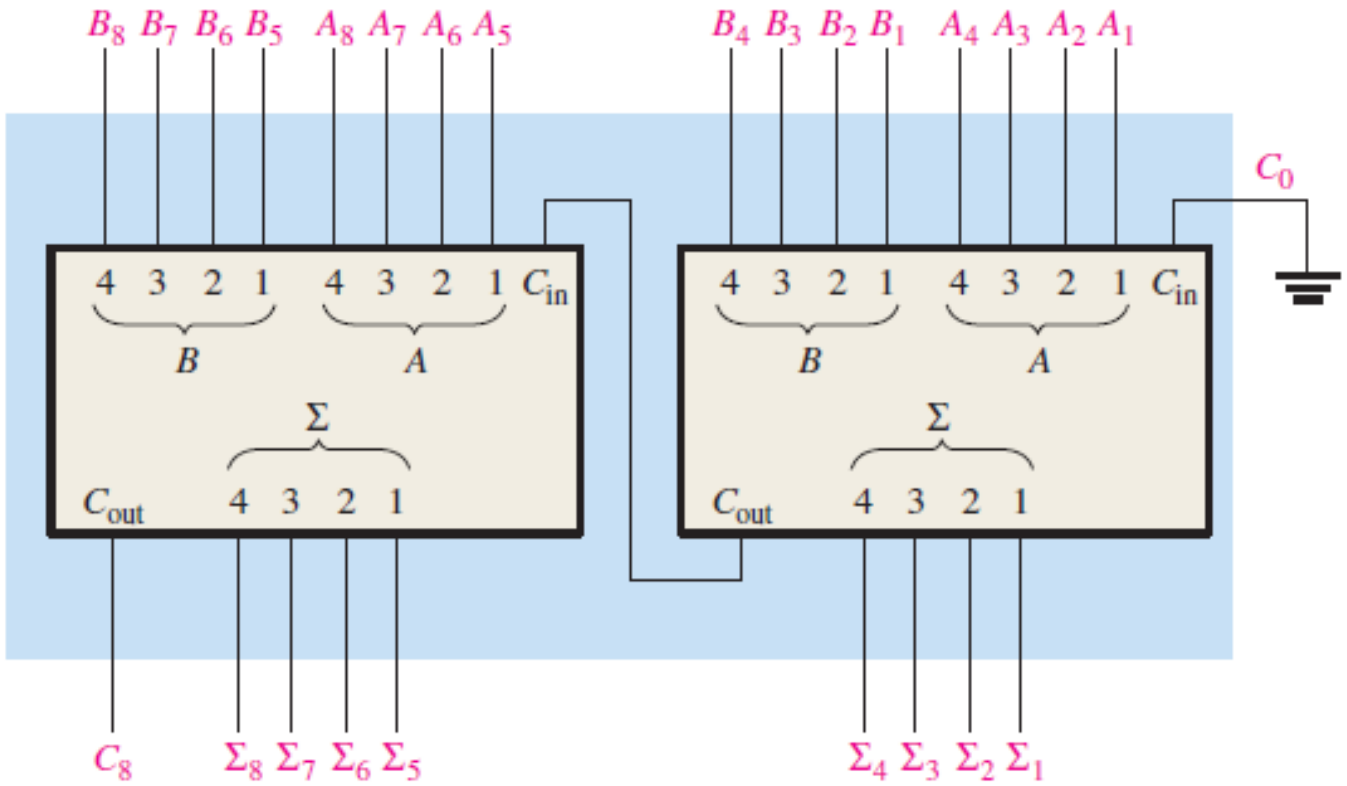




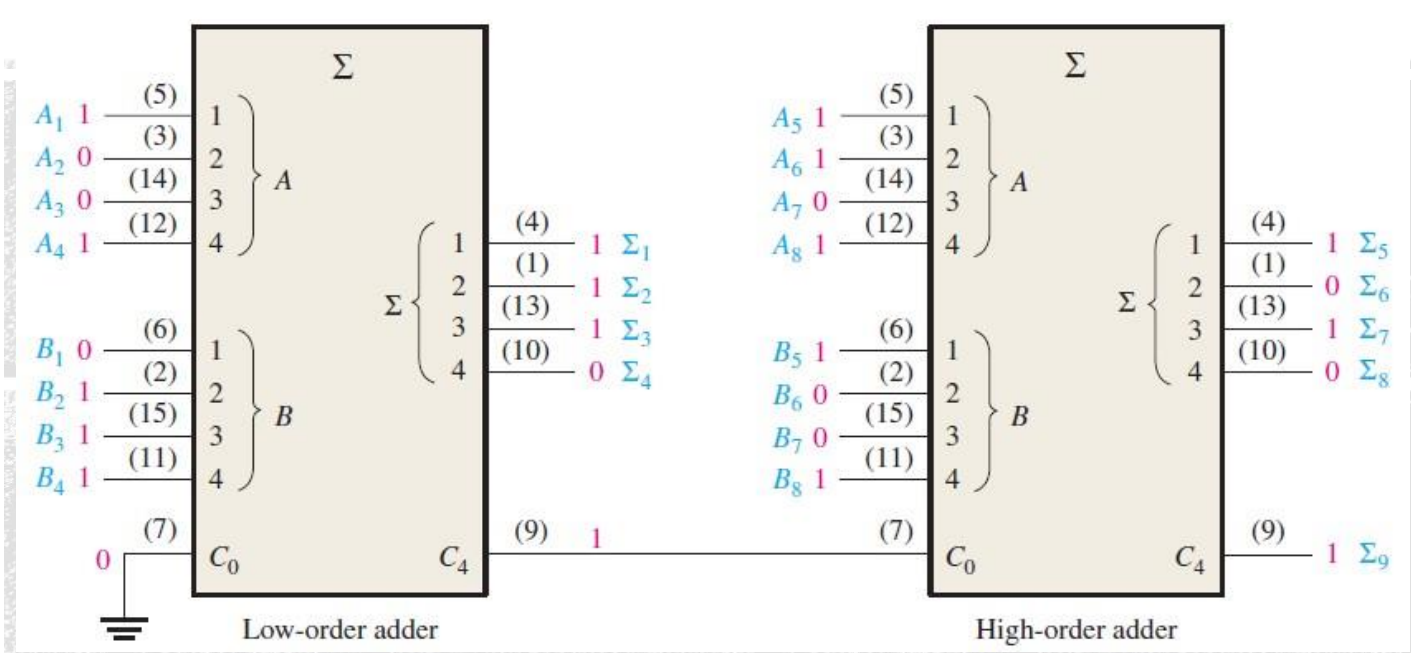


4-BIT PARALLEL ADDER

ADDER EXPANSION



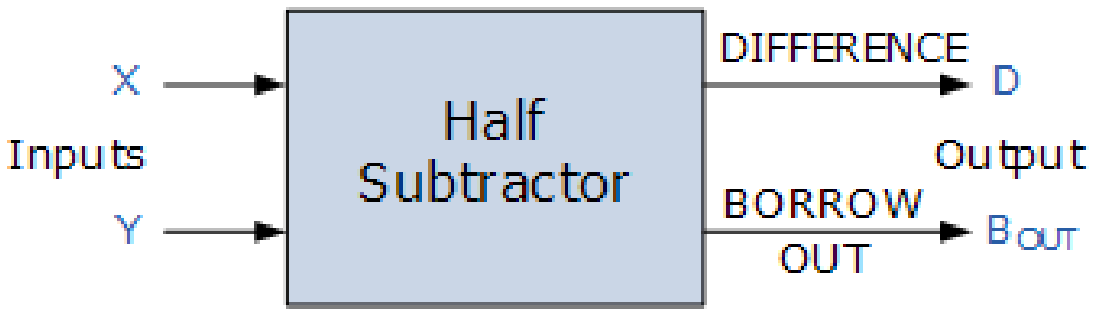
ADDER EXPANSION EXAMPLE



10111001
+10011110

HALF SUBTRACTOR

Block Diagram



Operation = x - y

Truthtable

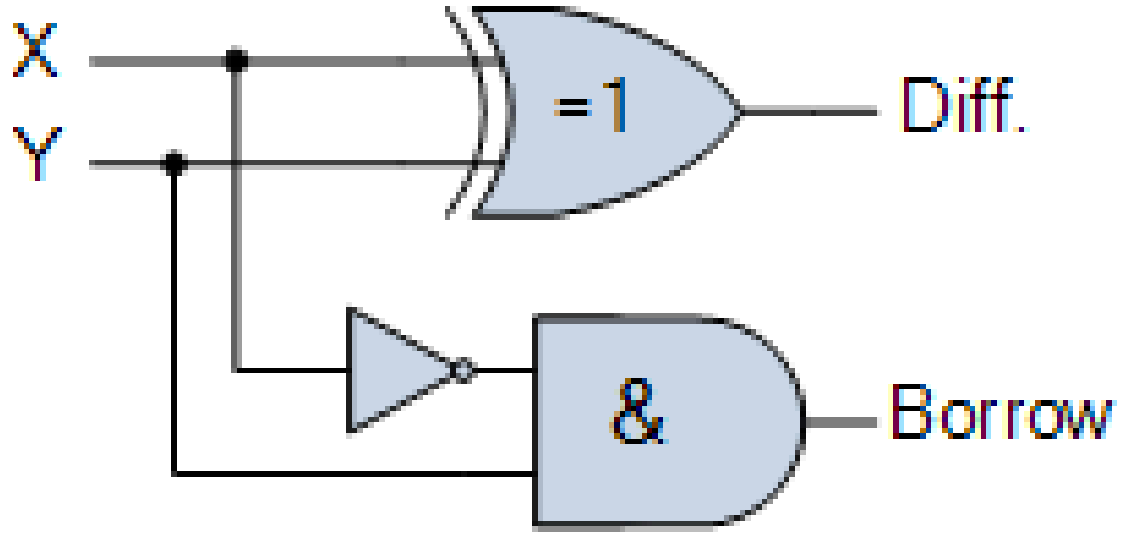
x	y	d	bout
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Output Expressions

D=x'y+xy'
D=x⊕y

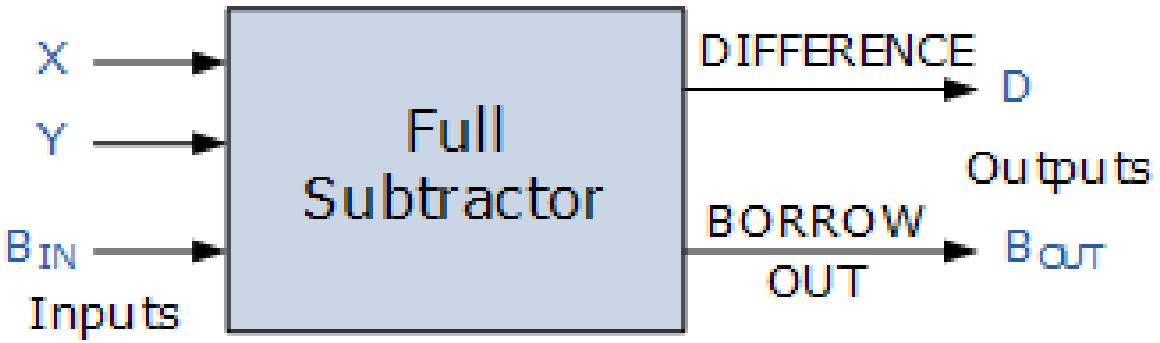
Bout=x'y

Logic Gate Diagram



FULL SUBTRACTOR

Block Diagram



Operation = X – Y - B_{IN}

= X - (Y+B_{IN})

X	Y	B_{IN}	D	B_{OUT}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$D= X'Y'B_{in}+X'YB_{in}'+X.Y'.B_{in}'+X.Y.B_{in}$

$=B_{in}\ (X'Y'+XY)+B_{in}'(X'Y+XY')$

$=B_{in}.(X\odot Y)+B_{in}'(X\oplus Y)$

$=B_{in}.(X\oplus Y)'+B_{in}'(X\oplus Y)$

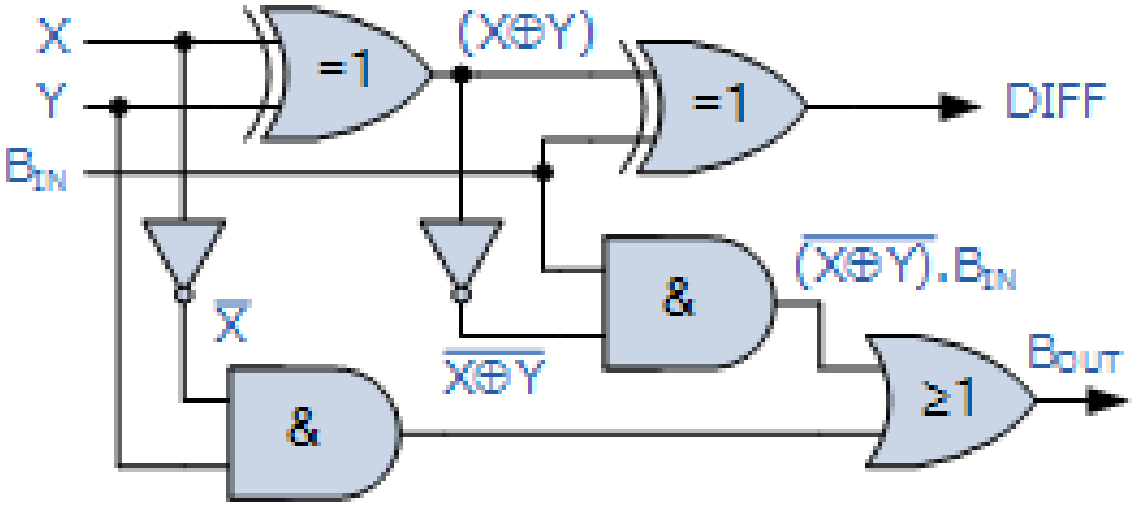
$=[(X\oplus Y)\oplus B_{in}]$

$B_{out}= X'Y'B_{in}+X'YB_{in}'+X'.Y.B_{in}+X.Y.B_{in}$

$=B_{in}\ (X'Y'+XY)+ X'Y(B_{in}'+B_{in})$

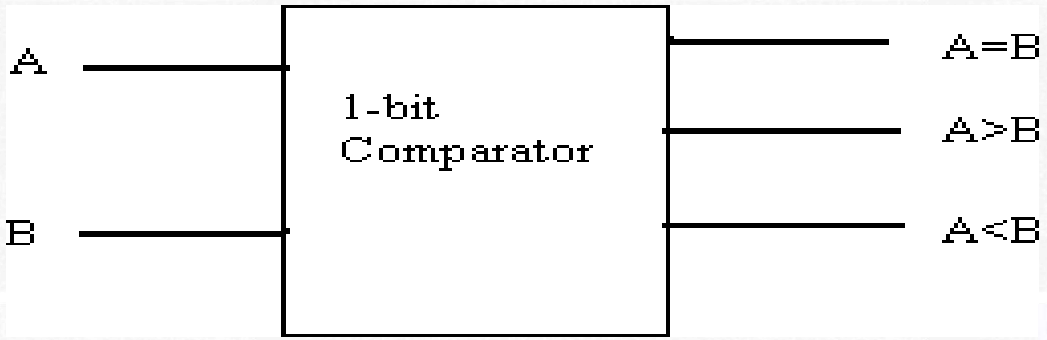
$=B_{in}.\ (X\odot Y)+ X'Y$

$B_{in}.(X\oplus Y)'+ X'Y$



COMPARATORS

- 1-bit Comparator



A	B	A=B	A>B	A<B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

Operation:
A Comparator Compares the two inputs given and tells whether they are equal, one is greater than the other or one is less than the other. Only one output is high for a given input condition of A & B.

OUTPUT EXPRESSION

(A=B)=A'B'+AB

=AʘB=(A⊕B)'

=(A'B+AB')'

(A<B)=A'B

(A>B)=AB'

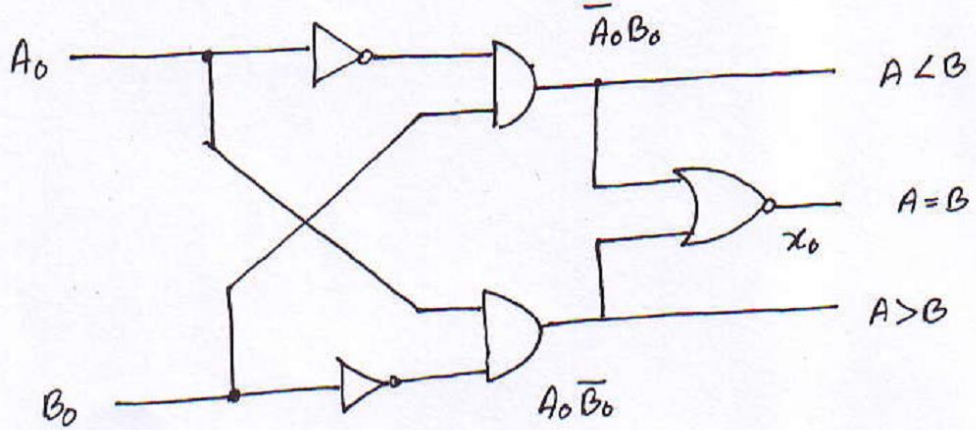
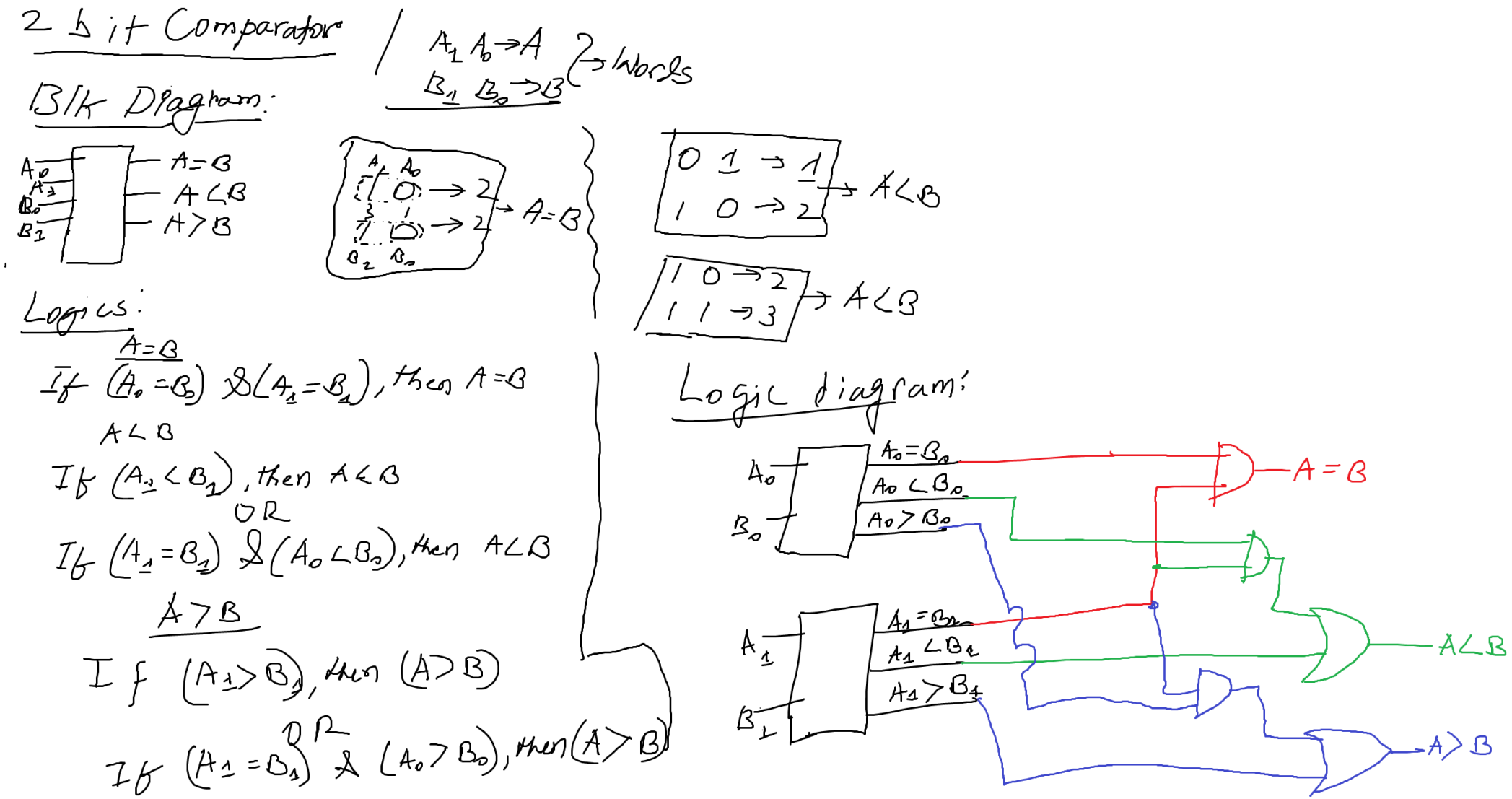


Fig : 1-bit magnitude comparator

2-bit Comparator



THANK YOU FOR YOUR ATTENTION