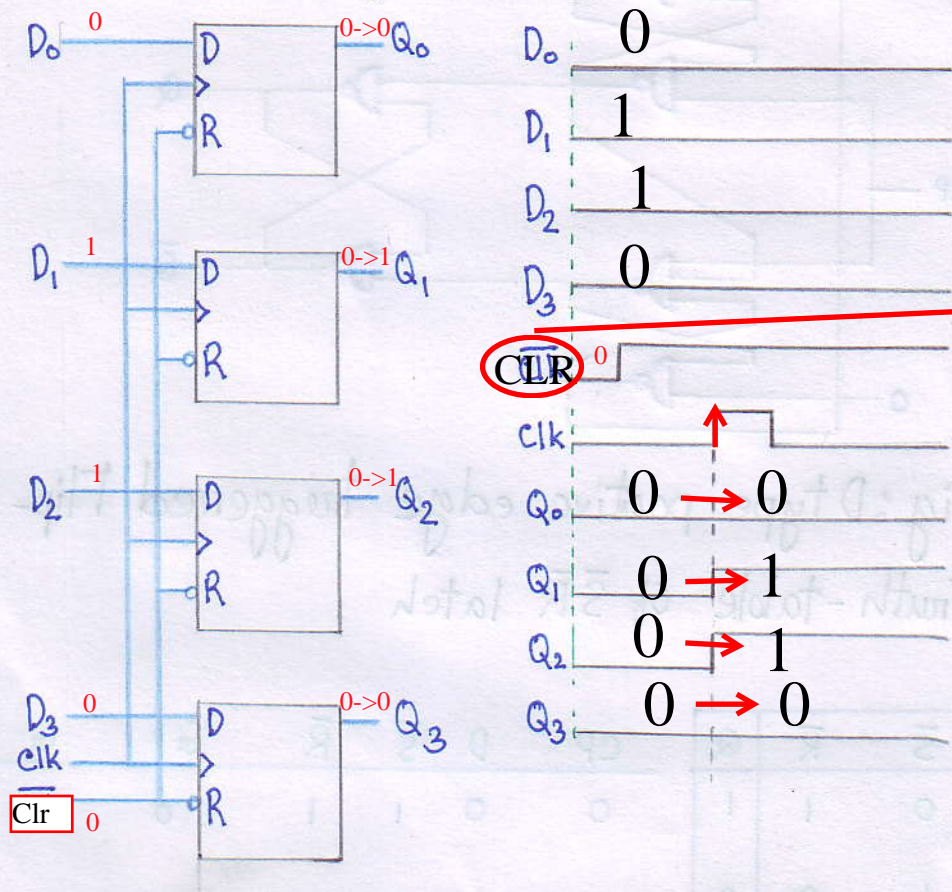


Lecture -16

Flip-Flop application:

Parallel Data Storage

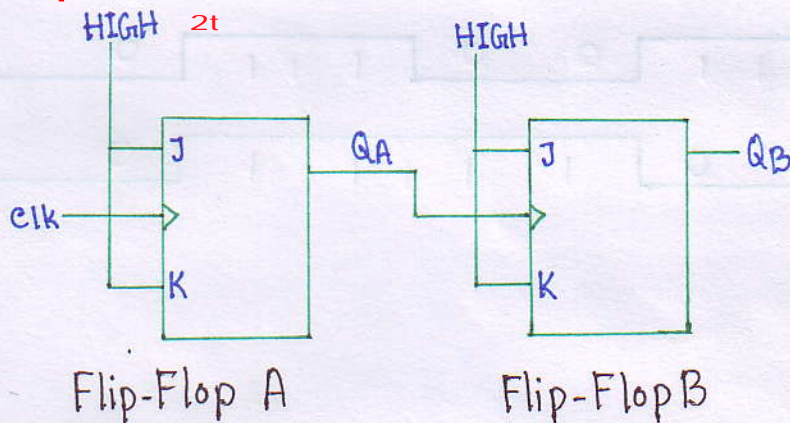
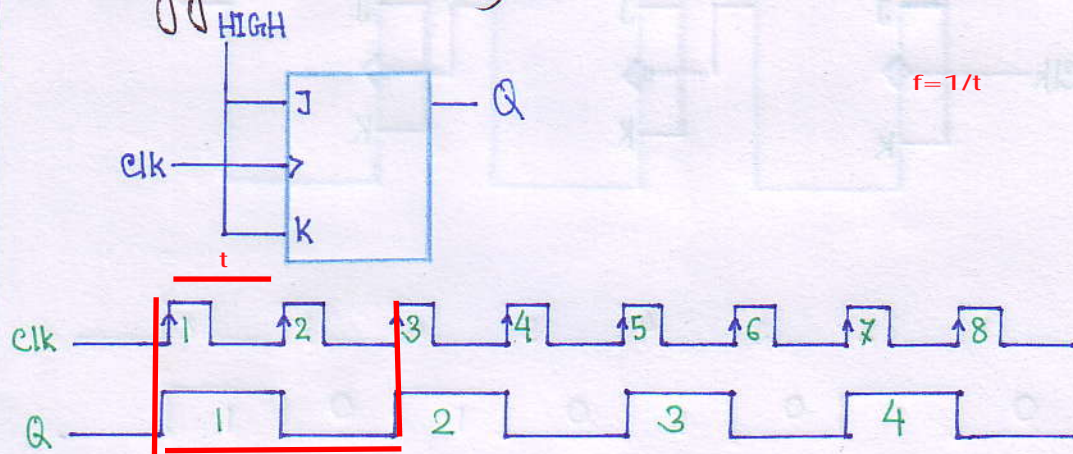


Initially, the CLR is made low so that all the flip-flops clear their output and store only a 0 at the output.

Fig: Flip-Flops used for parallel data storage

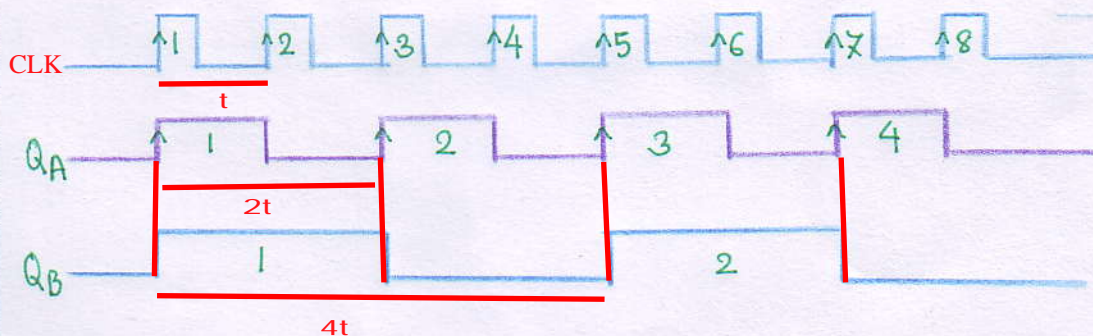
Frequency Division:

A J-K Flip-Flop can be used to divide the frequency of a clock by 2 when connected to toggle ($J=K=1$)



Flip-Flop A will toggle at the positive edge of CLK

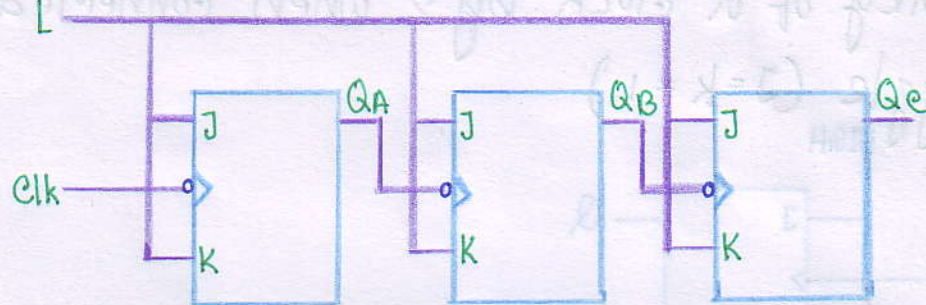
Flip-flop B will toggle at the positive edge of QA



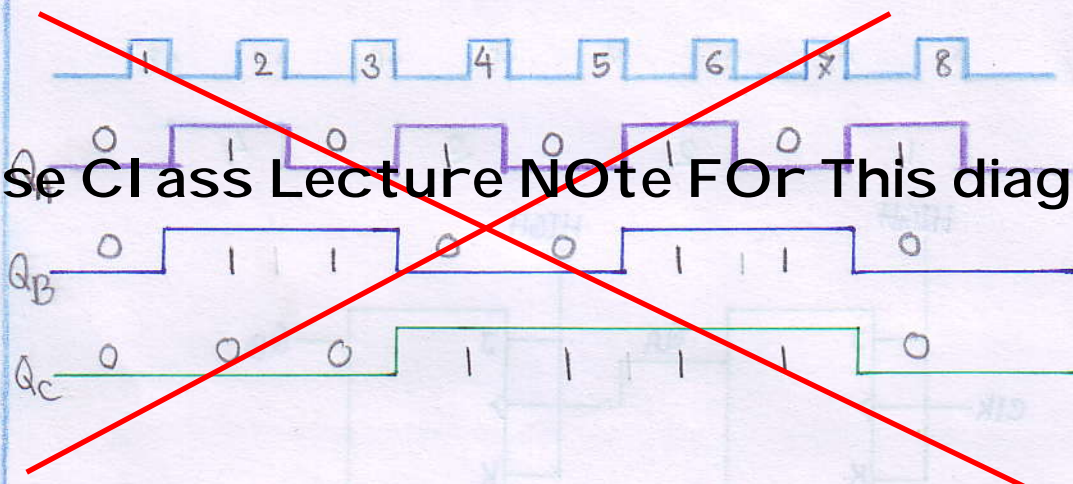
time period of QB = 2 times of time period of QA and = 4 times of time period of CLK

time period of QA = 2 times of time period of CLK

$$f = 1/t$$

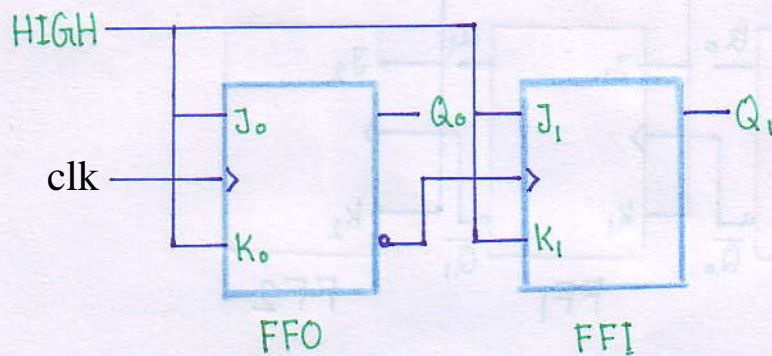


Use Class Lecture Note FOR This diagram



A synchronous Counter Operation:

A 2-bit Asynchronous Binary Counter



J₀ and K₀ will always toggle at the rising edge of clk

J₁ and K₁ will always toggle at the rising edge of Q₀

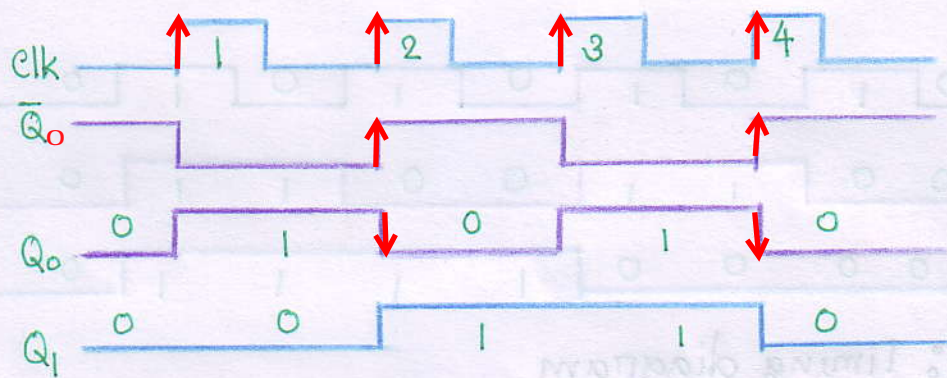
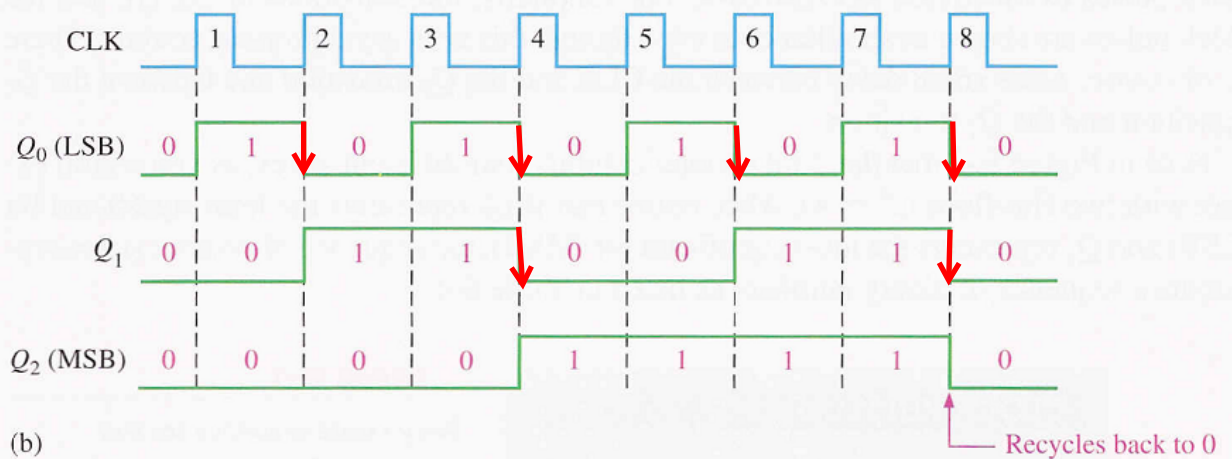
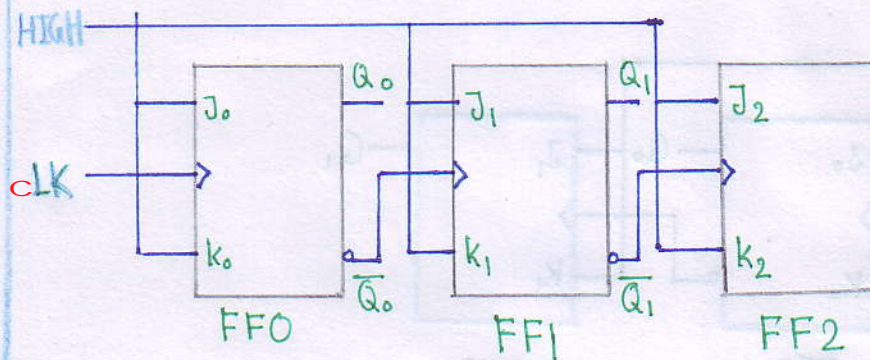


Fig: Timing diagram for the counter

Clock pulse	Q ₁	Q ₀
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0

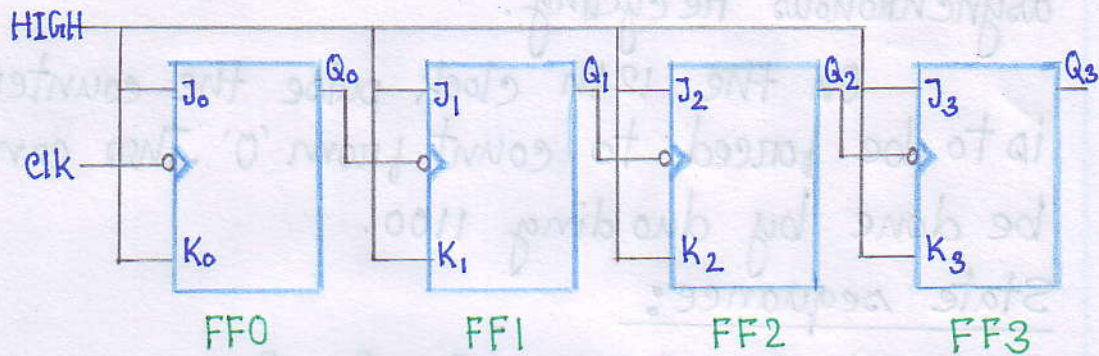
Table state sequence for a 2-stage binary counter.

A 3-Bit Asynchronous Binary counter



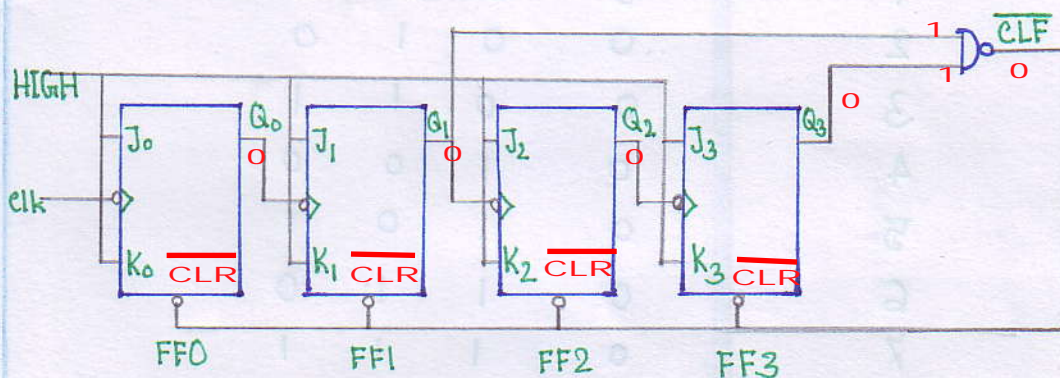
Clock pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

A Four bit Asynchronous binary counter



Asynchronous ^{Decade} counter :

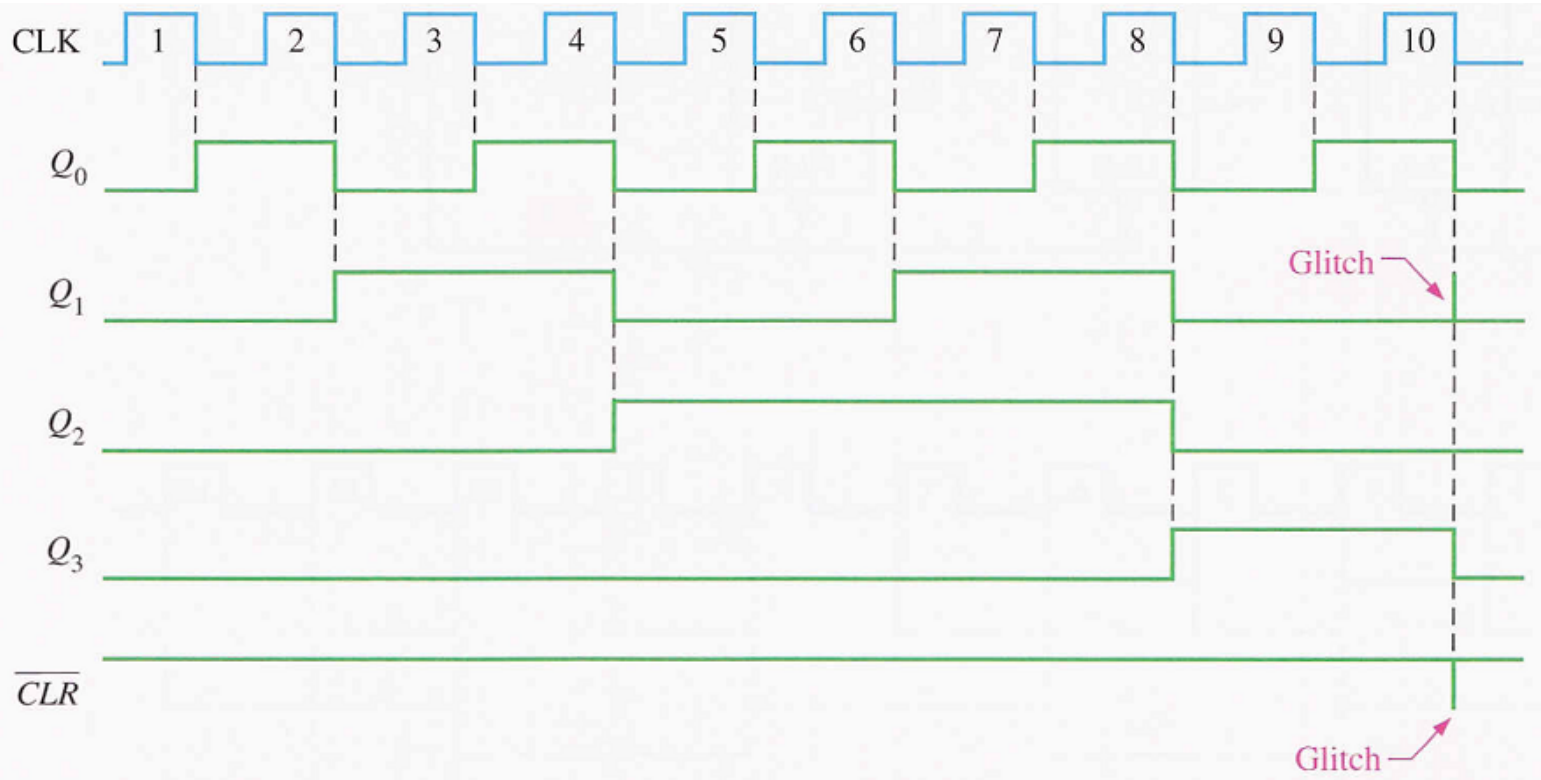
MODULUS-10



State sequence for an asynchronous decade counter :

Clock pulse	Q ₃	Q ₂	Q ₁	Q ₀
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
	0	0	0	0

A decade counter is going to count upto binary value of 0-9. It will recycle at the 10th Clock pulse, and you will only see a slight glimpse of the value 10, after which it will show 0 (that means it will recycle).



(b)