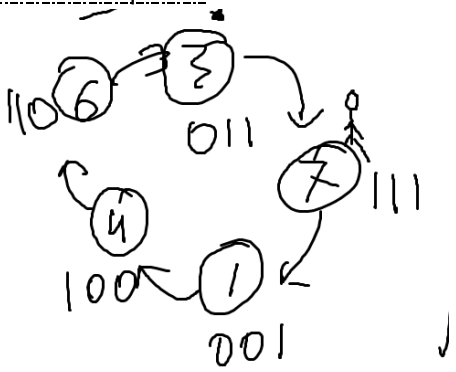
Synchronous Irregular Counters

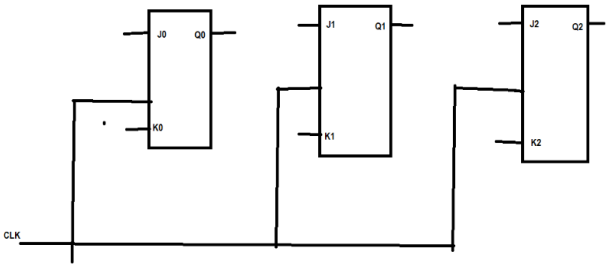
Design a synchronous irregular counter with the following count sequence: 3→7→1→4→6→3

STEP-1: Writing the binary of the given decimal sequence



STEP-2: Identifying the number of flip-flop required.

Here our system has a maximum decimal value of 7, **So the system can be represented with 3 bit output as 7=111, So the outputs of the system will be Q2, Q1 and Q0 and hence we will need 3 flip-flops in synchronous connection.**



STEP-3: Counter Table **(filling the present state and next state values)**

STEP-5: Use transition table on the right to fill up J0, K0, J1, K1, J2, K2 Values

	Present state			Next state								
	Q2	Q1	Q0	Q2	Q1	Q0	J0	K0	J1	K1	J2	K2
3	0	1	1	1	1	1	X	0	X	0	1	X
7	1	1	1	0	0	1	X	0	X	1	X	1
1	0	0	1	1	0	0	X	1	0	X	1	X
4	1	0	0	1	1	0	0	X	1	X	X	0
6	1	1	0	0	1	1	1	X	X	0	X	1

Transition Table:

$Q_P \rightarrow Q_N$	J	K
0 → 0	0	X
0 → 1	1	X
1 → 0	X	1
1 → 1	X	0

STEP-4: Creating Transition Table: (Look at the smaller version on the top right corner)

$Q_P \rightarrow Q_N$	**J**		**K**		**Comment**
0 → 0	0	0	0	X	No Change
	0		1		Reset
0 → 1	1	1	0	X	Set
	1		1		Toggle
1 → 0	0	X	1	1	Reset
	1		1		Toggle
1 → 1	0	X	0	0	No Change
	1		0		Set

STEP-6: Filling up K-MAPs for J0, K0, J1, K1, J2, K2

J0 Map

Q2Q1 \ Q0	0	1
00	X	X
01	X	X
11	1	X
10	0	X

J0=Q1

K1 Map

Q2Q1 \ Q0	0	1
00	X	X
01	X	0
11	0	1
10	X	X

K1=Q2.Q0

K0 Map

Q2Q1 \ Q0	0	1
00	X	1
01	X	0
11	X	0
10	X	X

K0=Q1'

J2 Map

Q2Q1 \ Q0	0	1
00	X	1
01	X	1
11	X	X
10	X	X

J2=1

J1 Map

Q2Q1 \ Q0	0	1
00	X	0
01	X	X
11	X	X
10	1	X

J1=Q0' / Q2

K2 Map

Q2Q1 \ Q0	0	1
00	X	X
01	X	X
11	1	1
10	0	X

K2= Q1

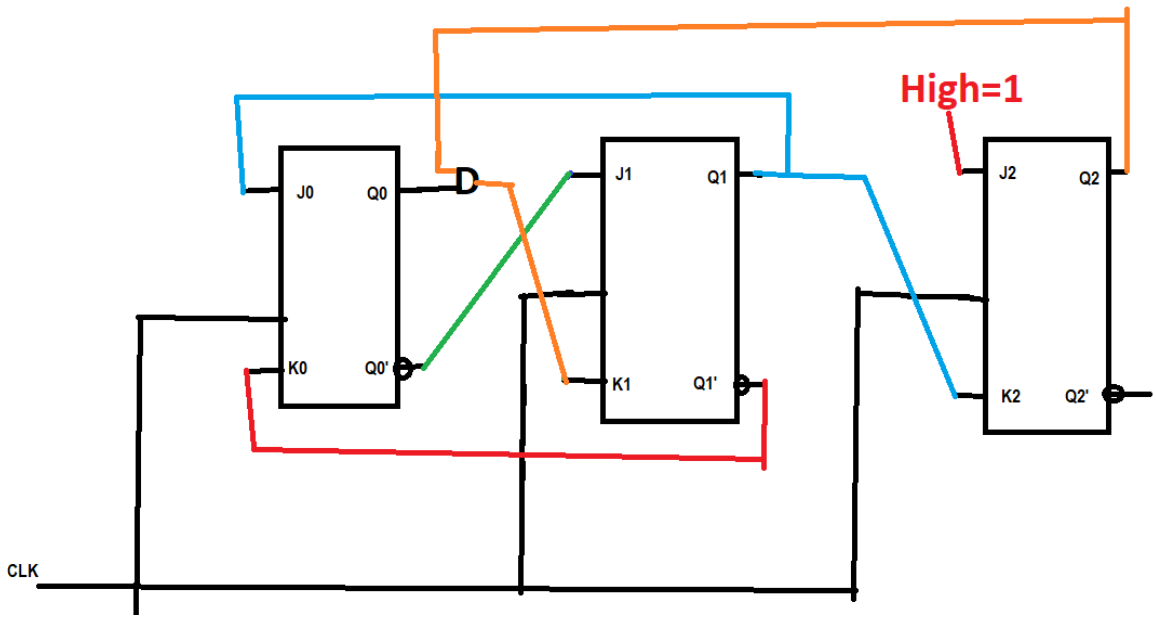
Final Output Connections

J0=Q1, **K0=Q1'**

J1=Q0', **K1=Q2.Q0**

J2=1, **K2=Q1**

STEP-7: Connecting the output connections in the diagram

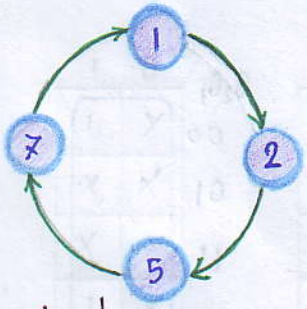


J-K FLIP-FLOP TRUTH TABLE

J	K	Q	COMMENT
0	0	Q_0	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q_0'	Toggle

Counter with Irregular count sequanee

Using J-K Flip-Flop design a counter with count sequanee.



Step1: Flip-Flop required = 3

Step2:

Next state table: All other states are don't care

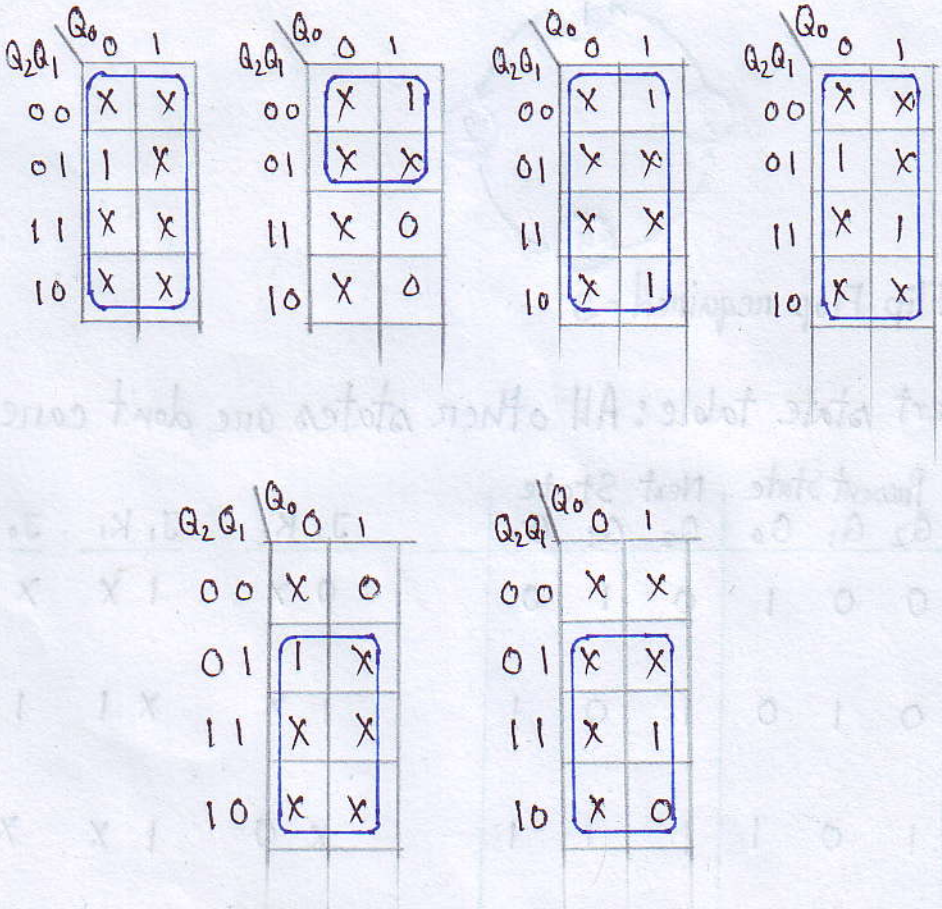
	Present State Q_2 Q_1 Q_0	Next State Q_2 Q_1 Q_0	J_2 K_2	J_1 K_1	J_0 K_0
1	0 0 1	0 1 0	0 X	1 X	X 1
2	0 1 0	1 0 1	1 X	X 1	1 X
5	1 0 1	1 1 1	X 0	1 X	X 0
7	1 1 1	0 0 1	X 1	X 1	X 0

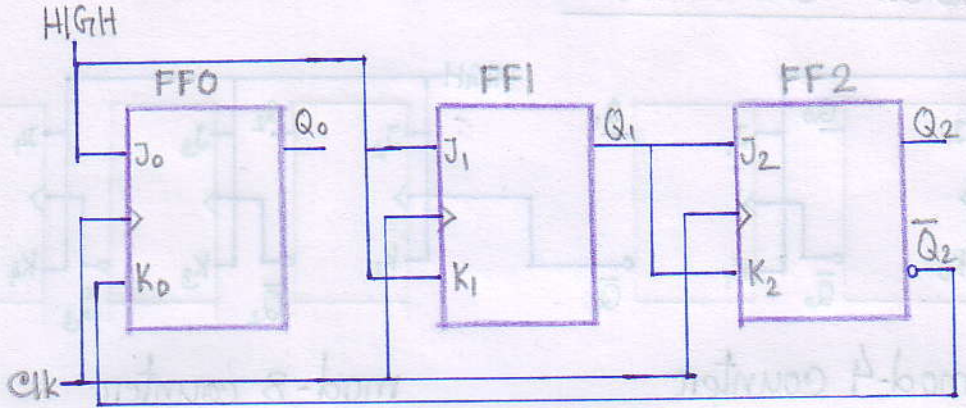
Step 3:

Transition table for J-K Flip-Flop

Output Transitions $Q_N \rightarrow Q_{N+1}$	Flip-Flop inputs J	K
0 → 0	0	X
0 → 1	1	X
1 → 0	X	1
1 → 1	X	0

Step 4:




HIGH
FF0
FF1
FF2
J_0
Q_0
K_0
J_1
Q_1
K_1
J_2
Q_2
$\overline{Q}_2$
K_2
Clk