Lecture-14

LATCHES: The latch is a type of bistable storage DEVICE

The S-R Latch:

Set Reset

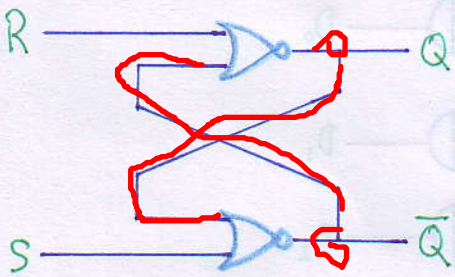


Fig: Active High input S-R Latch

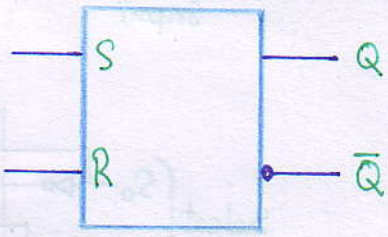


Fig: Logic symbol for Active-High input S-R Latch

Truth table for active-High input S-R Latch

Inputs S	Inputs R	Outputs Q	Outputs $\bar{Q}$	Comments
0	0	NC	NC	No change Latch
0	1	0	1	Latch Reset
1	0	1	0	Latch Set
1	1	0	0	Invalid condition

we will never operate latch in this condition

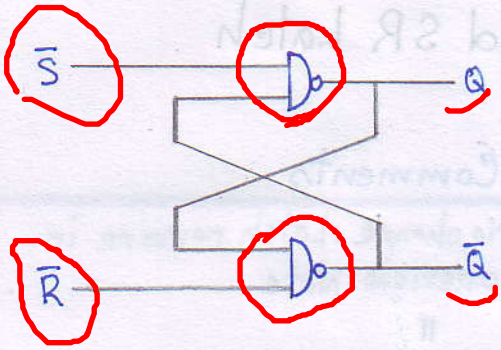


Fig: Active-LOW input $\bar{S}$-$\bar{R}$ latch

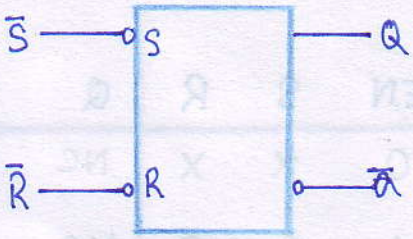
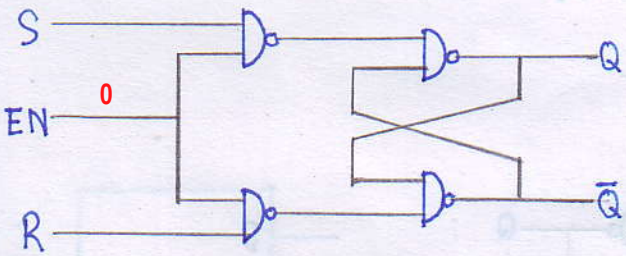


Fig: Logic symbol of $\bar{S}$-$\bar{R}$ latch

Input $\bar{S}$	Input $\bar{R}$	Output Q	Output $\bar{Q}$	Comments
0	0	1	1	Invalid condition
0	1	1	0	Latch Set
1	0	0	1	Latch Reset
1	1	NC	NC	No change. Latch

we will never operate latch in this condition

A Gated SR Latch:



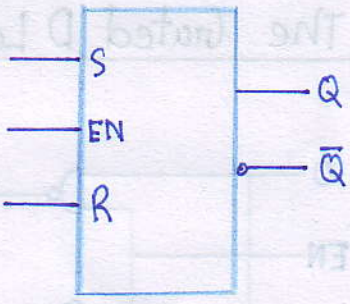
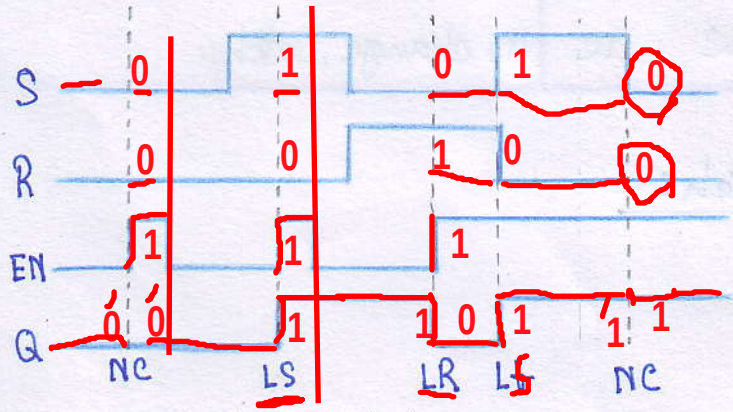


Fig: Logic diagram

Truth table for gated SR Latch

EN	S	R	Q	$\bar{Q}$	Comments
0	X	X	NC	NC	No change. Latch remains in previous state
1	0	0	NC	NC	"
1	0	1	0	1	Latch Reset
1	1	0	1	0	Latch Set
1	1	1	1	1	Invalid condition (Device is not operated in this condition)

Determine Q if the gated S-R Latch is initially RESET.



The Gated D Latch

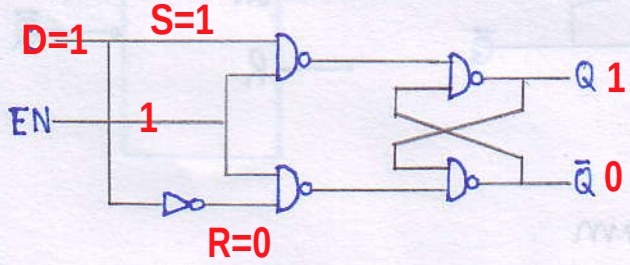


Fig: Logic diagram

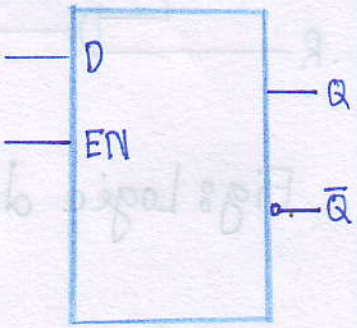
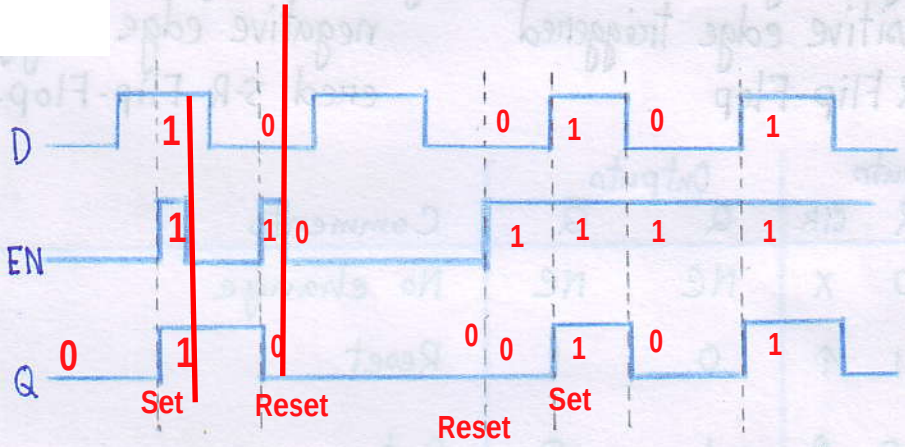


Fig: Logic symbol

Truth table for D Latch

Inputs		Outputs		Comments
EN	D	Q	$\bar{Q}$	
0	X	NC	NC	No Change
1	1	1	0	SET
1	0	0	1	RESET



The gated latches control the flow of information from the input to the output, based upon the level of the enable pin (EN). If the EN=0, the output of the device does not change. If EN=1, the output changes based upon the values from truthtable.

Determine Q if the D-Latch is initially Reset.

EDGE-TRLGGERED FLIR-FLORS

A flip-flops is a synchronous bistable An edge-triggered flip-flops changes state either at the positive edge (rising edge) on at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock.

The Edge-Triggered S-R Flip-Flops:

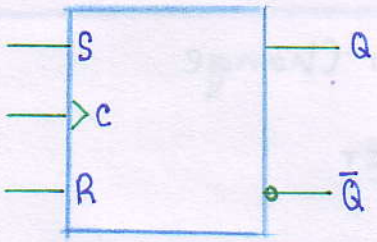


Fig: Logic symbol of positive edge triggered S-R Flip-Flop

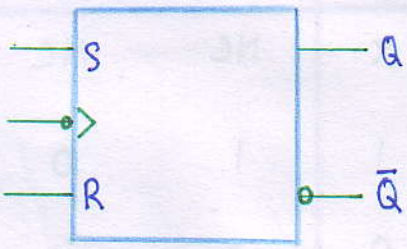
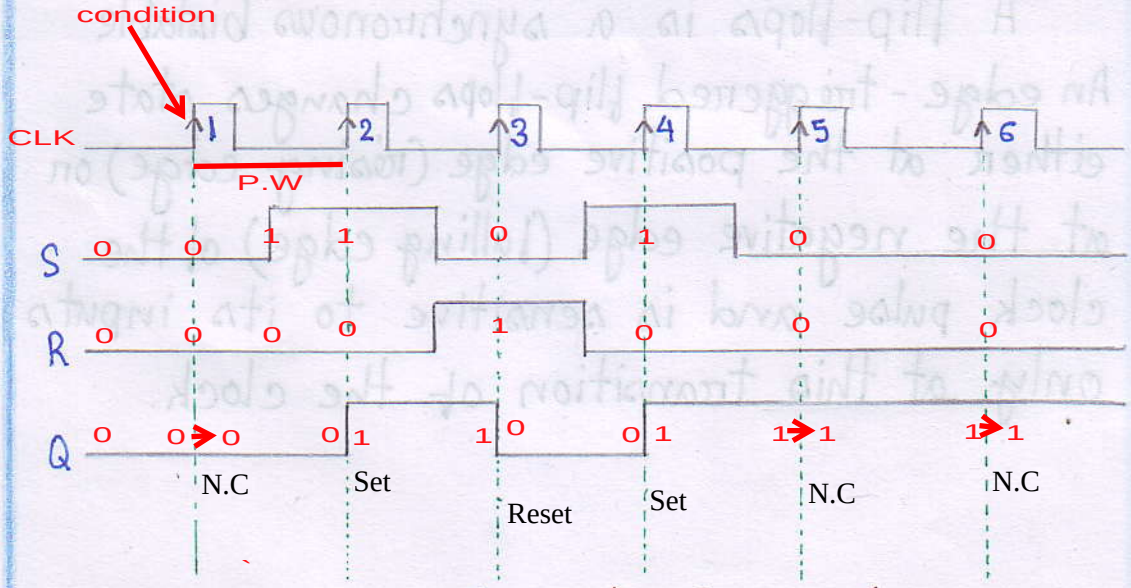


Fig: Logic symbol of negative edge triggered S-R Flip-Flop.

Inputs			Outputs		
S	R	Clk	Q	$\bar{Q}$	Comments
0	0	X	NC	NC	No change
0	1	↑	0	1	Reset
1	0	↑	1	0	Set
1	1	↑	?	?	Invalid

The rising edge of the clock is when the clock signal is going from low to high condition



Positive edge triggered

Determine Q if the n Flip-Flop is initially at Reset state

A method of Edge-Triggering

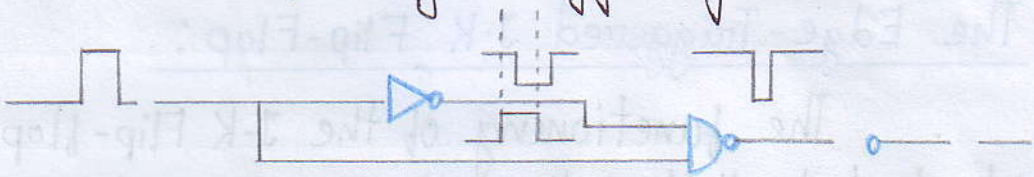
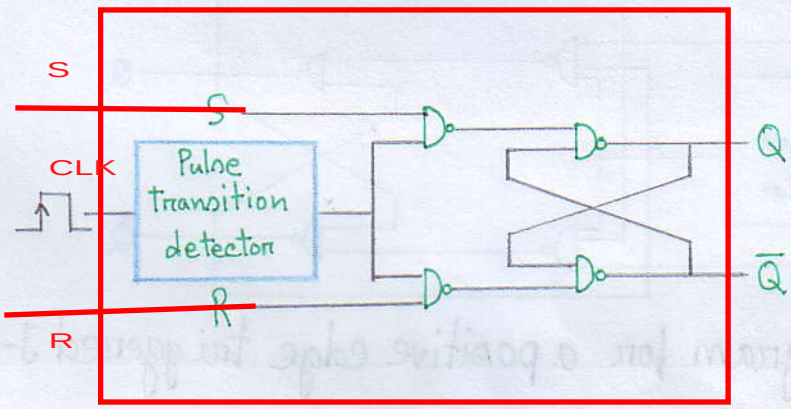


Fig: Pulse transition detector

The job of the pulse transition detector is to convert the level sensitivity of the EN pin of a gated S-R latch to edge sensitivity and convert the system to a S-R Flip-flop



S-R Flip-Flop