Lecture – 15

The Edge-Triggered J-K Flip-Flop:

The functioning of the J-K Flip-flop is idential to that of the S-R flip-flop in the SET, RESET and NO change conditions of operation. The different is that the J-K flip-flop has no invalid states as does the S-R Flip-Flop.

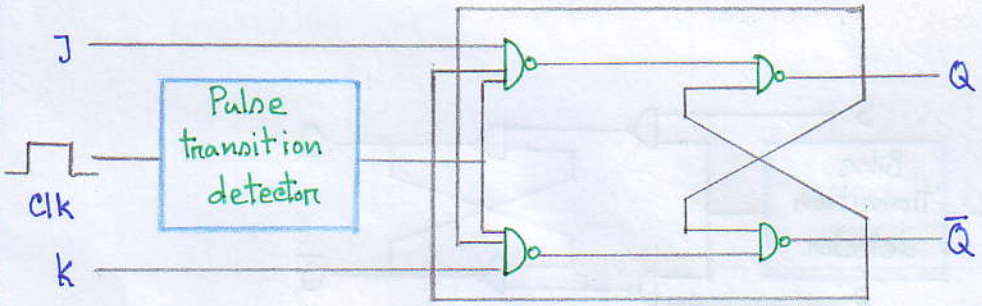
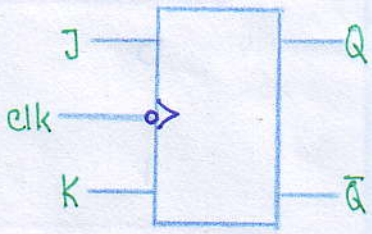
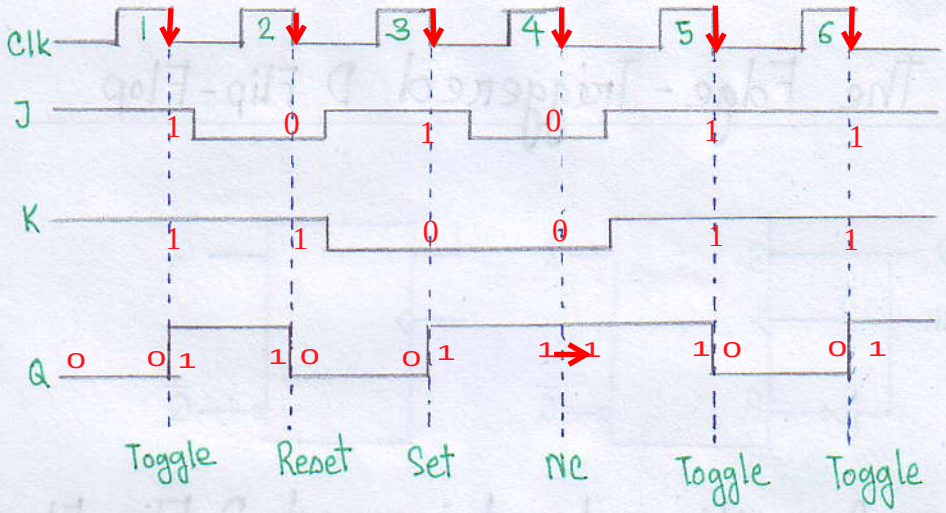


Fig: Logic diagram for a positive edge triggered J-K Flip-Flop.

Inputs			Output		Comments
J	K	Clk	Q	$\bar{Q}$	
0	0	↑	Q_0	$\bar{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	Q_0	Toggle

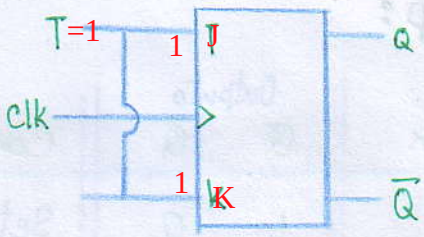
Determine Q output if the J-K Flip-Flop is initially RESET





T Flip-Flop:

A J-K flip-flop connected for toggle operation is sometimes called a T Flip-Flop.



Inputs		Outputs		
T	Clk	Q	$\bar{Q}$	Comments
0	1	Q_0	$\bar{Q}_0$	No change
1	1	$\bar{Q}_0$	Q_0	Toggle mode

The Edge-Triggered D Flip-Flop

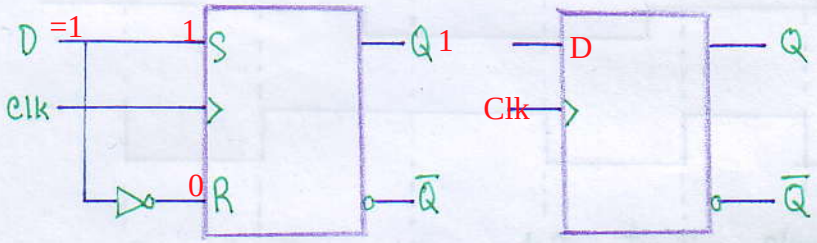


Fig: A positive edge-triggered D Flip-Flop Formed with an S-R Flip-Flop and an inverter.

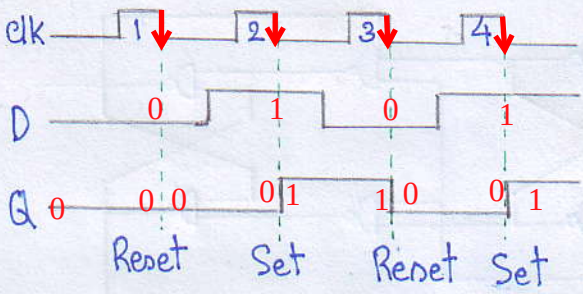
Truth table for positive edge-triggered D Flip-Flop:

Inputs		Outputs		
D	Clk	Q	$\bar{Q}$	Comments
1	↑	1	0	Set
0	↑	0	1	Reset

The D Flip-Flop is used to store a single data bit position edge-triggered Flip-Flop stores data at the leading edge of the clock.

negative edge triggred

Determine Q if the ↑D Flip-Flop is initially ReSet



S-R Flip-flop inputs (S & R)

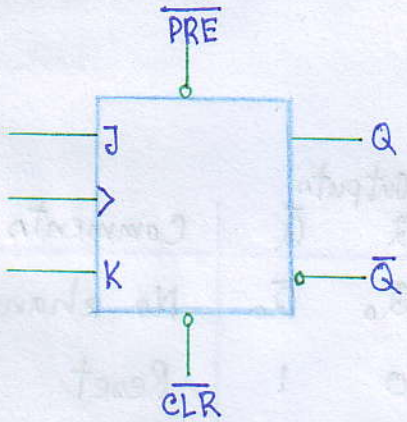
J-K Flip flop inputs (J & K)

T Flip-flop input (T)

D Flip-Flop input (D)

(S & R, J & K, T , D) all of these inputs are known as synchronous inputs

Flip-Flop with Asynchronous Inputs



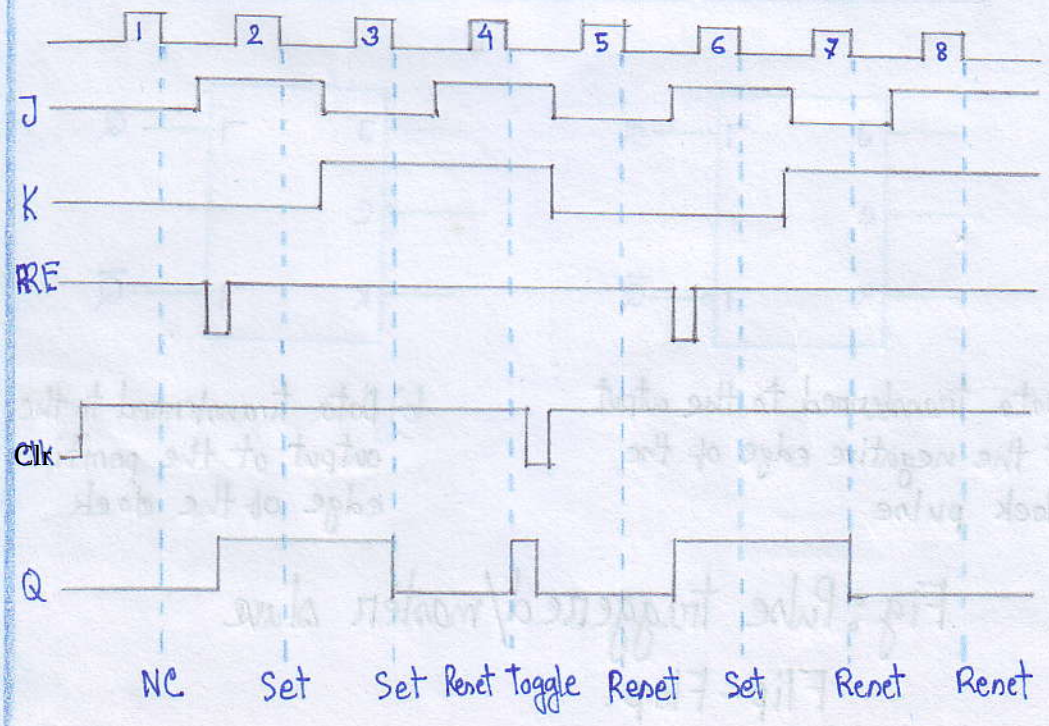
$\overline{PRE}$ and $\overline{CLR}$ are known as asynchronous inputs for flip-flops. They are active low in nature.

$\overline{PRE}$=PRESET=SET Operation, Q=1

$\overline{CLR}$=CLEAR= RESET Operation Q=0

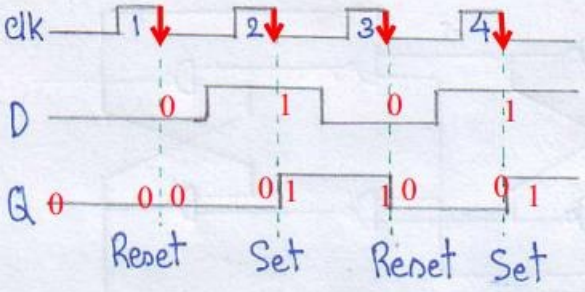
Fig: Logic symbol for a J-K Flip-Flop with active Low preset & clear inputs.

* Determine Q for the following inputs.



negative edge triggred

Determine Q if the ↑D Flip-Flop is initially ReSet



S-R Flip-flop inputs (S & R)

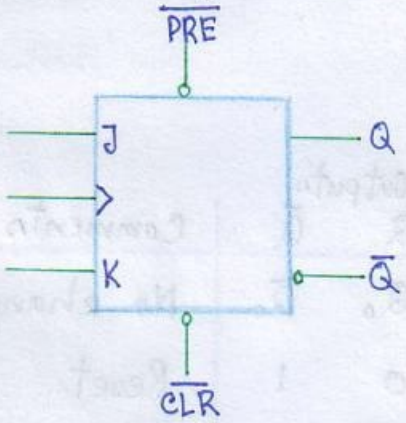
J-K Flip flop inputs (J & K)

T Flip-flop input (T)

D Flip-Flop input (D)

(S & R, J & K, T , D) all of these inputs are known as synchronous inputs

Flip-Flop with Asynchronous Inputs



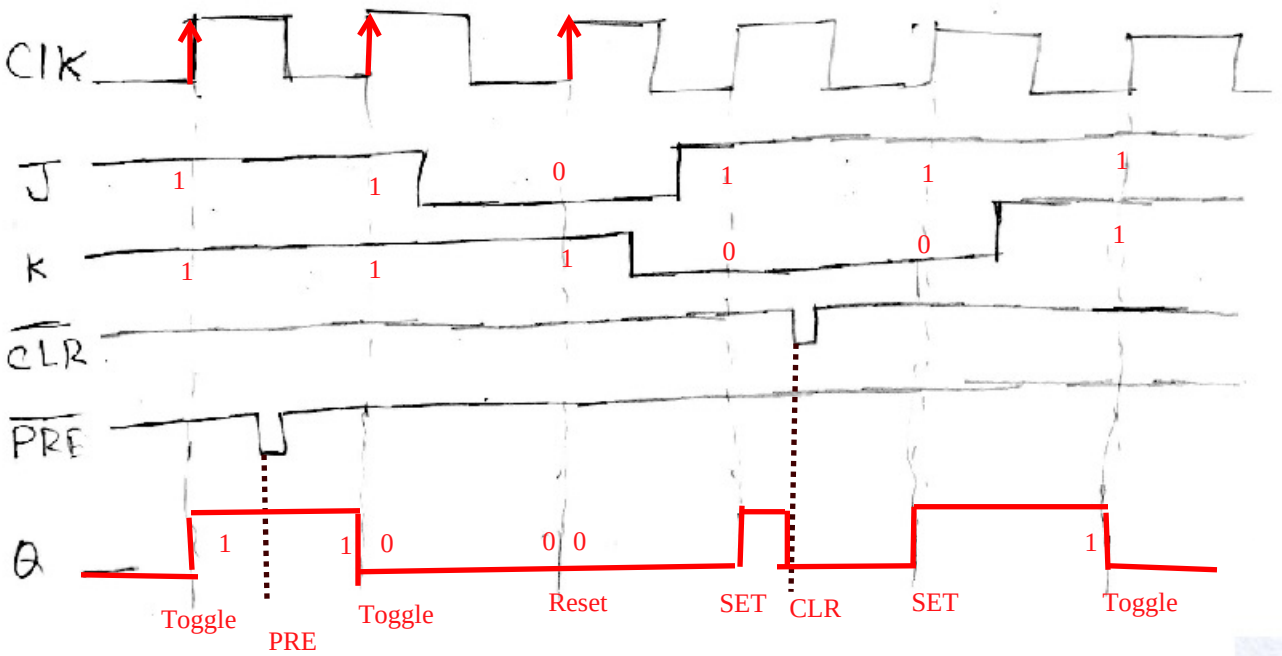
PRE and CLR are known as asynchronous inputs for flip-flops. They are active low in nature.

PRE=PRESET=SET Operation, Q=1

CLR=CLEAR= RESET Operation Q=0

Fig: Logic symbol for a J-K Flip-Flop with active

Determine the output Q for the positive edge triggered J-K flip-flop, if it is initially at reset condition. Here the PRE and CLR are asynchronous active low preset and clear operation respectively.



MASTER SLAVE FLIP-FLOPS

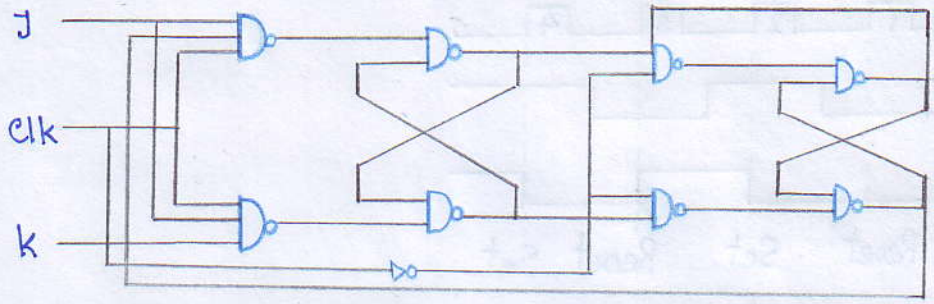
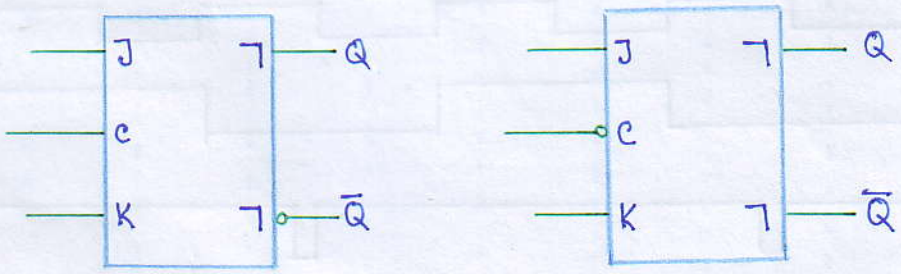


Fig: Logic diagram for a master slave J-k Flip-Flop.

Truth table:

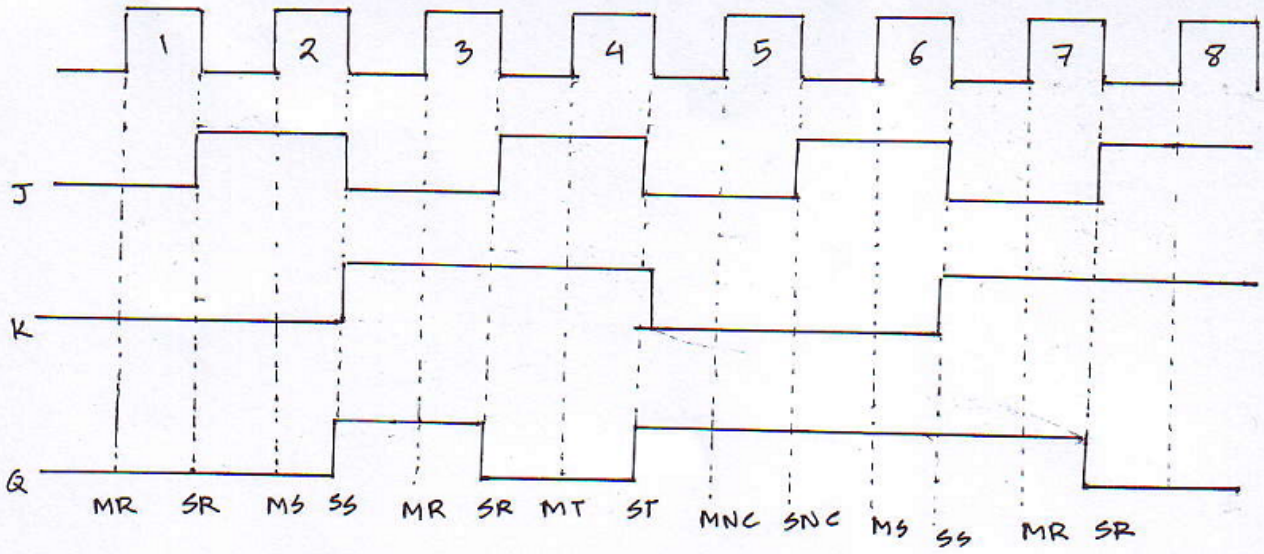
Inputs			Outputs		Comments
J	k	clk	Q	$\bar{Q}$	
0	0	⊓	Q_0	$\bar{Q}_0$	No change
0	1	⊓	0	1	Reset
1	0	⊓	1	0	Set
1	1	⊓	$\bar{Q}_0$	Q_0	Toggle



a) Data transferred to the output at the negative edge of the clock pulse

b) Data transferred to the output at the positive edge of the clock

Fig: Pulse triggered/master slave Flip-Flop.



Determine Q if the flip-flop is initially RESET

D type edge triggered Flip-Flop without pulse transition detector.

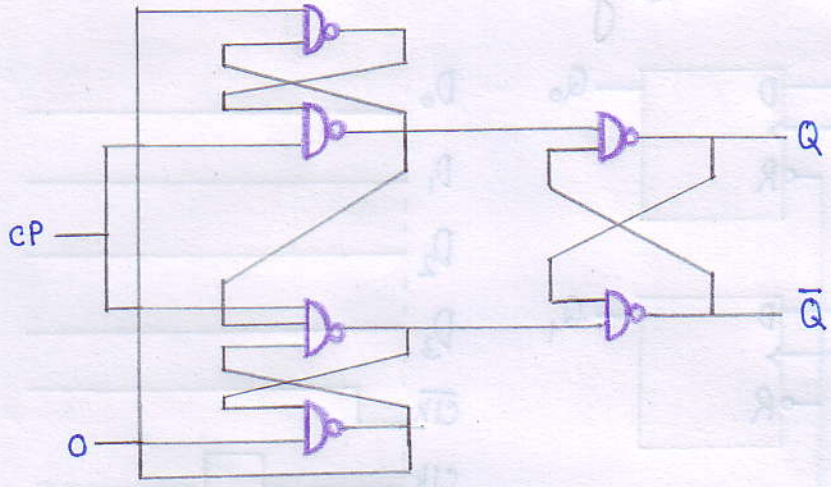


Fig: D type positive edge triggered Flip-Flop

Truth-table of $\bar{S}\bar{R}$ latch

$\bar{S}$	$\bar{R}$	Q
0	1	1
1	0	0
0	0	Invalid
1	1	No

CP	D	$\bar{S}$	$\bar{R}$	G1	G
0	0	1	1	0	1
1	0→1	1	0	0	1
0	1	1	1	1	0
1	1→0	0	1	1	0