Lecture-17

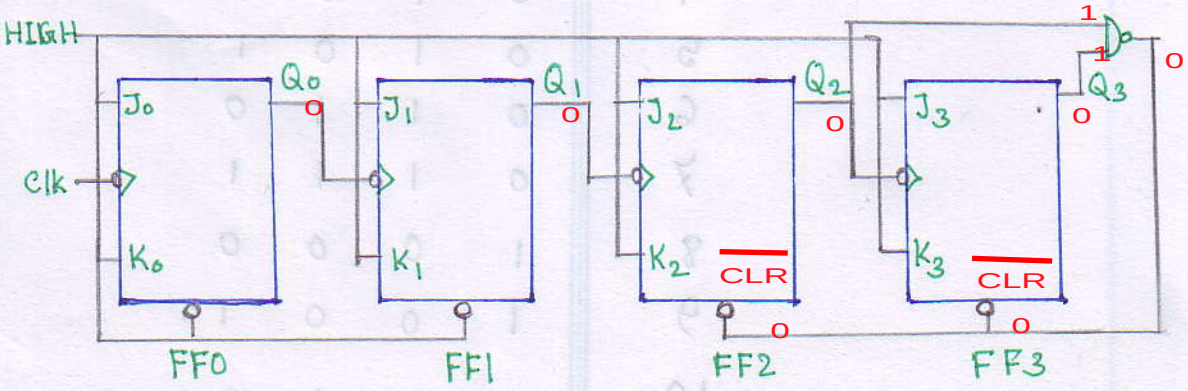
Asynchronous clocked Modulus-12 counter with asynchronous recycling.

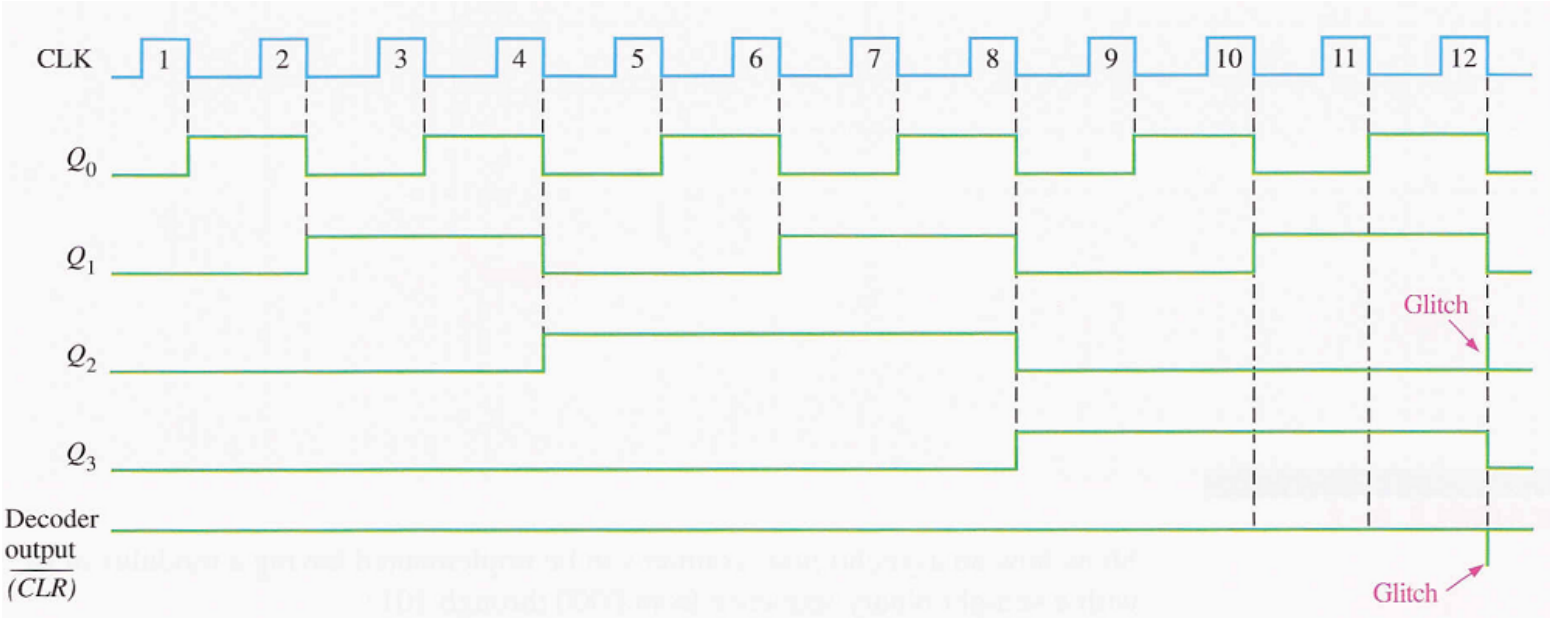
On the 12th clock pulse the counter is to be forced to count from '0'. This can be done by duoding 1100.

State sequanee:

Clock pine	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12(recycles)	01	01	0	0

A Modulus-12 counter is going to count upto binary value of 0-11. It will recycle at the 12th Clock pulse, and you will only see a slight glimpse of the value 12, after which it will show 0 (that means it will recycle).

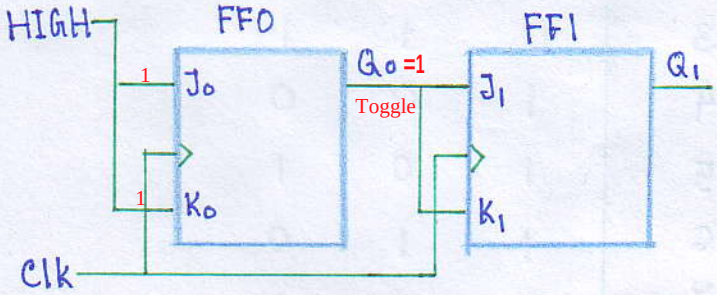



CLK
1
2
3
4
5
6
7
8
9
10
11
12
Q_0
Q_1
Q_2
Q_3
Glitch
Decoder output
$\overline{(CLR)}$
Glitch

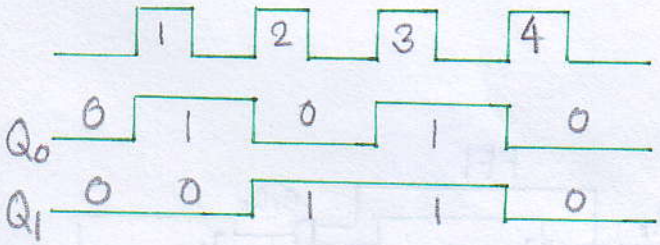
Synchronous Counter:

The Flip-Flops use this synchronous counter are all clocked at the same time by a common clock pulse.

A 2-bit synchronous Binary counter:



Timing diagram



State sequance

Clock pulse	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0

Q0 is toggling at every clock cycle

Q1 will only toggle if Q0=1

J0=K0=High

J1=K1=Q0

A 3-bit Synchronous Binary counter:

State sequance:

Clock pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8(recycles)	0	0	0

Q0 is toggling at every clock pulse

Q1 is toggling when and only Q0=1

Q2 is only toggling if Q1 and Q0 both =1

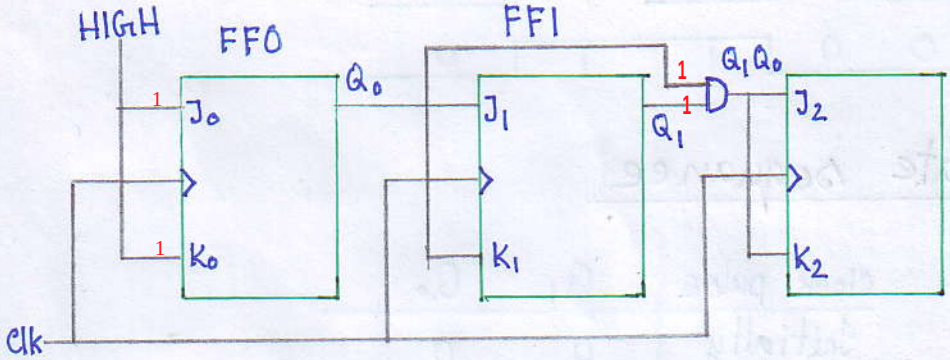


Fig: 3-bit synchronous binary counter

$J_1 = K_1 = Q_0$

JO=KO=High

$J_2 = K_2 = Q_1Q_0$

A 4-bit Synchronous Binary Counter:

State sequance:

Clock Pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16 (recycles)	0	0	0	0

Q0 is toggling at every clock pulse
So J0=K0=1/High

Q1 is toggling when Q0=1
So J1=K1=Q0

Q2 is toggling when Q1=0 AND Q0=0
So J2=K2=Q1.Q0

Q3 is toggling when Q2=1 AND Q1=1 AND Q0=1
So J3=K3=Q2.Q1.Q0

$J_1 = K_1 = Q_0$

J0=K0=1/High

$J_2 = K_2 = Q_1 Q_0$

$J_3 = K_3 = Q_2 Q_1 Q_0$

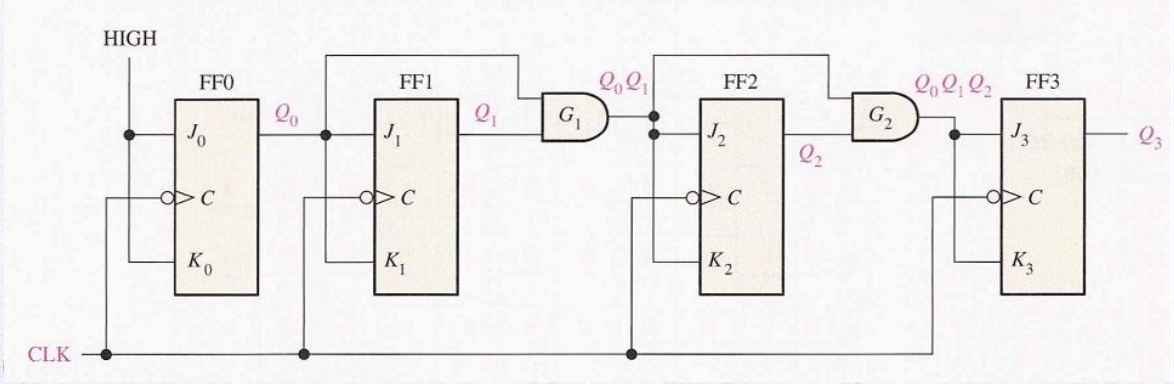


Fig: Synchronous 4-bit Binary counter

Synchronous Decode counter:

State sequance:

Clock Pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10 (recycles)	D	0	D	0

$J_1 = K_1 = Q_0 \bar{Q}_3$

$J_2 = K_2 = Q_1 Q_0$

$J_3 = K_3 = Q_2 Q_1 Q_0 + Q_3 Q_0$

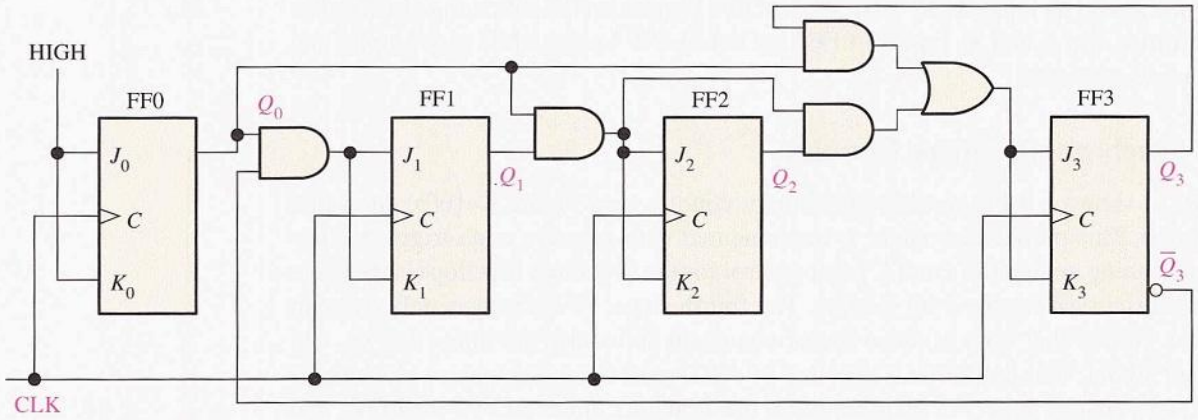


Fig: A Synchronous BCD decade counter

Modulus-12 Synchronous counter

State sequance:

Clock Pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	0	0	0	0

$J_0 = K_0 = 1$

$J_1 = K_1 = Q_0$

$J_2 = K_2 = \overline{Q}_3 Q_1 Q_0$

$J_3 = K_3 = Q_2 Q_1 Q_0 + Q_3 Q_1 Q_0$