American International University- Bangladesh
Faculty of Engineering (EEE)
Electronic Devices Laboratory

Title: Study of JFET and MOSFET Characterization.

Introduction:

The most common transistor types are the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and the Bipolar Junction Transistors (BJT). BJTs based circuits dominated the electronics market in the 1960's and 1970's. Nowadays most electronic circuits, particularly integrated circuits (ICs), are made of MOSFETs. The BJTs are mainly used for specific applications like analog circuits (e.g. amplifiers), high-speed circuits or power electronics.

There are two main differences between BJTs and FETs. The first is that FETs are charge-controlled devices while BJTs are current controlled devices. The second difference is that the input impedance of the FETs is very high while that of BJT is relatively low. As for the FET transistors, there are two main types: the junction field effect transistor (JFET) and the metal oxide semiconductor field effect transistor (MOSFET). The power dissipation of a JFET is high in comparison to MOSFETs. Therefore, JFETs are less important if it comes to the realization of ICs, where transistors are densely packed. The power dissipation of a JFET based circuit would be simply too high. MOSFETs became the most popular field effect device in the 1980's.

The combination of n-type and p-type MOSFETs allow for the realization of the Complementary Metal Oxide Semiconductor (CMOS) technology, which is nowadays the most important technology in electronics. All microprocessors and memory products are based on CMOS technology. The very low power dissipation of CMOS circuits allows for the integration of millions of transistors on a single chip.

The objective of experiment is to become familiar with the characteristics of JFETs and MOSFETs. The goals are:

1. To understand the basic operation of JFETs and MOSFETs and determine the threshold voltage.
2. To measure the I-V characteristics and find the different operating regions for both JFETs and MOSFETs.

Theory and Methodology:

JFETs Structure and Operation

Transistor is a kind of current-control device, and its generating current includes electron flow and hole flow. The transistor is therefore referred to as bipolar junction transistor.
FET is a unipolar device, in which the current of n-channel FET is formed by electron flow and the current of p-channel is formed by hole flow. FET is a kind of voltage-control device. FET can also perform the functions that general transistors (BJT) do, with the only exception that the bias conditions and characteristics are different. Their applications shall thus be chosen in accordance with related advantages and drawbacks. I
The characteristics of FET are listed as follows:

- FET has very high input impedance, typically around 100 MΩ.
- When FET is used as switch, there is no offset voltage.
- FET is relatively independent of radiation, whereas BJT is very sensitive to radiation (β value will be varied).

• Intrinsic noise of FET is lower than BJT, which makes FET suitable for the input stage of low-Ievel amplifier

• During operation the thermal stability of FET is higher than that of BJT.

However, FET also has some drawbacks: comparing with BJT, its product of gain and bandwidth is smaller and it is easier to be damaged by static electricity.

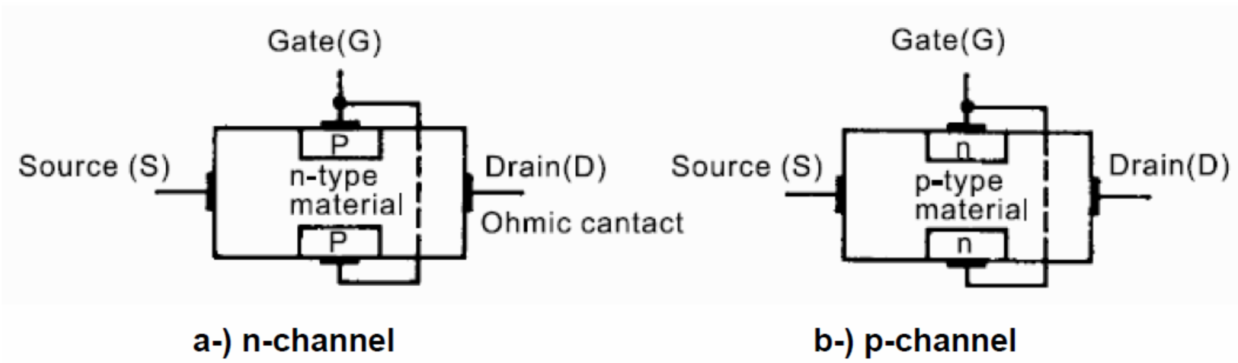

Figure 1: Internal Structure of n-channel and p-channel JFETs

The internal structure of JFETs is shown in figure 1. The n-channel JFET is formed by diffusing one pair of p-type region into a slab of n-type material. On the contrary, the p-channel JFET is formed by diffusing one pair of n-type region into a slab of p-type material.

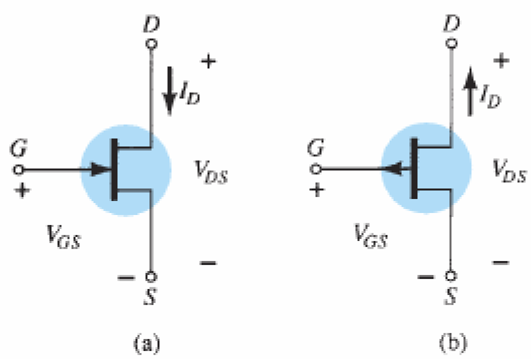

Figure 2: JFET symbols: (a) n-channel (b) p-channel

The p -channel JFET is constructed in the same manner as the n -channel device of but with a reversal of the p - and n -type materials. The defined current directions are reversed, as are the actual polarities for the voltages V_{GS} and V_{DS}. For the p -channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS} on the characteristics of figure 3, which has an I_{DSS} of 6 mA and a pinch off voltage of V_{GS} = +6 V.

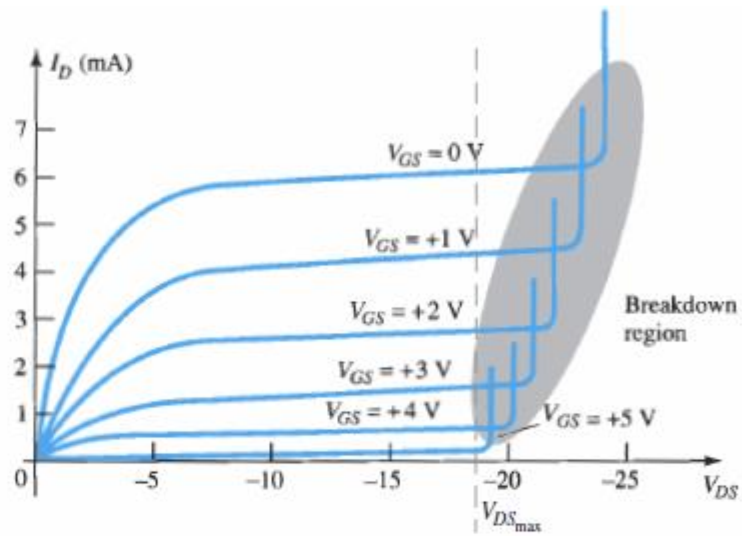

Figure 3: p-channel JFET drain -source characteristics with I_{DSS} = 6 mA and V_P = +6 V

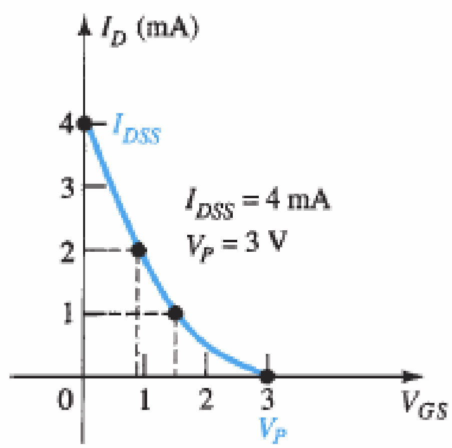

Figure 4: Transfer characteristics of p-channel JFET with I_{DSS} = 4 mA and V_P = +3 V

MOSFETs Structure and Operation

The MOSFETs are the most widely used FETs. Strictly speaking, MOSFET devices belong to the group of Insulated Gate Field Effect Transistor (IGFETs). As the name implies, the gate is insulated from the channel by an insulator. In most of the cases, the insulator is formed by a silicon dioxide (SiO_2), which leads to the term MOSFET. MOSETs like all other IGFETs has three terminals, which are called Gate (G), Source (S), and Drain (D). In certain cases, the transistors have a fourth terminal, which is called the bulk or the body terminal. In PMOS, the body terminal is held at the most positive voltage in the circuit and in NMOS, it is held at the most negative voltage in the circuit.

There are four types of MOSFETs: enhancement n-type MOSFET, enhancement p-type MOSFET, depletion n-type MOSFET, and depletion p-type MOSFET. The type depends whether the channel between the drain and source is an induced channel or the channel is physically implemented and whether the current owing in the channel is an electron current or a hole current. If the channel between the drain and the source is an induced channel, the transistor is called enhancement transistor. If the channel between the drain and source is physically implemented, then the transistor is called depletion transistor. If the current owing in the channel is an electron current, the transistor is called an n- type or NMOS transistor. If the current flow is a hole current, then the transistor is called p-type or PMOS transistor. Throughout the handout, we will concentrate on analyzing the enhancement type MOSFET. The cross section of an enhancement NMOS transistor is shown in figure 5. If we put the drain and source on ground potential and apply a positive voltage to the gate, the free holes (positive charges) are repelled

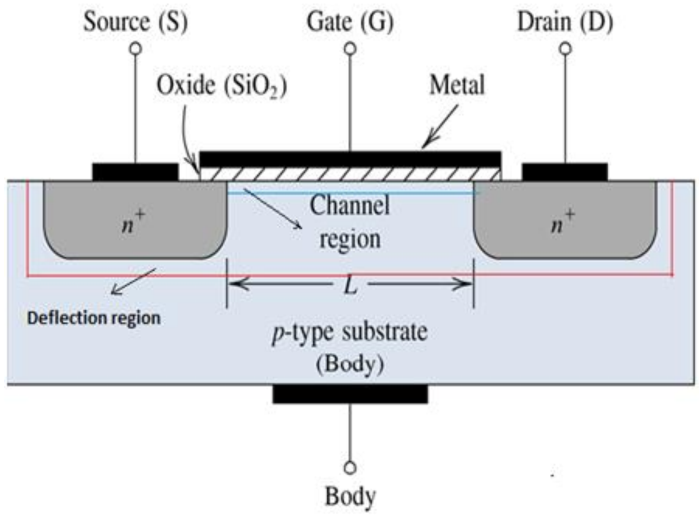

Figure 5: Schematic cross section of an enhancement-type NMOS transistor

from the region of the substrate under the gate (channel region) due to the positive voltage applied to the gate. The holes are pushed away downwards into the substrate leaving behind a depletion region. At the same time, the positive gate voltage attracts electrons into the channel region. When the concentration of electrons near the surface of the substrate under the gate is higher than the concentration of holes, an n region is created, connecting the source and the drain regions.

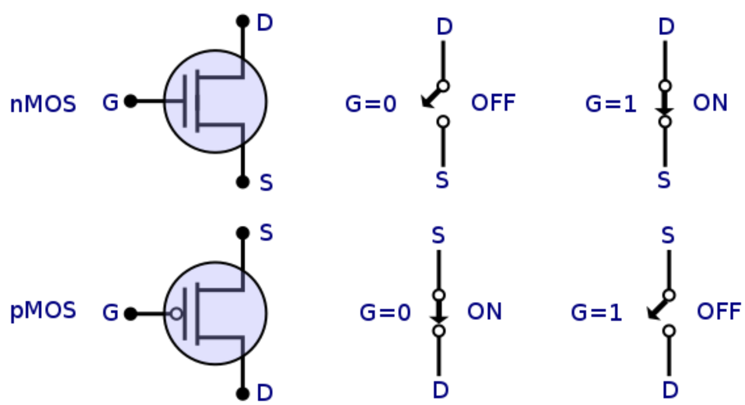

Figure 6: Symbols for Enhancement NMOS and PMOS transistors

The induced n-region thus forms the channel for current flow from drain to source. The channel is only a few nanometers wide. Nevertheless, the entire current transport occurs in this thin channel between drain and source. Now if a voltage is applied between drain and source electrodes an electron current can flow through the induced channel. Increasing the voltage applied to the gate above a certain threshold voltage enhances the channel. In the case of an enhancement type NMOS transistor the threshold voltage is positive, whereas an enhancement type PMOS transistor has a negative threshold voltage. So, in order for the current to flow from drain to source, the condition that should be satisfied is $V_G > V_{th}$, where V_G is the gate voltage and V_{th} is the minimum voltage required to form a channel between drain and source so that carriers can ow through the channel. By changing the applied gate voltage, we can modulate the conductance of the channel.

Depletion type MOSFETs use a different approach. The channel is already conductive for gate voltages of 0V. Such kinds of MOS transistors are realized by the physical implantation of an n-type region between the drain and the source.

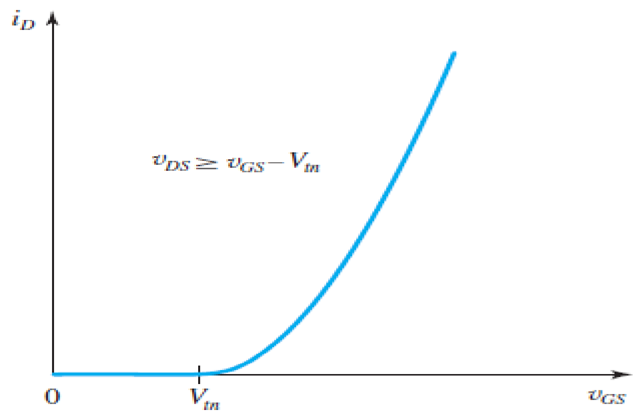

Figure 7: Drain current I_D vs gate to source voltage V_{GS} graph of an enhancement type NMOS showing threshold voltage V_{tn}

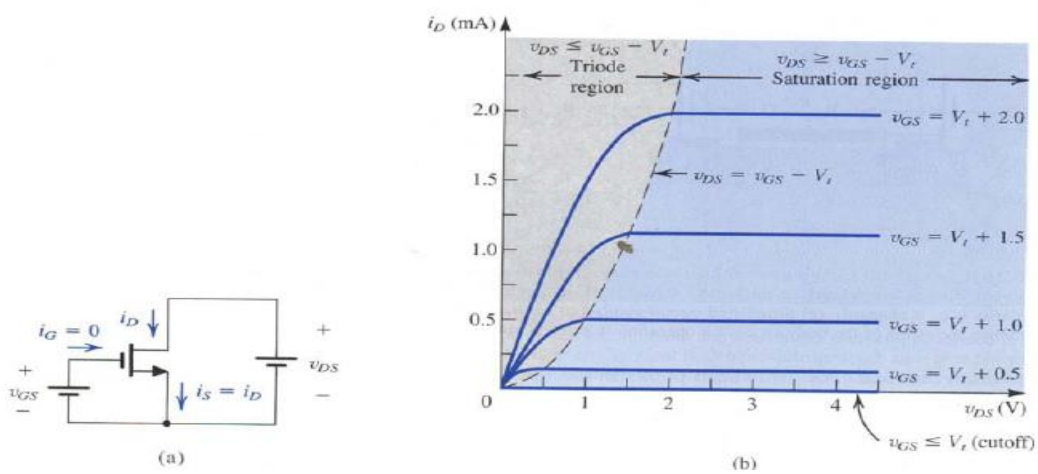

Figure 8: (a) an n-channel enhancement type MOSFET with v_{GS} and v_{DS} applied (b) the $i_D - v_{DS}$ characteristics of a device with $k'_n(W/L) = 1$ mA/V^2 showing the three operating region

Pre-Lab Homework:

1. Draw and explain the transfer characteristics and output characteristics of n-channel and p-channel JFETs. Define pinch-off voltage.

2. Explain the differences between an enhancement and depletion type MOSFET.

3. Explain the differences between an NMOS and PMOS transistor.

4. Draw and explain the transfer characteristics and output characteristics of n-channel and p-channel enhancement type MOSFETs. Define threshold voltage.

Students must install PSpice software and MUST present the simulation results using transistors to the instructor before the start of the experiment.

Apparatus:

(1) Multimeter
(2) J 176 (p-channel JFET)
(3) 2N7000 (n-channel enhancement type MOSFET)
(4) Connecting wires.
(5) Trainer Board

Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within V_{DD}) to turn on the transistors and/or chip, otherwise it may get damaged.

MOSFET transistors are very susceptible to breakdown due to electrostatic discharge. It is recommended that you always ground yourself before picking up the MOSFET chip. Do not touch any of the pins of the chip.

Experimental Procedure:

Transfer Characteristics of P-channel JFET(J 176)

1. Connect the circuit as shown in figure 9. Keep V_S = 10 V constant.
2. Use 1 kΩ resistor as load.
3. Now vary gate voltage V_G from 10 to 20 V in steps of 1 V and measure corresponding current through the resistor (I_D).
4. Complete table 1.
5. Now plot I_D vs V_{GS} curve using the data of table 1 and measure pinch-off voltage V_P.

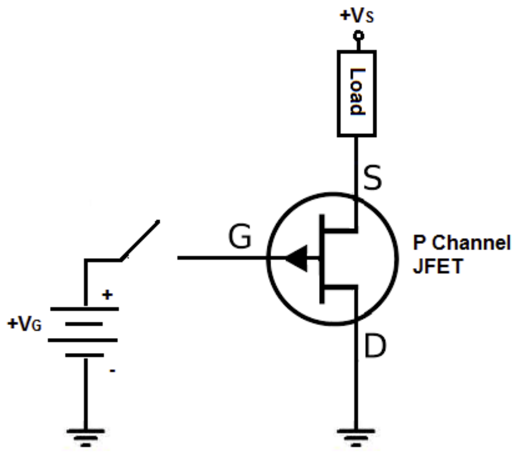

Figure 9: Circuit for plotting I_D vs V_D and transfer characteristics of p-channel JFET (J176)

I_D vs V_{DS} Characteristics of P-channel JFET(J 176)

1. Connect the circuit as shown in figure 9. Keep V_G = 15 V constant.
2. Use 1 kΩ resistor as load.
3. Now vary gate voltage V_s from 0 to 10 V in steps of 1 V and measure corresponding current through the resistor (I_D).
4. Complete table 2.
5. Now plot I_D vs V_{DS} curve using the data of table 2. Indicate the different operating regions.

Transfer Characteristics of n-channel enhancement MOSFET (2N7000)

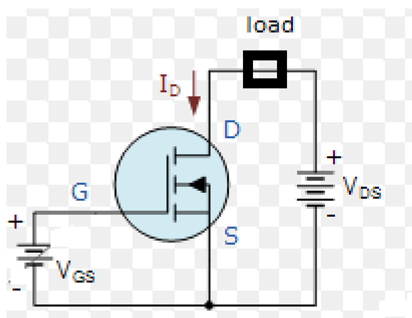

Figure 10: Circuit for plotting I_D vs V_D and transfer characteristics of p-channel JFET (J176)

1. Connect the circuit as shown in figure 10. Keep V_{DS} = 10 V constant.
2. Use 1 kΩ resistor as load.
3. Now vary V_{GS} from 0 to 10 V in steps of 1 V and measure corresponding current through the resistor (I_D).
4. Complete table 3.
5. Now plot I_D vs V_{GS} curve using the data of table 3 and measure threshold voltage V_{th}.

I_D vs V_{DS} Characteristics of n-channel enhancement MOSFET(2N7000)

1. Connect the circuit as shown in figure 10. Keep V_{GS} = 5 V constant.
2. Use 1 kΩ resistor as load.
3. Now vary gate voltage V_{DS} from 0 to 10 V in steps of 1 V and measure corresponding current through the resistor (I_D).
4. Complete table 4.
5. Now plot I_D vs V_{DS} curve using the data of table 4. Indicate the different operating regions.

Data Table:

Table 1

V_G (Volts)	V_{GS} (Volts)	I_D (mA)
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		

Table 2

V_S (Volts)	V_{DS} (Volts)	I_D (mA)
0		
1		
2		
3		
4		
5		
6		
7		
8		
9		

Table 3

V_{GS} (Volts)	I_D (mA)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	

Table 4

V_{DS} (Volts)	I_D (mA)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	

Results and Discussion:

Students will summarize the experiment and discuss it as a whole. Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. Discuss any mistake you might have made while conducting the investigation and describe ways the study could have been improved.

Report:

1. Plot the measured characteristic curves.
2. Indicate the region of operations properly.
3. Compare JFETs and MOSFETs.

References:

1. A.S. Sedra, K.C. Smith, Microelectronic Circuits, Oxford University Press (1998).
2. J. Keown, ORCAD PSpice and Circuit Analysis, Prentice Hall Press (2001).
3. P. Horowitz, W. Hill, The Art of Electronics, Cambridge University Press (1989).
4. David Comer & Donald Comer, "Fundamentals of Electronic Circuit Design".