Trends and patterns of ASIC and FPGA use in European space missions

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This document is a shorter version (simplified for open public release to the space ASIC/FPGA community) of the following Master Thesis:

Trends and patterns in ASIC and FPGA use in space missions and impact in technology roadmaps of the European Space Agency

Master Thesis by Roger Boada Gardenyes (developed and evaluated by T. U. Delft and ESA, 15th August 2012)

ABSTRACT

ASIC (Application-Specific Integrated Circuit) and FPGA (Field-Programmable Gate Array) are the two most complex and versatile integrated circuit technologies used nowadays in space missions. They are key technologies and perform the core of the avionics control and data processing of every satellite and spacecraft. Quantities used of ASIC and FPGA in space missions have been increasing significantly in the last years. Some of the fundamental differences between ASIC and FPGA are the development costs and the reprogrammability features, while in both cases there is a lengthy and costly customer design process behind. This research attempts to quantify the use of ASIC and FPGA technologies in space missions in the last years, to show the patterns and trends of use and to assess how these conclusions match the priorities established in the present technology roadmaps of the European Space Agency. The results of this study will be used as valuable inputs for future strategic and investment decisions of the European Space Agency and the European space community actors.

Keywords: ASIC, FPGA, European Space Agency, space missions, technology roadmaps.

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By R. Boada

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ACRONYMS

AFMS	ASIC, FPGA, Microprocessor and Standard ASIC
ARTES	Advanced Research in Telecommunication Systems
ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
CNES	Centre National d'Études Spatiales
DCL	Declared Component List
DMS	Data Management System
ECI	European Component Initiative
EEE	Electronic, Electrical and Electromechanical
ESCC	European Space Components Coordination
ESA	European Space Agency
FPGA	Field Programmable Gate Array
GEO	Geostationary Earth Orbit
GSTP	General Support Technology Programme
IC	Integrated Circuit
IPC	Industrial Policy Committee
ITAR	International Traffic in Arms Regulation
ITRS	International Technology Roadmap for Semiconductors
LEO	Low Earth Orbit
MEO	Medium Earth Orbit
MTR	Microelectronics Technology Roadmaps
NASA	National Aerospace and Space Administration
NRE	Non-Recurring Engineering
PA	Product Assurance
PF	Platform
PL	Payload
THAG	Technology Harmonisation Advisory Group
TDM	Technical Dossier of Microelectronics
TRP	Technology Research Programme

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1 INTRODUCTION

1.1 Motivation of research

ASIC and FPGA are key technologies in the development of space missions and perform the very hearts of the avionics control and the data processing systems of satellites[1]. They are complex and versatile integrated circuits which can implement large and complex functions. The main difference between these two technologies is that customers can buy “blank” FPGAs off the shelf and program them on their premises, while ASICs are integrated circuits (ICs) manufactured to a customer’s specification[2]. Microprocessors and Standard ASICs are two other classes of complex integrated circuits that perform key control functions which are fundamental for the overall satellite operation.

It is difficult to define if ASIC and FPGA are competing technologies or if each one has its own market. Sometimes it is possible to use both integrated circuits for the same purpose so they compete, but in other cases the ASIC technology is the only one technically feasible due to its higher performance. The choice between both technologies is not only based on technical parameters but also on economic and logistic parameters like time to market, price or the user experience on each technology[1].

According to Paris-based Euroconsult’s 12th World Market Survey, satellite manufacturers are at the beginning of a decade boom. It is expected that in the period to 2018, a 50 per cent more spacecrafts and satellites will be launched to the Earth orbit than in the preceding 10 years.

In addition, more hardware will be used in larger geostationary satellites as telecommunications companies try to pack in more channels and bandwidth[3]. These systems are becoming more complex and this trend will continue into the future so it will be required more complexity in the electronics and this can only be achieved by deploying highly integrated ASICs and FPGAs[4].

At the same time, the trend to use ASIC, FPGA, Microprocessor and Std. ASICs components is increasing as semiconductor integrated circuit technologies shrink in size and provide higher function densities and faster working speeds, while consuming less power and taking less area and weigh on the boards[5].

The main USA component suppliers to the space industry, Actel [6] and Xilinx[7], aim to benefit from this growth in two ways: through the increase in manufacturing and from a technology shift. Sharon Blades, Actel’s senior regional sales manager for northern Europe, emphasises “It’s big in Europe, America and India. The satellite business is a booming business – all sorts of satellites, whether for Earth monitoring, telecom or other applications. This has been our biggest year to date”.

The technology shift is taking the market away from ASICs towards programmable and reprogrammable devices, FPGAs. ASIC offer higher logic densities and lower costs at higher volumes, but demand serious upfront investment – known as non-recurrent engineering (NRE) - to make the masks that define the devices functions during manufacturing. “And customers don’t want to commit to NREs if they don’t have to” says Blades. On the other hand, Amit Dhir, senior director of Xilinx aerospace, defence and high performance computing business, says that the advantages of FPGAs are not just about the cost: “They allow customers to make changes right up to launch and they can get to market much quicker”[3].

The graph below made by ESA Microelectronics Section show an approximation of the evolution of FPGA and ASIC use in space missions in the next years[5].

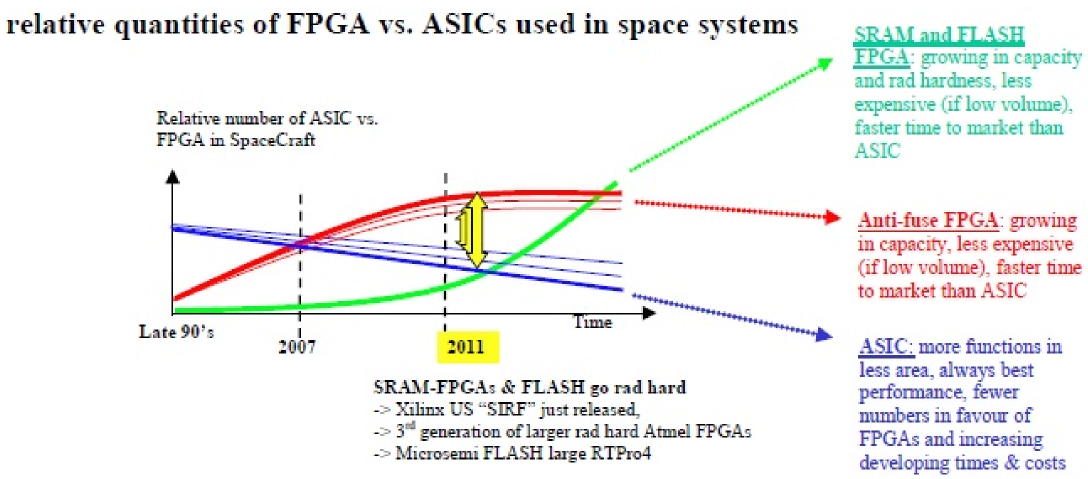

Figure 1: Trends in relative quantities of FPGA vs. ASICs used in space systems

However, the migration from ASIC to FPGA is not entirely simply for non-US satellite designers. All the major space FPGA suppliers are US companies, and as a consequence their space parts must be checked and sometimes explicitly approved for export under the US International Traffic in Arms Regulation (ITAR). If a part is protected by ITAR, much information about the technologies it contains is restricted to US citizens unless the Department of State grants an exemption. ITAR is an intend to stop American technology falling into enemy hands, but restrictions on military-grade chips can be an issue for non-US space organisations[3].

The European Space Agency has expressed that these regulations further complicate project management. Wolfgang Veith, ESA’s head of product assurance and safety, points out this issue:”It increases the risk, both programmatic and technological. It’s programmatic risk because it inevitably leads to extended procurement times. And the lifecycle of each component must be tracked to a large level of detail, from design to integration to testing to launch.”

In addition, restricted access to US technology makes failure analysis more difficult. “With European components, we have complete traceability and visibility. We have a deep insight”, Veith says. “But that is not the case with US components. We are very often denied the detailed knowledge that we require. Generally, this is not a problem but if something goes wrong then it can be. ”

Europe has an strategic interest in developing, maintaining and improving the availability of European space ASIC, FPGA, Microprocessor and Std. ASIC technology (AFMS) in order to increase competitiveness of European satellite equipment manufacturers and minimize the dependency on export restrictions like US International Traffic in Arms Regulations[8].

The motivation of this research is to quantify the types of ASIC, FPGA, Microprocessors and Std. ASIC used in the last years in European space missions. This study will provide ESA and the European space community with better and more accurate information of the use of AFMS in European space mission that can help ESA policy managers to make more educated decisions and face in better conditions the new challenges of complex IC technologies in the space sector as the technology shift from ASIC to FPGA technology and the reduction of US components dependency.

1.2 Research objectives

The aim of this research is to quantify the number of ASICs, FPGAs, Microprocessors and Standard ASICs (AFMS) used in European satellites in the last years in order to show the trends and patterns of use of these technologies in space missions and try to give some conclusions that could have a positive impact in the future decisions and developments of complex integrated circuit technologies in the European space sector.

This study has never been done before and its results will help and contribute to make better strategic future and investment decisions of the European Space Agency and all European space community actors involved in the developing of these technologies, technology vendors and technology customers.

This project analyses the past, current and future situations of the use of these technologies in space missions in order to help ESA to make more educated decisions about future investments. The research compares and connects the results obtained in the data exploration with the current ESA Microelectronics technology roadmaps (MTR) activities [5] to see how ESA is supporting and helping to fund these technologies and if the current and estimated future use of these technologies is in good match with the priorities adopted in ESA's roadmaps.

In addition, this study suggests improvements at the present ESA mechanisms to collect and archive the electronic, electrical and electromechanical (EEE) components information used in space missions.

To achieve the objectives of this research, there are some research questions and sub-questions that can help on defining the research strategy and putting some boundaries to the project.

The main research question is:

What are the trends and patterns of use of ASIC, FPGA, Microprocessor and Standard ASIC technologies in space missions and how are they reflected in the priorities of the European Space Agency for developing future integrated circuit technologies?

This main research question has been divided in some sub-questions in order to make the main objective more approachable:

1) *What quantities and types of AFMS have been used in space missions both in the payload and the platform in the last years?*

    1.1 *What are the quantities of AFMS used in space missions?*
    1.2 *What are the quantities of Programmable ICs (FPGA) versus Non-programmable ICs (ASIC, Microprocessors and Std. ASIC) used in space missions?*
    1.3 *What is the rate of reuse of complex IC designs used in space missions?*
    1.4 *What are the vendors and device families of the FPGAs more used in space missions?*

1.5 What are the Microprocessors and Std. ASICs used in space missions?

1.6 What is the distribution of technology nodes (i.e. minimum feature size, normally measured as the transistor gate width) in complex ICs used in space missions?

1.7 What are the quantities of analogue/mixed-signal versus digital integrated circuits used in space missions?

1.8 What is the distribution of integrated circuit pin counts (number of pins in the package) in complex ICs used in space missions?

1.9 What countries design complex integrated circuits for space missions?

1.10 What countries and vendors provide complex integrated circuits technology for space missions?

These sub-questions aim to quantify the number and types of ASIC, FPGA, Microprocessor and Std. ASIC used both in the payload and the platform of each satellite looking for IC technical characteristics like the rate of reuse IC designs, IC technology nodes, IC pin count, etc.

2) What are the trends and patterns of use of AFMS technologies in space missions?

2.1 What are the trends of use of AFMS in space missions in the timeline?

What are the patterns of use of AFMS in space missions with respect to…

2.2 …the mission lifetime?

2.3 …the mission overall cost?

2.4 …the satellite mass?

2.5 …the space programmes?

2.6 …the orbit?

This second group of sub-questions aims to use the information obtained in the first sub-question to look for trends and patterns in the use of complex integrated circuits from the space missions included in this research with respect to the launch date, lifetime, orbit, etc.

1.3 Anticipated issues

This chapter explains the difficulties and issues that were identified before starting the research which could introduce complexity in the development of this study. They are presented in the next points:

- **Lack of in-house know-how**

It is the first time that a study aims to quantify the ASIC, FPGA, Microprocessors and Std. ASIC used in ESA space missions. For this reason, there is no in-house reference to an appropriate methodology that could be used

- **Spread data and information**

The data of the quantities of AFMS used in space missions is spread among many documents, people and databases both from ESA and European space industry. The lack of integrated database containing this information could make the data collection process very slow and complex.

- **Information stored in different formats, styles and physical supports**

Beside the last point, there is not a standardized document that contains all the information requested in this research. It will be necessary to collect the data from documents with a diversity of formats, styles and physical supports.

- **Availability of the information**

As this information has never been searched before, there is no certainty that all this data will be available and possible to be collected. The results of this research will depend on the complexity of collecting and completing the data.

- **Confidentiality issues**

Most of the data needed for this research is under confidentiality restrictions both from ESA and the Industry. As a consequence, it will be necessary to ask for special permissions which can take more time and efforts, and in the worst case, the data could not be available due to confidential restrictions.

- **Time limitations**

The time to undertake this research is very limited, 5 months research, compared to the ambitious objectives it has. A first planning is scheduled to start with 3 months for data collection, 1 month for data exploration and 1 month to present and explain the results. The aim is to achieve as much as possible the objectives of the research but it is assumed that probably some of the objectives will not be achieved due to the complexity of the research and the issues commented above.

2 BACKGROUND INFORMATION

This chapter tries to compile all the information needed to understand the results of this research. It starts describing the AFMS technologies, continues presenting the main ESA information related to its organization, space missions, technology programmes and technology harmonisation, and finishes presenting the technology roadmapping tool.

2.1 ASIC, FPGA, Microprocessor and Standard ASIC technology

a) ASIC and FPGA: Definition and characteristics

Application Specific Integrated Circuit and Field Programmable Gate Array are very complex and dense integrated circuits used to contain control and data processing functions[9].

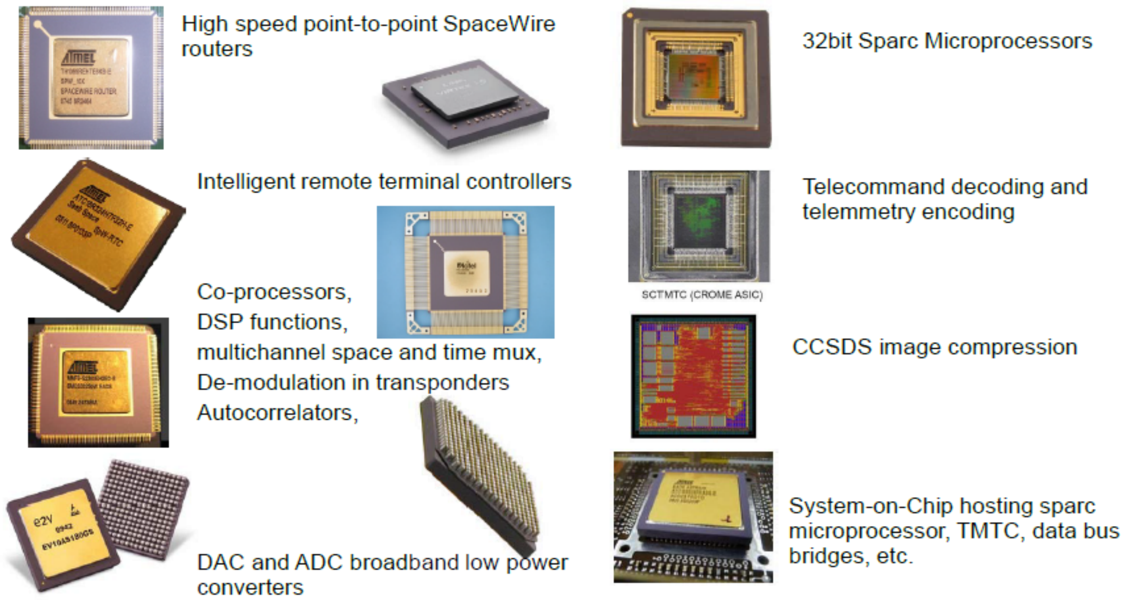

Figure 2: Integrated circuits for space applications

The complexity of these integrated circuits can be defined by the number of gates and the package number of pins. Today, space ASICs and FPGAs can have several million gates, track widths of 65 nm and packages with more than 1500 pins.

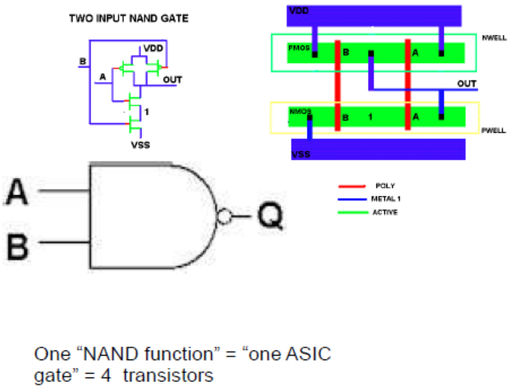

Figure 3: ASIC transistors and gates lay-out

ASICs and FPGAs are based in the same technology. They are built on silicon wafers, where circuits are chemically diffused with lithographic techniques, with very expensive, complex manufacturing tools and recipes, based on CMOS (Complementary Metal Oxide Semiconductor) technology. Moreover, both are designed by an expert team that generates the ASIC or FPGA circuit design using very similar standard CAD tools. However, the main difference between these technologies is that ASICs are unique types of integrated circuits meant for a specific application while FPGAs are reprogrammable integrated circuits[10].

On one hand, the advantage of ASIC technology lies in the performance as it has much denser layouts and interconnections that give a better speed and higher power performance than FPGA technology. On the other hand, ASICs are based on application specific customer designs and as consequence they have higher manufacturing costs and longer lead-times than FPGA technology[9].

In contrast, FPGAs are off-the-shelf components ready to be programmed with designs in a few minutes at designer’s premises. They are normally cheaper for low production volumes and have shorter lead-times than ASICs. However, the fixed array structure of FPGAs limits their performance, size and power optimisation.

b) ASIC and FPGA for space applications

Integrated circuits are of capital importance in order to achieve the necessary miniaturisation and performance levels that today and future space systems demand. Mask or field programmable integrated circuits implementing application specific functions are always one of the most critical microelectronics elements inside the space systems, as they normally host the heart of those systems (data processors, spacecraft controls)[5].

These custom ICs are possible thanks to the joint efforts and technology contributions of different companies and vendors: a design house, responsible for the actual design of the functions/circuit; design tool vendors, who provide the tools to do the designs; silicon technology manufacturers responsible for the technology where the functions will be implemented as hardware devices.

Although ASIC and FPGA follow a very strict and quality manufacturing process, there are some causes that can produce their failure:

- **Design mistake** some nominal or corner cases never simulated
- **Manufacturing problem** silicon wafer defects, badly calibrated machine, operator error, poor or insufficient error screening, etc.
- **System environment** out of specification use
- **Aging effects** electro migration, channel hot carriers, etc.

A part from these reasons, ASIC and FPGA used for space applications need to be more resistant due to the space environment effects:

- Vibration and mechanical shock
- Extreme temperatures
- Contamination effects
- Radiation effects

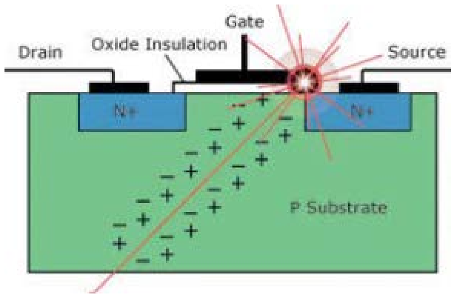

Figure 4: Radiation effects

Radiation effects are one of the main concerns for ASIC and FPGA use in space because they can bring to temporary or permanent integrated circuit malfunctions, risk of mission failure or loss and in there is not option to on-board integrated circuit replacement or repair in space.

ASIC and FPGA technologies for space applications follow special design process and are implemented with countermeasures to strength the protection against space radiation effects. These complex integrated circuits are requested to pass very strict and severe tests and simulations in order to be qualified for space applications.

Consequently, these technologies are very expensive to manufacture and test, and together with a very low volume market makes them a very special niche market that needs the support and funding from the European Space Agency for their research and development[1].

c) ASIC and FPGA vendors

There are several companies offering ASIC manufacturing service or operating as fabless ASIC vendors in Europe. They offer a combined wide range of digital, analogue and mixed signal technology for custom and semi-custom ASICs and other specialised integrated circuits as memories, microprocessors, FPGAs, convertors, image sensors, digital and linear discrete. They have all already produced integrated circuits for space applications or are being evaluated for space IC production[5].

These are some of the main groups which fit into the ASIC / complex IC category described above :

o **Atmel**	France with corporation HQ in USA
o **Austria Micro systems**	Austria
o **E2V**	France , UK
o **IHP**	Germany
o **IMEC**	Belgium
o **Infineon**	Germany
o **LFoundry**	Germany and France
o **TI**	UK with corporation HQ in USA
o **ON Semiconductors**	Belgium
o **Peregrine**	UK with corporation HQ in USA
o **Silana**	UK, HQ in Australia
o **STMicroelectronics**	France, Italy and Netherlands
o **X-FAB**	Germany, UK

For FPGA technology, the only European supplier is ATMEL who in 2004 introduced its first FPGA for space applications manufactured with European technology.

The main vendors of FPGAs currently used in European space applications are MICROSEMI (who acquired ACTEL in 2011) followed by XILINX, both headquartered in USA, with a technology offer that is manufactured, assembled and tested in Asia and the USA.

In some exceptional cases, some commercial FPGA technologies (also non-European, e.g. Lattice) have been used in European space projects, normally after applying countermeasures against radiation effects. This usage is only limited to non-critical applications inside payload instruments whose eventual radiation effects can be tolerated and managed by the instrument, and do not endanger the global success of the mission.

d) ASIC and FPGA: Trends and evolution

The current trend in space projects is to use more and more FPGA technology (whenever the application is not highly demanding in terms of power, speed and size). The FPGA approach is often a cheaper and faster development alternative to the ASIC approach, particularly for low volume integrated circuit needs. This is normally the case in space developments, with the exception, for example, of high telecom processing payloads where large arrays of ASICs are needed to implement the required processing capacity at an optimized power budget[5].

It is very difficult to quantify how much market share the FPGAs are taking over from the ASIC solution. At the beginning of the nineties FPGAs were hardly used inside space systems. Slowly, but steadily, FPGAs began to be introduced in the space units, taking place to ASICs. Reprogrammable FPGAs are finding their place in satellites and spacecraft, normally for non-mission critical applications, in the payload, where their higher sensitivity to radiation could be tolerated in exchange of having maximum flexibility to implement changes to the design without having to incur into lengthy and expensive redesign costs.

Some of the trends that make FPGAs a better alternative to ASICs for a growing number of higher-volume applications are[11][11][11][11][11]:

- Increasing integrated circuit design costs
- FPGA offers time-to-market advantage
- Weak economy asking for low-cost technologies
- Reusability and lower non-recurring engineering costs
- Some FPGAs have the capability of partial re-configuration that lets one portion of the device be reprogrammed while other portions continue running

However, there are some disadvantages with FPGA:

- Not a right device for high volume applications
- Higher power consumption compared to ASIC
- Large configuration time and compilation time in FPGAs compared with general-purpose processor

e) Microprocessors

A microprocessor is an integrated circuit with very extended and versatile use. It is a multipurpose programmable device that accepts digital data as input, processes it according to instructions stored in its memory, and provides results as output. Microprocessors operate in numbers and symbols represented in binary numeral system[12].

Microprocessors used for space applications need some improvements to prevent from the radiation effects. One of the main companies involved in developing these technologies is Atmel (France) who has been building rad-hard microprocessors for space for more than 16 years[13].

f) Standard ASICs

Standard ASICs (also sometimes called “Application Specific Standard Products” or ASSPs) are catalogue products available off-the-shelf normally from the ASIC vendor which manufactured it. The advantage of Std. ASICs is that customers can reuse specific standard functions designed by the vendor using these components which save a lot of economic and time resources for the user.

In Europe, Atmel (France) and Dynex (UK) are the only companies that have a portfolio of Standard digital ASICs for space applications. This has been possible due to the dedicated ESA funded developments in order to have these ASICs available as Standard products for European space applications[5].

Microprocessors and Standard ASICs are very important and critical electronic components used in the avionics control and data processing systems in space missions and they are included in this research as a specific type of complex integrated circuits together with the ASIC and FPGA technology.

2.2 European Space Agency (ESA)

2.2.1 ESA Facts

European Space Agency mission is to promote, for exclusively peaceful purposes, cooperation among European countries in space research and technology and their space applications[14].

ESA was established in 1975 and at this moment has 19 member states: Austria, Belgium, Czech Republic, Denmark, Finland, France, Germany, Greece, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Romania, Spain, Sweden, Switzerland and United Kingdom.

In addition, Canada takes part in some projects under a cooperation agreement and Hungary, Poland, Slovenia, and Estonia are participating in a Plan for European Cooperating States, while other countries are in negotiation about joining this initiative[15].

ESA is headquartered in Paris and has five other main establishments: ESTEC in Netherlands, ESRIN in Italy, ESOC and EAC in Germany and ESAC in Spain. The total staff of all the establishments is more than 2.000 people and the overall annual budget is about 4.000 million Euros (2012) [16].

Over the last 30 years, ESA has designed and tested more than 60 satellites, developed 5 types of launcher and made more than 180 launches to the space.

2.2.2 ESA space missions

ESA space missions can be classified by different parameters, one of the most representatives is the <u>space programme</u> they belong[15]:

a) Earth observation

Earth Observation space satellites are a powerful scientific tool used to learn more about our planet and understand better and improve the management of Earth and its environment. They not only provide information across space but also across time period so they can highlight environmental changes occurring gradually. In long term, monitoring Earth environment will give a reliable assessment of the global impact of human activity and the climate change extension.

b) Human Spaceflight

Human Spaceflight programme has the aim to introduce Europe in the participation of the development of space infrastructure like the International Space Station, which allows conducting experiments in weightlessness environment. The purpose of this research and technology development is to benefit people on Earth and prepare Europe for the new challenges of human space exploration.

c) Launchers

Access to space brings many benefits and this is only possible by having launchers capable to place satellites in space. In the 30 years, Europe has made a big effort to guarantee the access of European satellites to space developing successful like Ariane or Vega. ESA, European research centres and aerospace industry are reviewing new technologies and propulsion systems to make access to space simpler and cheaper in the future.

d) Telecommunications and navigation

ESA and the European Commission are developing the Galileo programme, a joint initiative in order to provide Europe with its own independent global satellite navigation system, compatible and interoperable with the existing American GPS and Russian Glonass military systems.

In addition, telecommunication satellites are a fundamental part of global communications network which represent an important commercial sector and provide all kind of services over almost every region in our planet. ESA supports the deployment of new satellites and programmes like Alphasat/Alphabus a large platform for high-power telecommunication satellites.

e) Technology

ESA works together with European industry in developing and testing sophisticated technologies in order to make future space missions and applications possible. New technology products need to be proved in orbit to make sure there is no risk associated with the use of these technologies in Space. ESA is preserving and expanding the technology base of European industry to ensure its competitiveness and give rise to commercial products and services.

f) Science and robotic exploration

Space Science missions explore our Solar System and Universe to try to answer ultimate question like how did our Earth and Solar System evolve , where are we in the universe, where did the life come from and if we are alone in the universe. ESA is working now in a programme for the next twenty years with the aim to discover if other worlds exist and how life and the Universe evolved from the Big Bang to nowadays.

A part from the space program, ESA satellites can also be classified by their Earth orbit:

a) Low Earth Orbit (LEO)

LEO is defined as an orbit below an altitude of 2000 km from the Earth. For example, this is the orbit of the International Space Station and many Earth Observation satellites.

b) Medium Earth Orbit (MEO)

MEO is the region of the space around the Earth above the LEO orbit (2000 Km) and below Geostationary Orbit (35786 Km). It is common for navigation satellites.

c) Geostationary Earth Orbit (GEO)

GEO is a circular orbit at 35786 Km altitude from the Earth. An object in this orbit has an orbital period equal to the Earth rotational period (one day) so the object in the space looks motionless as a fix position in the sky. It is common for telecommunication satellites.

d) Interplanetary

Interplanetary "orbit" is a trip of a satellite to another planet so it is not orbiting around Earth. Most science programme satellites fall in this orbit category.

3 METHODOLOGY

3.1 Integrated circuit technologies and space missions studied

Ideally, this research would have included all integrated circuits used in all ESA satellites but due to time limitations, 5 months research, it has only focused in some specific types of technologies used in a selected number of space missions. This chapter describes the types of integrated circuit technologies studied and explains what space missions have been prioritized for this study.

3.1.1 Integrated circuit technologies subject of this research

The study focuses on high complexity and high effort design full-custom or semi-custom integrated circuits, which use digital, analogue or mixed-signal technology, both programmable and non-programmable. The specific types of complex integrated circuits included in this study are:

- **ASIC (Application Specific Integrated Circuit):** is an integrated circuit designed and manufactured for a particular use, rather than intended for general-purpose use. This study covers digital and mixed-signal ASICs, but focuses only on "high complexity" ASICs, excluding from the analysis ASICs with less than 40 pins.

- **FPGA (Field Programmable Gate Array):** is a general purpose integrated circuit designed to be configured by the customer or designer after manufacturing. The configuration of the FPGA (also referred to as "programming" or "burning" the FPGA) is achieved by programming memory cells or fuses inside the chip that determine the internal connectivity of create the desire functions inside the FPGA. This study covers all the FPGA types that were found in the components lists of the satellites examined, without exclusions.

This research also distinguishes and compiles information of two other classes of integrated circuits that have a special interest in the ESA Microelectronics technology roadmaps:

- **Microprocessor:** is a general purpose integrated circuit that incorporates the functions of a computer's central processing unit (CPU). It performs logical and arithmetic operations on the input data, as specified in the instructions created by the user ("software"), and produces output data. The data and instructions are normally stored in external memory chips. This study covers all microprocessors types that were found in the components lists of the satellites examined, without exclusions.
  Therefore, this category includes "**Digital Signal Processors**" (microprocessors with an architecture optimized for the fast operational needs of digital signal processing) and

"**Microcontrollers**" (small microprocessors normally used for more specific embedded applications).

- **Standard ASIC (or Application Specific Standard Product, ASSP):** is an integrated circuit that implements certain specific functions that appeal to a market wider than the company which created the IC. As opposed to ASICs which are produced by or for one customer, Standard ASICs or ASSPs are available as off-the-shelf components. This study covered digital and mixed-signal Standard ASICs or ASSPs, but focused only on "high complexity" ones, excluding from the analysis those with less than 40 pins and those with very simple and limited amount of functions (see exclusions below).

Due to the limited time (5 months) and human resources allocated to this study, this research focuses exclusively on the components stated above, and excludes the following IC components:

- Integrated circuits with less than 40 pins (low complexity)
- Low complexity (less than 40 pins) digital, analogue and mixed-signal ICs which are available as ASSPs or catalogue standard products, among which:
  - Transceivers
  - Analogue-to-Digital (ADC and DAC converters)
  - Amplifiers
  - Encoders/ Decoders
- Monolithic Microwave IC (MMIC)
- Radio Frequency (RF) circuits
- Image sensors
- Memories

In conclusion, this study focuses on the most complex integrated circuits used in space missions that are of special interest for support and development as reflected in the ESA Microelectronics technology roadmap activities.

3.1.2 IC Technical parameters

The complex integrated circuits presented above have many technical parameters and characteristics that can be studied. However, to focus on the objectives of this research the IC technical parameters studied for each component found in this research are the following:

- **Designed by**: company, university or institute who designed (ASIC, FPGA) or used (Std. ASIC or Microprocessor) the component
- **Design country:** home country of the designer of the IC or the user of the existing IC.
- **Vendor:** company who supplies the technology
- **Vendor country:** home country of the vendor
- **Analogue & Mixed-signal /Digital**
  - **Analogue & Mixed signal:** IC using analogue or mixed-signal functions

    - **Digital:** IC implementing only digital functions
- **FPGA type (FPGA):** defines the specific FPGA device
- **Antifuse/FLASH/SRAM(FPGA)**
    - **Antifuse:** one time programmable
    - **FLASH:** reprogrammable, based on EEPROM memory cells
    - **SRAM:** reprogrammable, based on SRAM cells
- **Product name (µP, Std. ASIC):** standard name for Microprocessors and Std. ASICs
- **Feature size:** smallest size of the physical tracks lay-out that make the basic circuit elements: the transistors. It is an indicator of the complexity of the component, as smaller feature sizes are used for very complex (high number of logic gates and pins) designs, on average
- **Package type:** encapsulation technology
- **Number of pins:** number of the package pins (inputs and outputs)
- **Payload/ Platform**
    - **Payload:** contains all instrument and experiment units on-board satellite
    - **Platform:** contains the avionics (on-board computer and data handling systems) that globally control the satellite
- **Unit:** name of the sub-system that contains the components
- **Quantity:** total IC quantity used on-board the satellite

3.1.3 Space Missions

The European Space Agency has launched around 60 space missions in the last 35 years. However, this research will only analyse, due to time limitations, some of these satellites and spacecrafts. The type of mission, the launch date and other mission characteristics are the main criteria followed to choose the space missions included in this research but there are also other variables that have been taking into account like the complexity to obtain the data.

These are the mission characteristics that have influenced the selection of space missions to be included in this research.

- **Space programmes**

  Space missions in ESA can be classified in 6 main space programmes: Earth observation, Telecommunications and Navigation, Human Spaceflight, Launchers, Technology and Science. To have a complete view of all the integrated circuits used in space missions, it is important to include satellites from different space programmes as each space has its own objectives and characteristics and this affects to the nature of the components used in the satellites.

- **Launch date**

This research includes space missions launched in different dates to be able to analyse and compare the results in time, showing the evolution of use of the integrated circuit technologies. The baseline was to cover missions launched since around 2000 and onwards.

- **Lifetime**

  Satellite lifetime defines the nominal duration of a mission in space. It is expected to find differences in the use of complex integrated circuits depending on the life duration of the mission and for this reason it is interesting to select space mission with lifetime variety.

- **Cost**

  Satellite overall cost is a very significant characteristic of a satellite as it shows what is the amount of economic and technical resources invested in a mission and it will be very interesting to see how the use of complex integrated circuits is influenced by the total budget of the mission.

- **Mass**

  Satellite mass, and therefore most of the times that means larger size and overall complexity, is another characteristic that could drive differences in the quantities of electronic components used in the spacecraft so it is important to have a wide range of space missions with different mass.

- **Orbit**

  Satellite orbit is a satellite characteristic that might have a strong influence in the selection of the integrated circuits to be used. The study tried to include a variety of space missions with different orbits. The satellite orbits can be classified in four groups: LEO, MEO, GEO and Interplanetary.

Out of a global ESA mission list of more than 60 space missions, this is the list of the 17 space missions selected as top priority for this research, in an effort to maximise diversity in all the parameters listed above, while also taking into account the anticipated difficulties and easiness in accessing the necessary information for the study:

Name	Programme	Launch Date
Ariane 5	Launcher	1997
Proba 1	Technology	2001
Artemis	Telecommunication	2001
Envisat	Earth Observation	2002
Rosetta	Science	2004
Venus Express	Science	2005
Immarsat 4	Telecommunication	2005
ATV	Human Spaceflight	2008
GOCE	Earth Observation	2009
Herschel-Planck	Science	2009
Proba 2	Technology	2009
Hylas	Telecommunication	2010
Galileo IOV	Navigation	2011
Vega	Launcher	2012
Proba V	Technology	2012
Sentinel 2	Earth Observation	2013
Bepicolombo	Science	2014

Table 1: Top priority 17 space missions to be studied

However, this list was subjected to some modifications due to time limitations and the actual difficulties encountered when trying to obtain the data (explained in the Methodology chapter) and at the end of the 5 month research, the list of space missions included in this study to be analysed was finally reduced to 11 missions.

These are the European Space missions finally included in this research:

Mission name	Space Programme	Launch date	Lifetime (years)	Cost (M€)	Mass (Kg)	Orbit
Ariane 5	Launcher	1997	-	8000	746000	GEO
Rosetta	Science	2004	12	1000	3000	Interplanetary
Venus Express	Science	2005	9	220	1240	Interplanetary
GOCE	Earth Observation	2009	1.7	350	1050	LEO
Immarsat 4	Telecommunication	2009	13	1200	5960	GEO
Hylas	Telecommunication	2010	15	120	2242	GEO
Galileo IOV	Navigation	2011	12	1512	700	MEO
Vega	Launcher	2012	-	710	138000	LEO
Proba V	Technology	2012	2.5	60	160	LEO
Sentinel 2	Earth Observation	2013	7	435	1200	LEO
Bepicolombo	Science	2014	7.5	970	1140	Interplanetary

Table 2: List of 11 space missions included in this research

This final list includes missions from all the space programmes (in exception of Human Space flight), launch dates range from the 1997 to the 2014 and with a reasonable variety of lifetime, cost, mass and orbit characteristics.

It is important to make clear that even though the space missions included in this research cover a wide range of different types of missions, every space mission is unique and the results of this research will only apply to these space missions selected.

From the 17 missions pre-selected but not included in the research, most of them are in the way to be finished and only need some more time and efforts to be completed. In addition, the number of space missions included in this study is open to be improved with more missions in the future in order to have a more comprehensive vision of the use of these complex integrated circuits in European Space missions.

3.2 Data collection

This chapter aims to explain what was the process and methodology used for the data collection of this research. It is important to take into account that data collection was the part that took most of the time and efforts of this research, around 3 of the 5 months.

The data collection process can be divided in four main phases as the following figure presents:

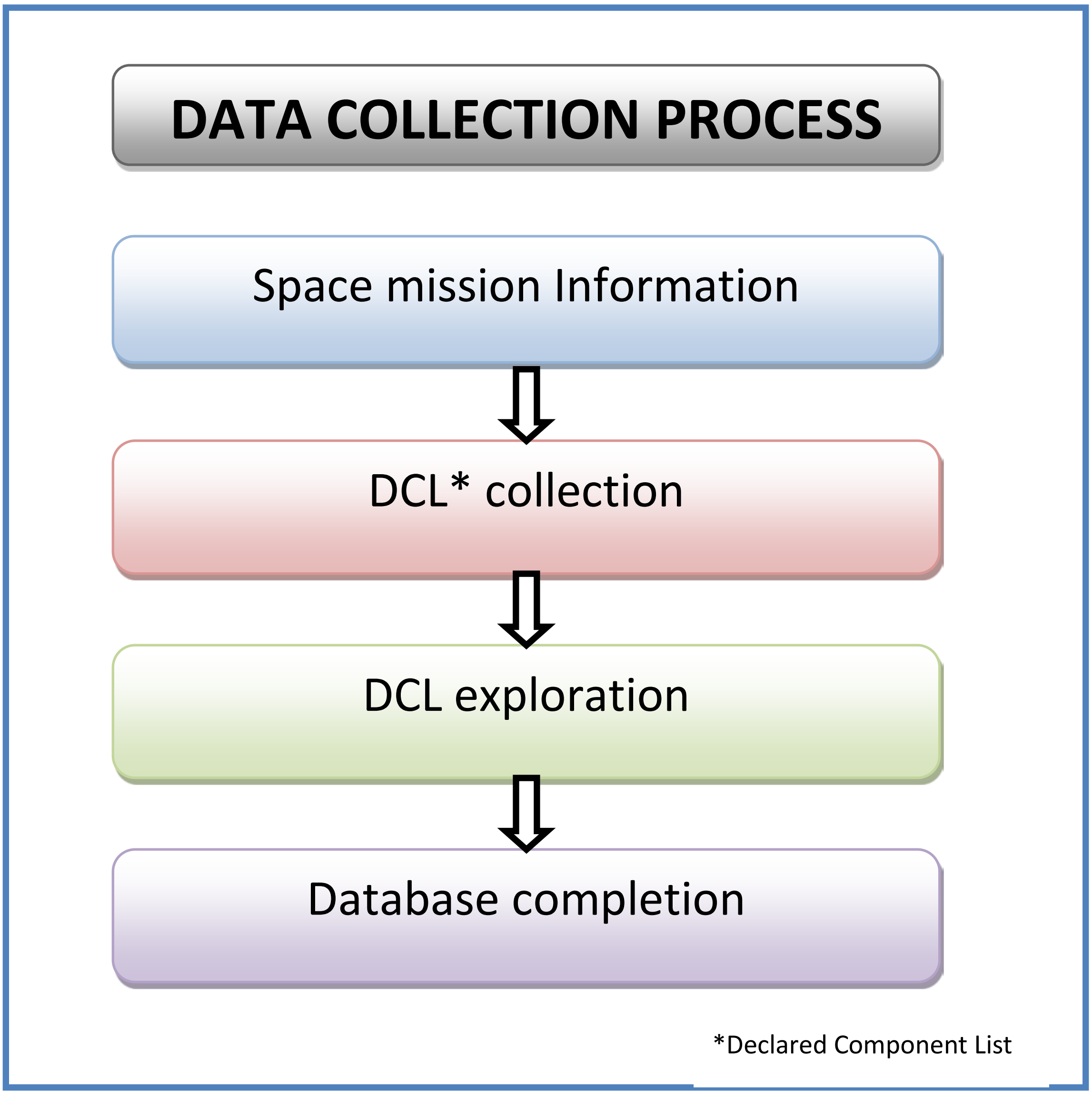

Figure 5: Data collection process

The data collection process started by searching some information of the space missions studied in the research. The objective was to get basic background knowledge about the characteristics and functions of the mission, the main units and instruments that compose the satellite, and some first details of the managers and engineers involved in the mission. This phase took around the 10% of the data collection time.

The second phase consisted on collecting the Declared Component Lists. These documents contain most of the data required in this study. DCLs were collected from ESA and Industry managers and engineers and the procedure to contact these people was based in the fundamentals of the “snowball sampling”, explained below. This phase took around the 30% of the data collection time.

DCL exploration phase used a semi-automatic search algorithm to look into the DCLs for ASIC, FPGA, Microprocessors and Std. ASICs components used in the units and instruments of the space mission. The data extracted in this phase was compiled and managed in an Excel database. This phase took around the 20% of the data collection time.

Data completion phase aimed to obtain and complete the technical information of the components specified in the third phase that is missing or doesn’t appear in the DCLs but that it is required for the research. The two main sources of information to fulfil these gaps in the database were:

a) ESA and industry engineers who supervised or participated in the development of the unit and/or the components inside
b) Component datasheets or other similar documents that contain technical specifications of the components.

The process of contacting the engineers and designers was also based in the snowball sampling technique. This phase took around the 40% of the data collection time.

The process explained above was repeated for each and every of the space missions included in this research. In some cases, it was not possible to finish all the process and some missions are still in the DCL collection or database completion phase.

This is a brief description of some important concepts, methods and tools used in the Data collection process:

a) **Declared Component List**

A Declared Component List or DCL is a document made by the prime contractor of the mission that contains the list of all EEE components used in the spacecraft.

In general, DCLs give information of the components used in one unit or equipment but sometimes it is possible to find a consolidated DCL compiling the DCLs of all units and listing all the components used in the overall satellite. DCLs can be found in PDF, paper or Excel format.

Declared Components Lists is the reference document used to get the data needed for this research. However, they do not contain all the data requested and often some information in the document is missing. The information that can normally be obtained from a DCL is:

- **AFMS and name**
- **Designer and designer country**
- **Vendor and vendor country**
- **Package type and number of pins**
- **Unit and payload/platform**

- **Quantity**

This is the common information that can be found in a DCL:

ALPHABUS CONFIDENTIAL RESTRICTIVE USE

ALPHABUS

Reference :	ABU-JPT-LIS-13671
Date :	14/04/2011
Issue :	6
Page :	25/ 25

3.2 WAY OF READING

Column 1 :	Type and description of the component (For FPGA/PROM PPBI process always included acc to Astrium/Thales internal process)
Column 2 :	Case
Column 3 :	Manufacturer and country (ref attached list §3.1)
Column 4 :	Procurement Agency
Column 5 :	Procurement generic specification (**applicable issue of generic and detail specifications are stated in the PAD sheet ; they can't be introduced in the database**).
Column 6 :	Quality level
Column 7 :	Authorized Part List E3000 (**no more applicable, not used**)
Column 8 :	Approval status of parts : **PAD status is given in PCB's and assessment report**
Column 9 :	PAD sheet reference (**applicable issue of generic and detailed specification are stated in the PAD sheet**).
Column 10 :	Equipments manufacturer
Column 11 :	Quantity of parts per equipment (**for information only**). 0 = qty not provided
Column 12 :	Notes (other than PAD reference.....)

Figure 6: DCL information

b) Snowball sampling

DCL collection and data completion phases use a method to contact ESA and Industry managers and engineers based in the snowball sampling technique. Snowball sampling can be defined as a non-probability sampling technique that is used by researchers to identify potential subjects in studies where subjects are hard to locate[27].

This method is used when researchers do not have access to sufficient people with the characteristics they are seeking[28]. It is particular useful when the population interested to be studied is hidden or hard to reach such as drug addicts, homeless people, prostitutes and so forth[29]. For example, in[30], the snowball sampling was successfully employed investigating backpacker tourists and marginalized men organic social networks and social dynamics.

The snowball sampling procedure is used as follows: A random sample of individuals is drawn from a given finite population. Each individual in the sample is asked to name other different individuals not included before in the sample. Then, each of the individuals of the first stage is asked to name other different individuals not named before. This procedure is continued until each of the individuals of some of the stages has been asked to name different individuals[31]. In other words, the method can be summarized in these points:

- Find people to study
- Ask them to refer people who fit in the study requirements, then continue with these new people
- Repeat this method of requesting referrals until enough people is studied

The snowball sampling can be classified in 3 types[27]:

- Linear snowball sampling

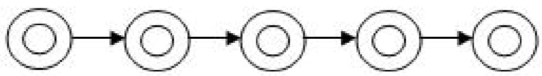

Figure 7: Linear snowball sampling

- Exponential Non-Discriminative snowball sampling

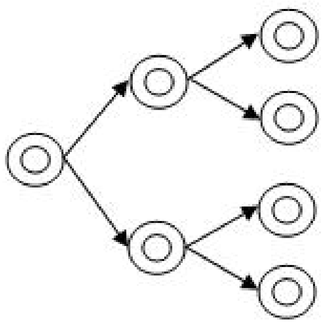

Figure 8: Exponential non-discriminative snowball sampling

- Exponential Discriminative snowball sampling

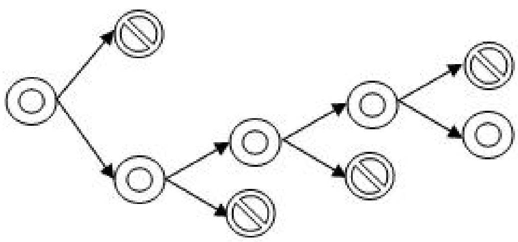

Figure 9: Exponential discriminative snowball sampling

The advantages of this method are the possibility to include people you would not have known before and to collect data from experts recommended by other people that in another method would be impossible to include. On the other hand, there are some disadvantages like that the information collected can be inexact and produce inaccurate results or that there is a lack of definite knowledge as it is not possible to know if all the relevant data has been collected.

The snowball sampling is not used as a sampling method in this research, but its basic principles have been used successfully to get in contact with ESA and Industry managers and engineers that can provide the documents and data needed in this research. Using this method and creating a contact networks, it has been possible to access to critical information that in other way would not be possible. As a result at the end of the 3 months of data collection more than 100 people were contacted and 150 documents were collected.

c) Excel AFMS Database

Microsoft Excel is the main tool used in this research. It has been chosen for its flexibility and ease to work with, as well as, for its performance in data analysis, creating tables and graphs.

The Excel AFMS database contains the data and technical parameters of the ASIC, FPGA, Microprocessor and Std. ASIC used on-board (as explained in 3.1.2), the space mission characteristics (as explained in 3.1.3), the tables and graphs created to explore the data and a list of all data sources used in this research.

3.2.1 Space mission information

Some initial information research about the selected ESA space missions was very important in order to have some background information and better knowledge of the architecture and the purpose of the mission.

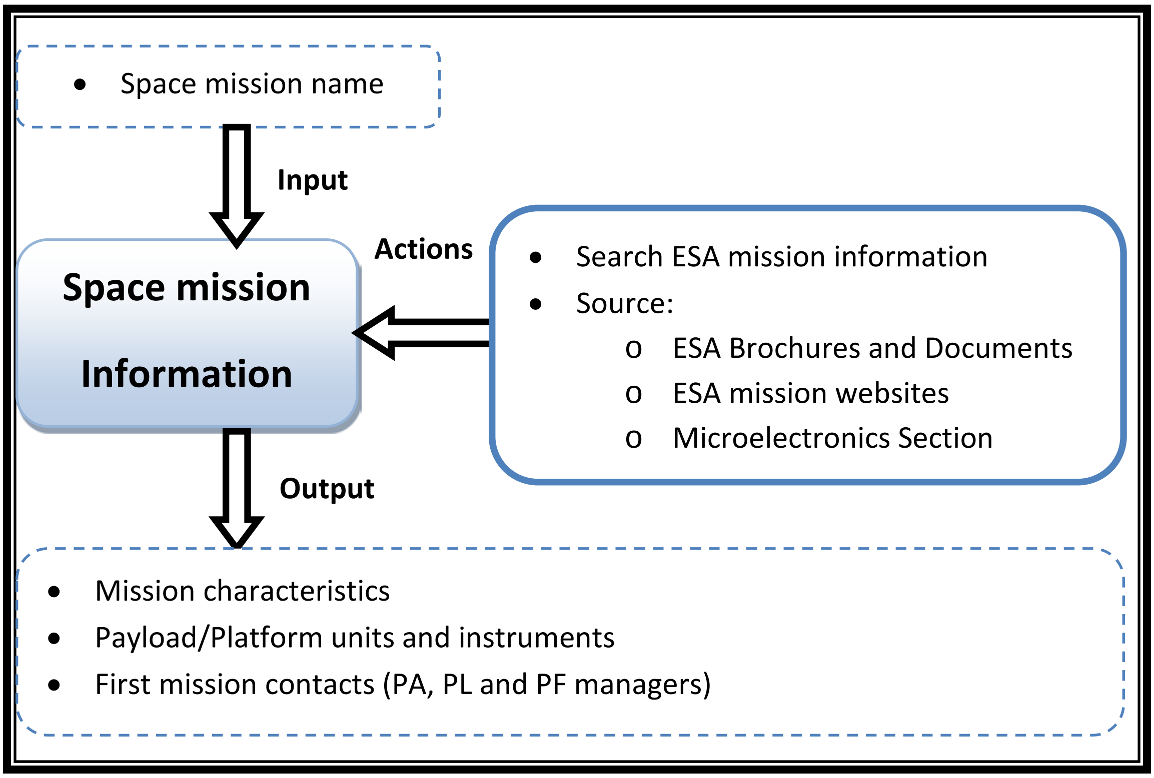

Figure 10: Space mission information process

Basically, the purpose of this phase was to get some information over what units compose the platform and payload of the satellite and which ones have more possibilities to use ASIC, FPGA, Microprocessors and Std. ASICs. It also aimed at finding out the space missions characteristics (e.g. the launch date, lifetime, orbit or cost) and the mission managers and engineers who can help in the DCL collection phase.

Most of this information could be easily found in specific ESA brochures and public and intranet websites for each space mission. To get the first contacts of managers and engineers involved in the space missions it was very useful to talk to the ESA Microelectronics engineers that gives or have given support to those missions.

3.2.2 DCL collection

This phase had as input the contacts of the managers and engineers obtained in the space mission information phase. From these first contacts, a process based in the snowball sampling technique was used to create a network of people that could provide the data and documents needed for this research. These contacts were asked for the DCLs of the mission and once the DCLs were received, they were archived as data source in the Excel AFMS database. The complete process is explained as follows.

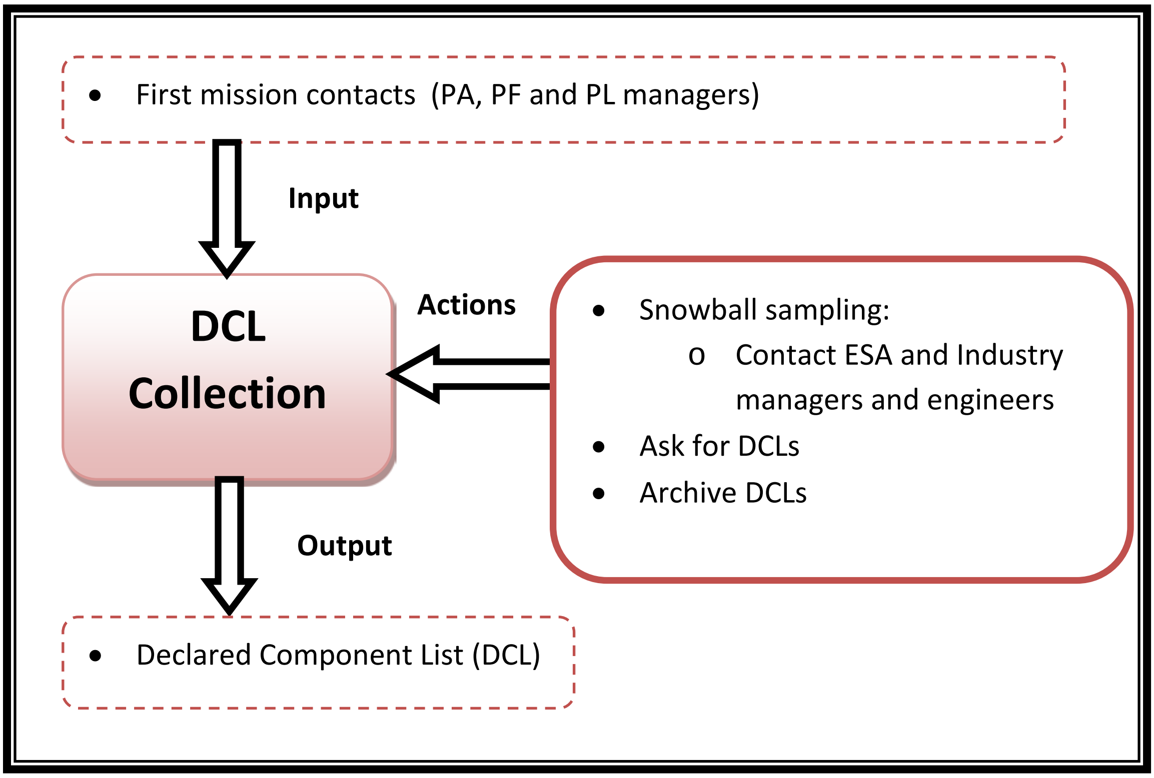

Figure 11: DCL Collection process

The collection data process started contacting the ESA managers and engineers obtained in the space mission information phase. The first contact was done via mail or phone to explain in a few words the objective of the research and the importance of DCL documents to obtain the data needed. Then, it asked for the DCLs of the mission and, in case of not being available, it asked for another contact that could help in getting the requested information.

In general, the response was positive and the people answered sending the DCL (if they had it), or suggesting another contact both from ESA or the Industry. This procedure was repeated systematically until all the DCLs were received.

Sometimes there was no response so a call or mail reminder was send to the contact. In case of not response, the solution was to start the network with another contact.

The positions of the people requested for a DCL were very varied. These are some examples:

- Product Assurance manager
- Platform or Payload manager
- Head of mission projects
- Administrator of Record Management Office
- Senior Component engineer

In addition, the DCLs can be received in different ways and formats, for example:

- By mail, in PDF or Excel format
- By letter, in CD support
- By USB (in person), in PDF or Excel format
- By folders (in person), in paper format

The complexity of this phase was due to the difficulties on collecting all the DCLs of the mission. In the best cases, there was only one consolidated DCL that included all the DCLs of the mission (e.g. Ariane 5). In other cases, there were two consolidated DCLs, one for the payload and another for the platform (e.g. Hylas). However, in most cases, there was a DCL for each unit or instrument of the satellite or spacecraft. This means that first it was necessary to know all the units and instruments of the satellite (Space missions information phase) and then to ask for each of these DCLs which, by the way, were normally provided by different people.

Another difficulties found in this process were related with the confidentiality terms of these documents, the permission to access some specific mission databases or the necessity to contact the industry to obtain certain documents. These are some cases were these difficulties were encountered during the DCL collection phase:

- **Galileo IOV:** to obtain the DCLs of Galileo IOV satellite it was necessary to make sure that the final report will not contain any quotation about company names, disclosing proprietary and company-confidential information.

- **Alphasat/Alphabus:** the DCLs of this mission were archived in a specific database of the mission. To get access to this Data Management System, it was necessary to sign a confidentiality form and to ask for a user profile to be able to search the requested documents in the database. (The data of this mission is not include in this research as it was not possible to collect all the DCLs)

- **Rosetta:** Rosetta mission has the particularity that its payload contains more than 10 different instruments using complex ICs. For this reason, to obtain each instrument DCL it was necessary to contact all of the different companies suppliers of each instrument.

- **Immarsat 4:** this is a very particular case as it is a commercial telecommunications satellite. To obtain the consolidated DCL of the satellite it was necessary to contact and go personally to the industry to copy by hand the information of the DCL as it was not allowed for confidentiality restrictions to send the document or make copies of it.

3.2.3 DCL exploration

Once all the mission DCLs were collected, it was time to explore them in order to extract the list of AFMS and their key parameters used in that mission. The objective of this phase was to fill as many data fields as possible in the Excel AFMS database using the information provided in the DCLs. To do an efficient and successful search and to make sure that no components were missed, a systematic data search algorithm was applied.

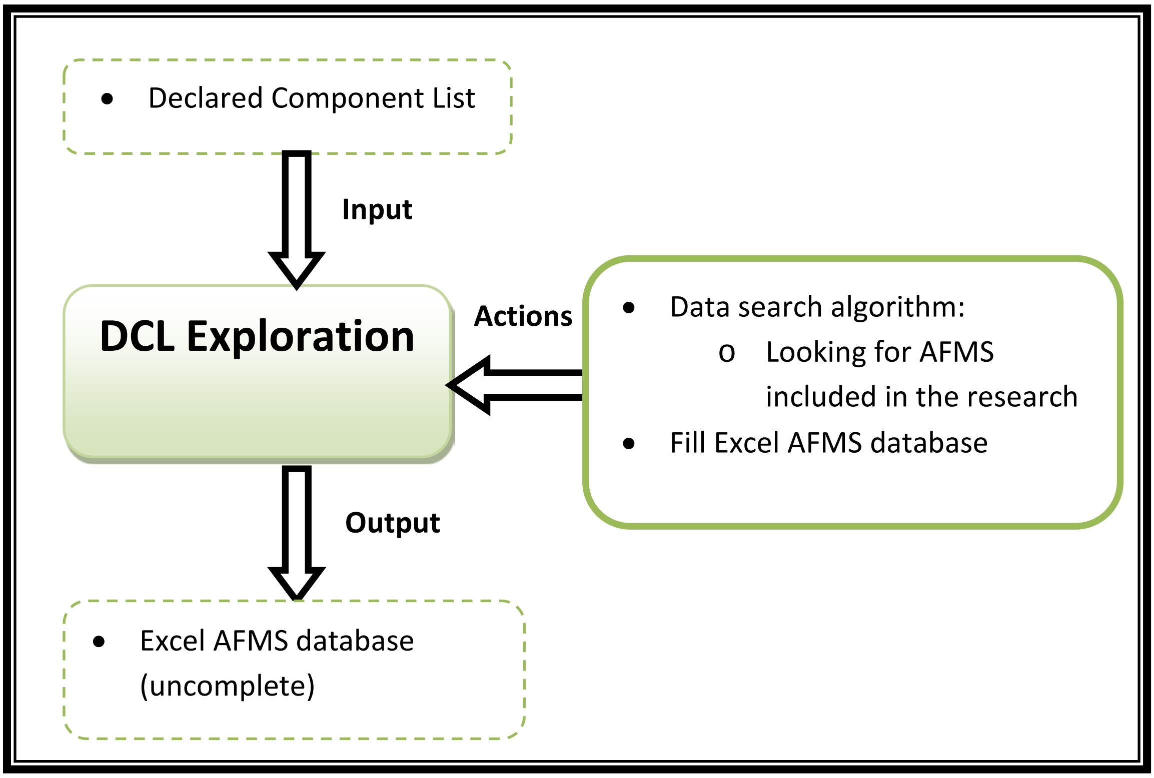

Figure 12: DCL Exploration process

There is not a standardized DCL document for all the units and missions but in general they have similar formats and contain similar information so a generic search algorithm was used to find the complex ICs and associated parameters in the DCL.

When there was uncertainty of whether or not certain electronic component listed in the DCL was to be included in the Excel AFMS database, information resources like Internet, vendor brochures or component datasheets were very helpful in determining whether a given DCL component was to be added to the Excel AFMS database or not. In addition, the experience after exploring many DCLs provided agility to spend less time on applying the data search algorithm.

The Data search algorithm is based on filtering the possible complex IC candidates by using the following criteria:

a) Family Code (FC) and Group Code (GC)

Family Code (FC) and Group Code (GC) is a parameter included in most DCLs that gives a classification in families and groups of the EEE components appearing in the DCL. The codes for the ASIC, FPGA, Microprocessors and Standard ASICs are the following:

FC	GC	Family	Group
08	30	Microcircuits	Programmable Logic
08	40	Microcircuits	ASIC Technology Digital
08	41	Microcircuits	ASIC Technology Linear
08	42	Microcircuits	ASIC Technologies Mixed Analogue/Digital

Table 3: Family Code (FC) and Group Code (GC)

b) Component name and description

The name and description fields of the component in the DCL were the main reference to find the searched components. The keywords used for this search can be generic words like "ASIC","FPGA", "Microprocessor" or "Processor", as well as, the designer's or vendor's name for the ASIC, FPGA, Microprocessor and Standard ASIC, when known.

This is an example list of some known names (used by the vendor and/or the designers) for these integrated circuits:

ASIC	FPGA	Microprocessor	Standard ASIC
AGGA-2A	A1020B	AT695	29C516E
ASP50	A1280XL	AT697E	AT7908E
IBIO S4	A14100A	AT697F	AT7909E
CHASE	A54SX32A	AT7913E	AT7910E
COCOS	AT40KEL040	MA17501	AT7911E
COMA4	RT54SX72SU	MA17502	AT7912F
CROME 2	RTAX1000SL	MA17503	T7906E
HAMSTER	RTAX2000SL	MAS281	TSS901E
M2	RTSX32SU	SpWRTC	UT69151
ZASIC	RTSX72SU	UT699RH	UT1553B

Table 4: ASIC, FPGA, Microprocessor and Standard ASIC example known names

c) Package and pin number

As it was defined before, the scope of this study excludes all the components with less than 40 pins. This gave an easy way to filter and sort all the components of the DCL by the pin number to discard those below 40 pins.

In addition, the package technology gives an idea of the complexity of the component and can also be used as a reference.

These are some examples of packages types used in complex integrated circuits:

Packages
QFP-208
CQFP-256
MQFP-196
CGA-349
DIE

Table 5: Package type examples

d) Vendors and manufacturers

There is a relatively small number of vendors and manufacturers of ASIC and FPGA technology and they can be easily identified. Having a look to the technology vendor website it is often easy to check if a component is one of the complex integrated circuits included in the research.

This is a list of some vendors and manufacturers of these technologies found in the missions investigated:

ASIC	FPGA	Microprocessor	Standard ASIC
Aeroflex	ACTEL (Microsemi)	Aeroflex	Aeroflex
AMIS	Aeroflex	ATMEL	ATMEL
ATMEL	ALTERA	DYNEX	DYNEX
Honeywell	ATMEL	FREESCALE	HONEYWELL
INFINEON	XILINX	HONEYWELL	IBM

Table 6: ASIC, FPGA, Microprocessor and Standard ASIC main vendors

3.2.4 Database completion

The database completion phase focused on getting the data not available yet but necessary to complete all the Excel AFMS database fields of the list of components found in the DCLs. The data missing in the database at this point was due to these two main reasons:

a) there was information missing in the DCL, though the corresponding data field in the DCL was present;
b) the corresponding data field did not appear in the DCL at all.

To find the information missing or not clear in the DCL (a) it was necessary to contact again the ESA managers and engineers who provided the document to ask for further information. In the other case (b), it was necessary to do an information research of each component in particular to obtain that information.

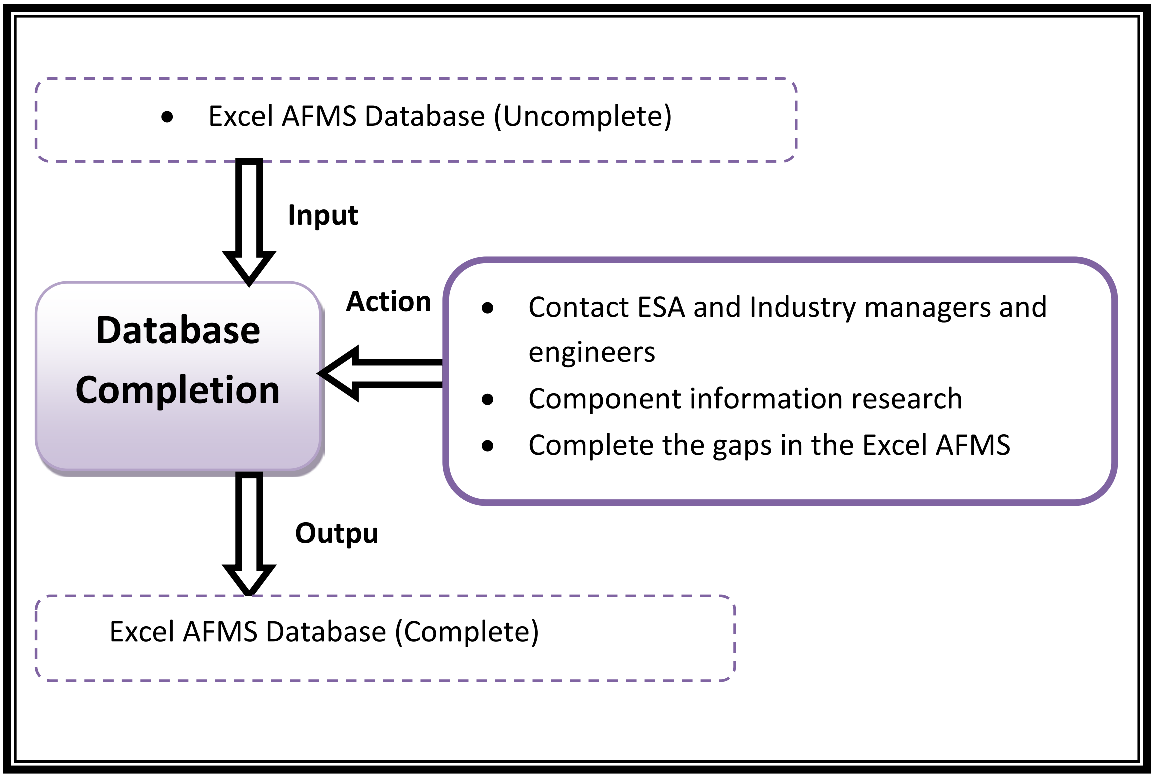

Figure 13: Database completion process

a) Completing the missing information in the DCL

This phase started contacting again the ESA managers and engineers who provided the DCL in order to ask for further and more detailed information about the quantities and other technical characteristics that were missing in the DCL.

To ask for this information, a list of all the missing information in the DCL was created and sent via mail to the contact that provided the DCL asking for some help to complete the information and details missing.

In general, the response was an email or a call explaining the information needed. In some cases, it was possible to arrange a meeting with the ESA engineer involved in the design or the procurement of those components in order to try to solve the doubts in person and fill the information needed. If the contact did not have the information, it was suggested a new contact that could be both from ESA or the supplying company of the component. This procedure was repeated systematically until all the missing gaps were filled.

The quantity of integrated circuits used in the space mission was one of the most critical information needed for this research but at the same time was one of the fields more difficult to fill as it did not appear always in the DCLs. When it did, there was no confidence that the quantities shown in the DCL made reference to the quantities used in the Flight Model, in the Engineering model or prototypes, or the total procurement including or not the attrition and spears.

In addition, the quantities that appear in a DCL normally make reference to the quantity of components per unit so it was necessary to know the number of units in the satellite to get the total quantity used in the satellite. For all the reasons mentioned above, the quantity was the most common Excel AFMS data field requested to be filled and clarified in those mails.

b) Completing the Excel AFMS data fields not included in the DCL

Finally, the most technical parameters of AFMS were not specified in the DCLs so it was necessary to do a research work to find these technical specifications and details.

The Excel AFMS data fields that were not normally specified in the DCL are:

- **Analogue/Mixed-signal/Digital**
- **FPGA type**
- **Antifuse/FLASH/SRAM**
- **Product name**
- **Feature size**

The FPGA type and product name (Microprocessors and Std. ASICs) fields could be completed using the name specified in the DCL and searching in internet for the datasheets of the components to find out the type and the families of the complex IC.

The rest of data fields were tried to be completed looking at the datasheets and other technical documents of the component. It was also useful to ask ESA microelectronics engineers that have given support to those missions or the industry engineers that designed or used that component in particular. Another good source information to complete these data fields was to look for these components in two specific databases from the ESA Microelectronics section (ASCOT and Space ASIC Logbook) which contain a list of ASICs with its technical parameters which ESA has developed or given support.

This last phase of the data collection process was very complex as it has been explained before and with 3 months research was not possible to complete all the information requested.

All the sources of information used along the data collection process (ESA, industry and vendor documents, web links, and names of ESA staff and contractors) are recorded in the Excel AFMS database for future references.

3.3 Data Exploration

This chapter explains the method used to explore, present and visualize the quantities and types of ASIC, FPGA, Microprocessor and Std. ASIC used in European space missions from the data stored in the Excel AFMS database. In addition, it explains the different levels of tables and graphs created in order to explore the trends and patterns of use of these technologies.

The first part of this chapter explains how the different fields and parameters from the Excel database are combined in order to show as much valuable information as possible of the use of AFMS in European space missions. In other words, this chapter explains why some specific data fields are of interest to be crossed in the graphs, instead of others, in order to obtain valuable information.

The second part of this chapter explains the tables and types of graphs created, and their relationships, in order to present and visualize the results of crossing the interesting Excel AFMS data fields and thus try to identify possible trends and patterns of interest for future ESA Microelectronics technology roadmaps.

3.3.1 Subset of IC parameters explored

From the complete set of IC parameters collected in the database only some of them were selected to be explored in order to meet the research objectives. The figure below shows the IC parameters collected for this research and the subset of these data fields selected to be combined and related.

The Excel AFMS data fields that were collected but not used in the data exploration phase can be used in the future for other types of studies, or a continuation and expansion of the work done in this study.

Figure 14: Subset of data fields selected

These are the relations between the subset of data fields selected to be explored in this research:

- **AFMS-Payload/Platform-Total quantity**

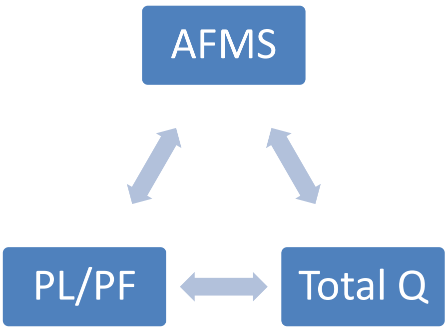

Figure 15: AFMS- Payload/Platform- Total quantity

These 3 data fields were combined to answer the following research sub-questions:

1.1. What are the quantities of AFMS used in space missions?

Crossing the columns of AFMS and Payload/Platform with the quantities used of each component it was possible to get the quantities used of each type of complex IC per payload or platform for each space mission included in this research.

1.2. What are the quantities of Programmable ICs (FPGA) and Non-programmable (ASIC + Microprocessor + Std. ASIC) used in space missions

To get this information it was used the same procedure than the point above but grouping the ASIC, Microprocessors and Std. ASIC as Non-programmable devices and the FPGA as Programmable components.

The idea behind of separating the AFMS in two different groups: the programmable IC (FPGA) and the non-programmable IC (ASIC, Microprocessor and Std. ASIC) was to see how much ground the FPGAs have been gaining in the space avionics (due to their versatility and competitive costs) with respect to the other "non-programmable" IC types.

Even though microprocessors can be also classified as "programmable" ICs because they operate based on software (instructions) which is kept (programmed) on external memory , for the purpose of this comparison, FPGAs are left alone in the "programmable" group, as they are unique IC components in the sense that it is their actual hardware (the inter-connections of their internal circuit blocks) that is physically modified (reconfigured) when the users (not the manufacturer) programme them by either physically modifying anti-fuse structures or programming internal SRAM or EEPROM memory banks, all of them inside the IC device.

This last stage physical modification to the circuitry inside the chip to implement the user desired functions that we are calling "programming" is unique to FPGAs. In the case of microprocessor programming, the instructions that are programmed normally stay outside the microprocessor, in "external" memory devices.

1.3. What is the rate of reuse of complex IC designs used in space missions?

This information needs a more complex procedure to be obtained. First of all, the number of rows in the Excel AFMS database corresponds to a different IC type, or else to an IC type already declared in another row, but used in a different unit. ASICs are counted separately, and then this number is compared to the total quantity of AFMS used both in the payload and the platform to get the rate of reuse of complex IC designs.

These 3 parameters give the quantity of truly "different and unique" AFMS designs (also broken down by IC type indicating if in the PL or PF) compared to the number of parts that constitute "a reuse" of an already counted design (i.e. a repetition in use for an already used design). This comparison was made to find trends or patterns on how same designs are often (and to which extent) repeated inside satellites.

The parts that were counted as reused parts can be found inside a same unit of the PF or PL, or are reused across different units of the satellite. The case of IC design reuse when implemented in FPGAs is more complicated to discern. For example, if there are 8 FPGA Actel RTAX2000 used in the GPS unit of the platform it counts like one same IC design reused 7 times unless there is evidence that some of these FPGAs were hosting different designs, for example because they were designed/used by different groups but for the same unit, and that is reflected on the DCL.

In some cases, this information was provided by, one of the satellite engineers. Else, unless any evidence of the contrary was gathered, the FPGA count is assumed to be a repeat (knowing that this is an assumption in favour of higher reuse rate conclusions).

- **Vendor-FPGA type-Payload/Platform-Total quantity**

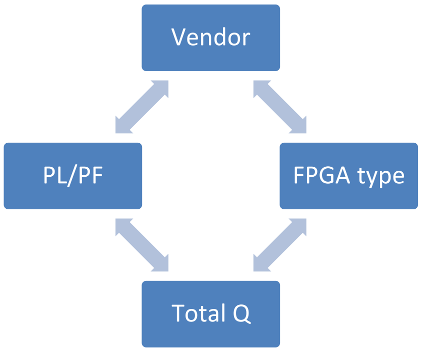

Figure 16: Vendor-FPGA type-Payload/Platform-Total quantity

These 4 data fields were combined to answer the following research sub-question:

1.4. What are the vendors and device families of the FPGAs more used in space missions?

Crossing the columns of FPGA vendors and types, payload/platform and total quantities used of each component it was possible to display the FPGA vendors and types that are more used both in the payload and the platform in space missions.

These sets of data allowed seeing the evolution and trends on specific FPGA families utilisation, across time and different mission types. It is interesting to see how fast or slowly is the adoption of the new FPGA classes introduced in the market, as well as the fading out or permanence of the older devices.

It is also interesting to know what the different rates in the use of different vendor technologies are, and observe the preferences for each technology type depending on the kind of mission. All of this will help in making future IC technology development investment decisions, as well as anticipating dependency with non-European technology.

- **Product name-Payload/Platform-Total quantity**

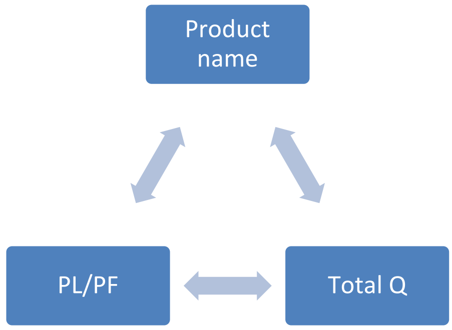

Figure 17: Product name-Payload/Platform-Total quantity

These 3 data fields were combined to answer the following research sub-question:

1.5. What are the Microprocessors and Std. ASICs used in space missions?

The product name column gives the standard name of Microprocessors and Std. ASICs and crossed with the Payload/Platform and total quantity columns shows the types these complex ICs used both for the payload and the platform in space missions.

These two types of ICs are of special interest, since ESA dedicates special efforts to maintain these versatile products available in Europe. The case of Std. ASICs, despite the low usage, has been and still is a special one, as it remains a way to capitalize on the huge time, money and manpower investment that developing a new standardized space IC function represents.

- **Feature size-Payload/Platform-Total quantity**

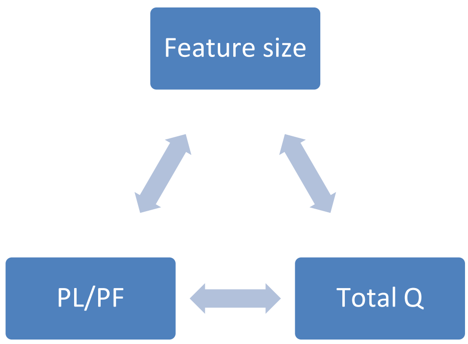

Figure 18: Feature size-Payload/Platform-Total quantity

These 3 data fields were combined to answer the following research sub-question:

1.6. What is the distribution of technology nodes (i.e. minimum feature size, normally measured as the transistor gate width) in complex ICs used in space missions?

Crossing the columns of feature size and Payload/Platform with the quantities used of each component it is possible to get the distribution of technology nodes (i.e. minimum feature size, normally measured as the transistor gate width) range from 0.8 μm to 65nm found in each space mission explored in this research. This comparison revealed trends and patterns on how the new technologies are being adopted, while some of the older ones still remain heavily used or are being phased out of our satellites.

- **Analogue & Mixed-signal /Digital-Payload/Platform-Total quantity**

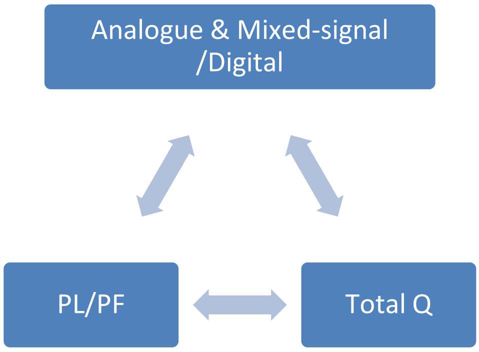

Figure 19: Analogue & Mixed-signal /Digital-Payload/Platform-Total quantity

These 3 data fields were combined to answer the following research sub-question:

1.7. What are the quantities of analogue/mixed-signal versus digital integrated circuits used in space missions?

Crossing these 3 columns it was possible to get the quantities of Analogue & Mixed-signal/Digital components have been used both in the payload and the platform of the space missions explored in this research.

The analogue and mixed-signal components group includes all integrated circuits with total or part of its design being analogue, while the digital devices only contain digital functions. It is interesting to observe and quantify this ratio, as analogue IC technology is becoming a reliable and efficient way to achieve even higher integration levels of the on-board avionics, and therefore save costs and achieve better performance. Yet, there are numerous difficulties in establishing qualified supply chains of the analogue technology for space. ESA is very active in this front, and the Microelectronic technology roadmaps are reflecting and increasing number of new investments in this area.

- **Number of pins-Payload/Platform-Total quantity**

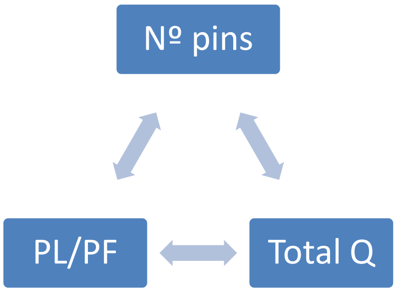

Figure 20: Number of pins-Payload/Platform-Total quantity

These 3 data fields were combined to answer the following research sub-question:

1.8. What is the distribution of integrated circuit pin counts (number of pins in the package) in complex ICs used in space missions?

The number of pins of the complex ICs was classified in some groups to make it easier to explore and cross with the quantities used both in the payload and the platform of space missions. These groups were chosen somehow arbitrarily but bearing most common sizes in mind:

- 41 to 150 pins
- 151 to 250 pins
- 251 to 350 pins
- 351 to 450 pins
- 451 to 650 pins
- More than 650.

As a reminder, this study only includes complex integrated circuits with more than 40 pins.

Observing the number of pins, together with the feature size, we can have a relative idea of the complexity of the designs (which is somehow proportional to the costs and efforts of the users which went into designing (for FPGAs and ASICs) and manufacturing the IC (if we talk about ASICs). These data refers however to all the ICs counted, including pin complexity of the off-the-shelf components (Std. ASICs and microprocessors) and thus reflecting as well the development efforts and costs of the vendors or technology providers.

- **Design country /Digital-Payload/Platform-Total quantity**

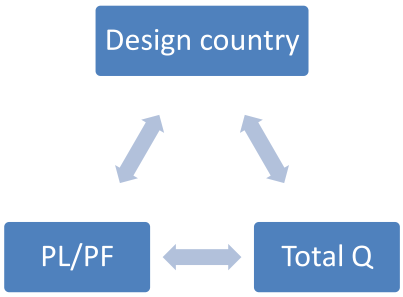

Figure 21: Design country /Digital-Payload/Platform-Total quantity

These 3 data fields were combined to answer the following research sub-question:

1.9. What countries design complex integrated circuits for space missions?

Crossing these 3 columns it was possible to know where the integrated circuits used in the satellite was designed (in case of ASIC and FPGA) or used (in case of the off-the-shelf Std. ASICs and microprocessors).

It was interesting to see the geographical distribution of the IC design efforts. This is something which depends on the ESA contract tendering and awarding process, and therefore it is influenced by technical but also programmatic assessments and decisions.

- **Vendor country /Digital-Payload/Platform-Total quantity**

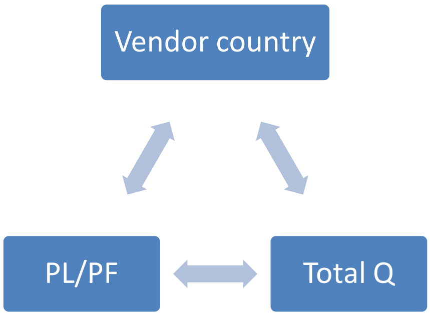

Figure 22: Vendor country /Digital-Payload/Platform-Total quantity

These 3 data fields are combined to answer the following research sub-question:

> *1.10. What countries and vendors provide complex integrated circuits technology for space missions?*

Crossing these 3 columns it was possible to know what countries provide the complex ICs technology used in space missions.

It was of special interest for ESA programmes and roadmaps to observe the ratio between ICs manufactured in Europe and those coming from USA, and therefore affected by export regulations which may have an undesired impact in the calendar of the mission development or even pose some risks to the availability of parts .

4 RESULTS

This chapter discusses the information presented in the graphs in order to try to answer the objectives of the research. It is divided in two parts: the first one presents the results of the quantities and types of AFMS that have been used in space missions both in the payload and the platform in the last years; the second one visualizes the trends and patterns of use of these technologies in the timeline and with respect to different space mission parameters like the lifetime, cost, mass, space programme or orbit.

During the process of data exploration, more than 120 graphs were generated. However, only a small subset of those graphs that show interesting and representative results for the purpose of the research objectives are presented and discussed in this chapter.

The main results presented in this chapter (which of course only apply to the limited group of missions studied in this research) are summarized in the following points:

- The quantities of complex ICs used in space missions move in a range of 50 to 400 per mission, with the exception of Immarsat 4 that uses more than 1500.
- FPGAs are used in average in larger quantities than ASICs with a percentage of 50% to 30%, respectively. Microprocessors and Std. ASICs are used in small quantities with a general percentage of use of around 15% and 5%, respectively.
- The total amount of complex ICs used in European satellites seems to be increasing in the last years, and very likely will continue to grow in the future.
- FPGA technology seems to be taking an increasingly larger share of the complex IC technology used in the space sector in the last years, in detriment of the ASIC market (around 10% of total percentage).
- Missions with longer lifetimes seem to use more ASICs than missions with shorter lifetimes. The same seems to happen for high cost missions compared to low cost missions.
- FPGAs are used in larger quantities the missions studied in this research than non-programmable components (ASIC + Microprocessors + Std. ASIC) with and average percentage of use of 60%.
- The percentage of reuse of complex IC designs in space missions is in average of 80%, with the exception of the launchers Ariane 5 and Vega, with percentages of 42% and 58% respectively
- USA is dominant in the space complex IC market and provides a range of 60% to 90 % of the total number of ICs used in the European space missions included in this research, with the exception of Galileo (15%). All FPGAs are provided by US vendors.
- Telecommunications and navigation satellites use the largest quantities of integrated circuits (400 to 1500), followed by Earth Observation and Science missions (around 200) and Launchers and Technology missions with less than 100 complex ICs per spacecraft.
- On average, the farther is the distance from Earth of an orbit, the larger are the quantities of complex integrated circuits that seem to be used in the satellite.

4.1 Quantities and types of AFMS used in space missions

This chapter explains the use of AFMS technologies, from a quantitative point of view, of the space missions included in this research. The results are presented by each of the IC parameters studied and the results are presented in the following approach:

- Exploring and commenting the graphs that show the quantities and types of AFMS used per space missions;
- Displaying and commenting one mission graph as an example and then compare its results with the particularities of other space missions included in this research
- Giving general conclusions and trying to highlight the main important points observed in data gathered about the type of technology used per mission (spacecraft).

Sentinel 2 mission was chosen as the example case to be visualized and compared to the other missions included in this research because it can be defined as a representative and well into the average space mission case in terms of the quantities and types of complex integrated circuits used both in the payload and the platform.

These are the main mission characteristics of **Sentinel 2**:

Space Programme	Earth Observation
Launch date	2013
Lifetime (years)	7
Cost (M€)	435
Mass (Kg)	1200
Orbit (Km)	LEO
Prime	EADS Astrium
Prime country	Germany

Table 7: Sentinel 2 mission characteristics

4.1.1 IC Overview

The chart below shows in columns the total quantity of AFMS used in the 11 space missions included in this research.

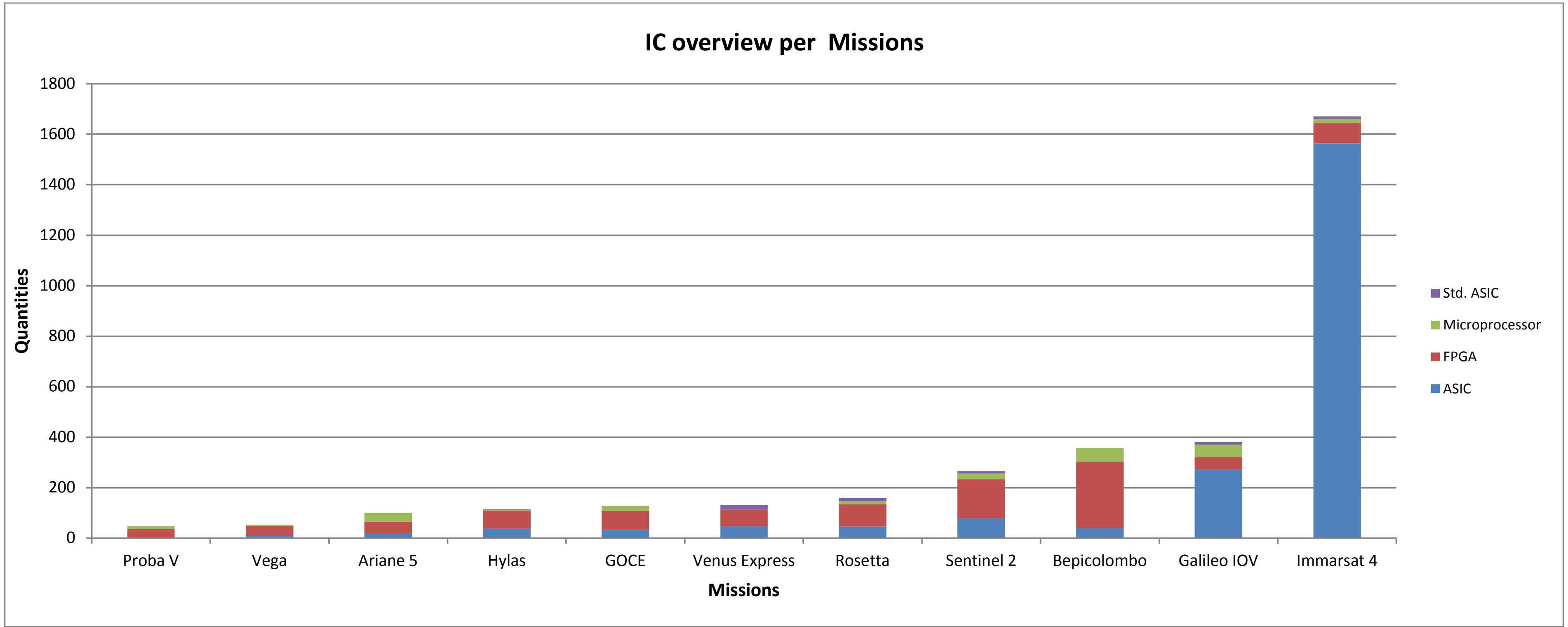

Figure 23: IC Overview per missions (Totals)

The range of AFMS quantities move from 47 (Proba V) to 381 (Galileo IOV) with the exceptional case of Immarsat 4 that uses 1671 complex integrated circuits. The large amount of ICs found in Immarsat 4 corresponds to the repetitive and massive use of ASICs for signal processing in the payload.

Exploring Sentinel 2 now as an average and representative recent particular space mission case, it is observed that this mission uses 266 complex ICs out of which around 85% of them are used in the platform and only a 15% in the payload.

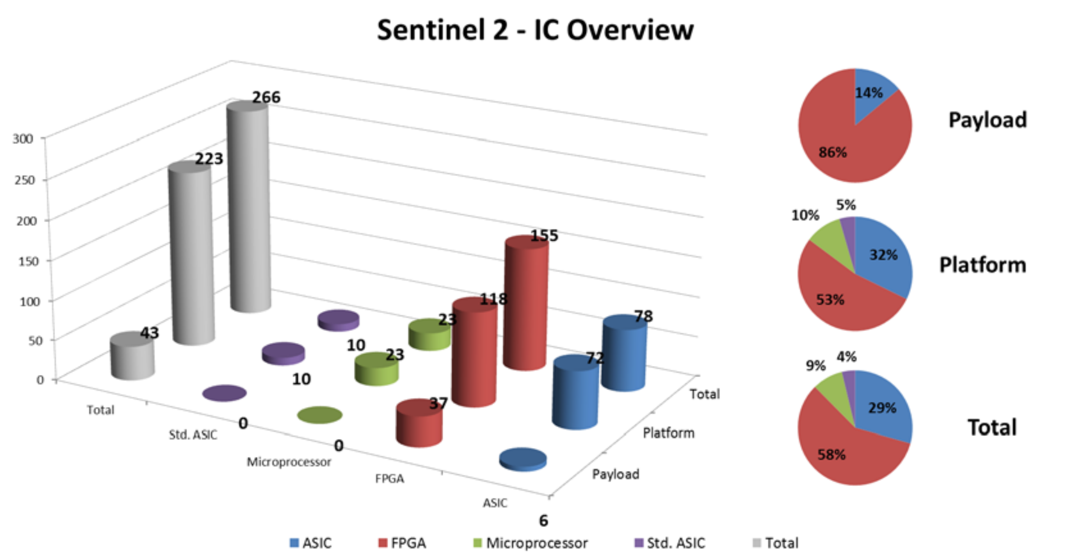

Figure 24: Sentinel 2 - IC Overview

Sentinel 2 has a wide representation of all complex integrated circuits studied in this report: ASIC, FPGA, Microprocessors and Std. ASIC. FPGA is the predominant complex IC in this satellite with a 58% of use, followed by ASIC technology (29%) and in a less percentage Microprocessors and Std. ASIC with 9% and 4% of use respectively. This distribution shows the importance in use of ASIC and FPGA technologies in space missions and the much smaller use of Microprocessors and Std. ASICs.

The fact that Microprocessors are used in small amounts does not mean that they are less important or critical to the mission. On the contrary, they perform key control functions which are fundamental to for the overall satellite operation. It is however interesting to see how many of these devices are actually used in each satellite, to help us forecast the demand for future missions to come. In Sentinel 2 (as well as in other satellites analysed in this study), there is a huge quantity of image sensors complex IC that, because they are image sensors and not signal control or signal processing integrated circuits, and due to the limited resources for making this study, they were not quantified and they have been left out of this research.

With respect to the quantities of AFMS used in the other missions included in this research, these are some particularities observed in the other missions included in the research. The missions that are not commented show similar AFMS quantities than Sentinel 2.

- **Ariane 5** and **Vega** missions, have no payload as they are launchers. For this reason, they use a smaller number of complex ICs than the other missions, 100 and 53 respectively. Vega uses smaller quantities of complex ICs than Ariane 5 because it is a lower cost launcher.
- **Proba V** mission uses the lowest number of complex ICs (47) out of which 77% are FPGAs and 23% Microprocessors. This reduced number of ICs is because Proba V is one

of the smallest satellites built by ESA with dimensions of 0,765x0,73x0,84 m. It is interesting to see how FPGAs outnumber by far ASICs in this small satellite. The performance capabilities and competitive prices of today's space FPGAs have met the requirements of this mission, and have prevailed over other considerations, as for example export regulations.

- **Galileo IOV** is a navigation satellite that uses 381 complex ICs. It is important to highlight that the 72% of the total ICs used are ASIC while only the 12 % are FPGAs. In addition, the platform uses almost only ASICs with a 97% of percentage and in the payload are shared by ASIC, FPGA and Microprocessors with approximately a third part for each (29%, 28% and 35% respectively). In this case, ESA's strong requirement to stay away from USA components export regulations and the conservative and stringent technical requirements have made of ASICs the preferred option, especially in the platform.

- **Immarsat 4** is a very singular mission as it is a large commercial telecommunication satellite built by EADS Astrium with collaboration of ESA. It uses the huge quantity of 1671 integrated circuits out of which 93% of them are ASICs located in the payload. The large arrays of ASICs in Immarsat 4 payload are used to process the dense flow of telecommunication signals. ASICs are one of the best options for telecommunication satellites payloads for their better technical features in terms of power consumption, high integration densities and timing performance.

These are the main points that can be extracted as a conclusion regarding the quantities of AFMS used in all the space missions included in this research. The percentages presented in the next points have been obtained doing the average of the percentages of all the missions include in this research.

- The quantities of complex IC used in the space missions included in this research move in a range of 50 to 400 per mission, with the exception of Immarsat than uses more than 1500.
- In average, the quantities of complex ICs used in the platform (70%) are higher than in the payload (30%), with the exception of Immarsat 4 (99% in the payload) and the launchers that only have platform.
- FPGAs are used in average in larger quantities than ASICs in the space missions included in this research with a percentage of 50% to 30%, respectively.
- Microprocessors and Std. ASICs are used in small quantities compared to ASICs and FPGAs with an average percentage of use of around 10%.

4.1.2 Programmable (FPGA) vs. Non-programmable (ASIC + Microprocessor + Std. ASIC)

This column chart shows in increasing order the percentage of FPGAs versus the Non-programmable integrated circuits used in the space missions studied in this research.

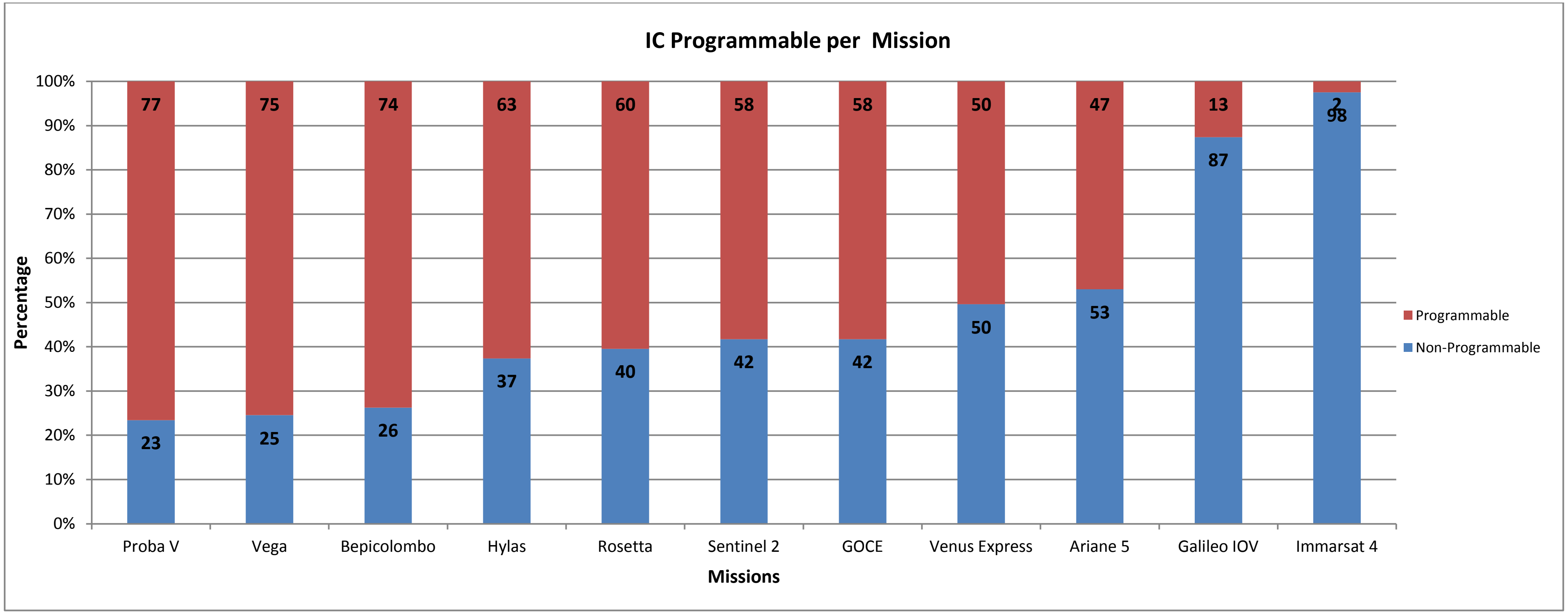

Figure 25: Programmable/Non-programmable per Missions (Percentage)

Except in Galileo IOV and Immarsat 4 missions where the percentage is very high (around 90%), in general the satellites move in a range from 25% to 50% of use of Non-programmable circuits (ASICs + Microprocessors + Std. ASICs). This means that in the time span observed from 2004 to 2014, FPGAs are used in a higher percentage (60% in average) than ASICS, Microprocessors and Std. ASIC together.

Sentinel 2 uses a slightly higher quantity of programmable components than non-programmable, 58 to 42 percentages respectively. In addition, around the 75 % of programmable complex ICs used in Sentinel 2 mission are in the platform.

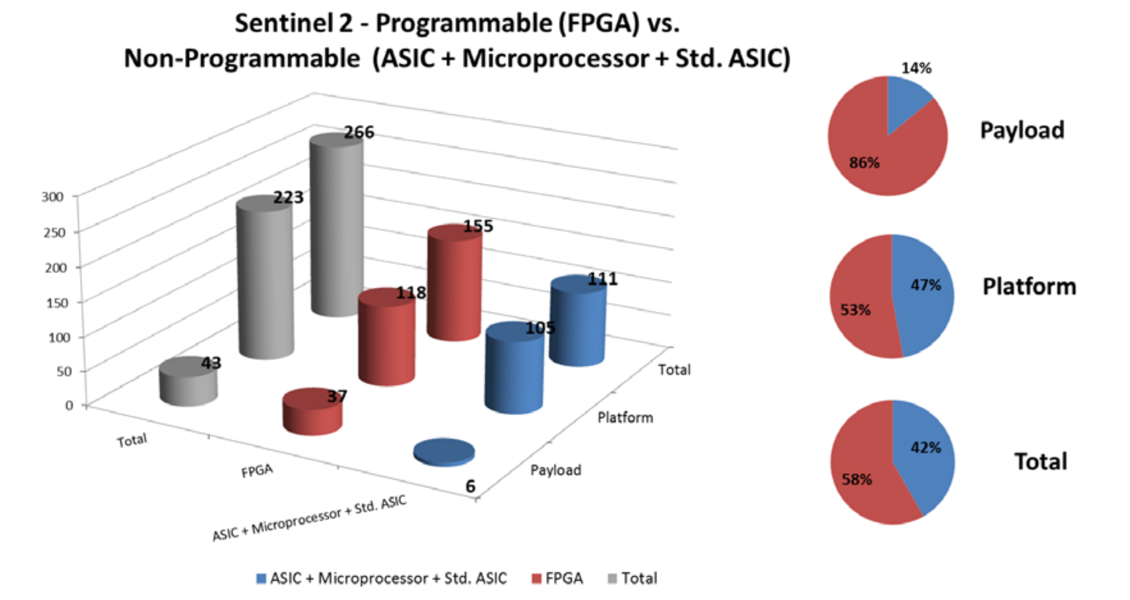

Figure 26: Sentinel 2 Programmable (FPGA) vs. Non-programmable (ASIC + Microprocessor + Std. ASIC)

Looking at the use of programmable complex ICs in the other missions included in this research the following particularities have been observed:

- **Immarsat 4** and **Galileo IOV** missions use a higher percentage of Non-programmable integrated circuits, more specifically ASICs, than the other missions studied in this research because they are Telecommunication and Navigation satellites that use large arrays of ASICs to process the data.
- **Hylas** satellite has the particularity that its entire payload is composed by programmable devices (FPGAs).

In general terms the use of programmable and non-programmable complex ICs in the space missions included in this research can be summarized in the following points:

- The percentage of use of programmable complex ICs (FPGA) move in a range from 50% to 75% in the missions studied in this research, with the exception of Immarsat 4 and Galileo IOV that uses around 90% of non-programmable components (ASIC + Microprocessors + Std. ASIC)
- In general, payload units use a higher average percentage of FPGAs (70%) than platforms units (50%).

4.1.3 Reused IC designs

This column chart shows in increasing order the percentage of the reuse of IC designs in the space missions studied in this research.

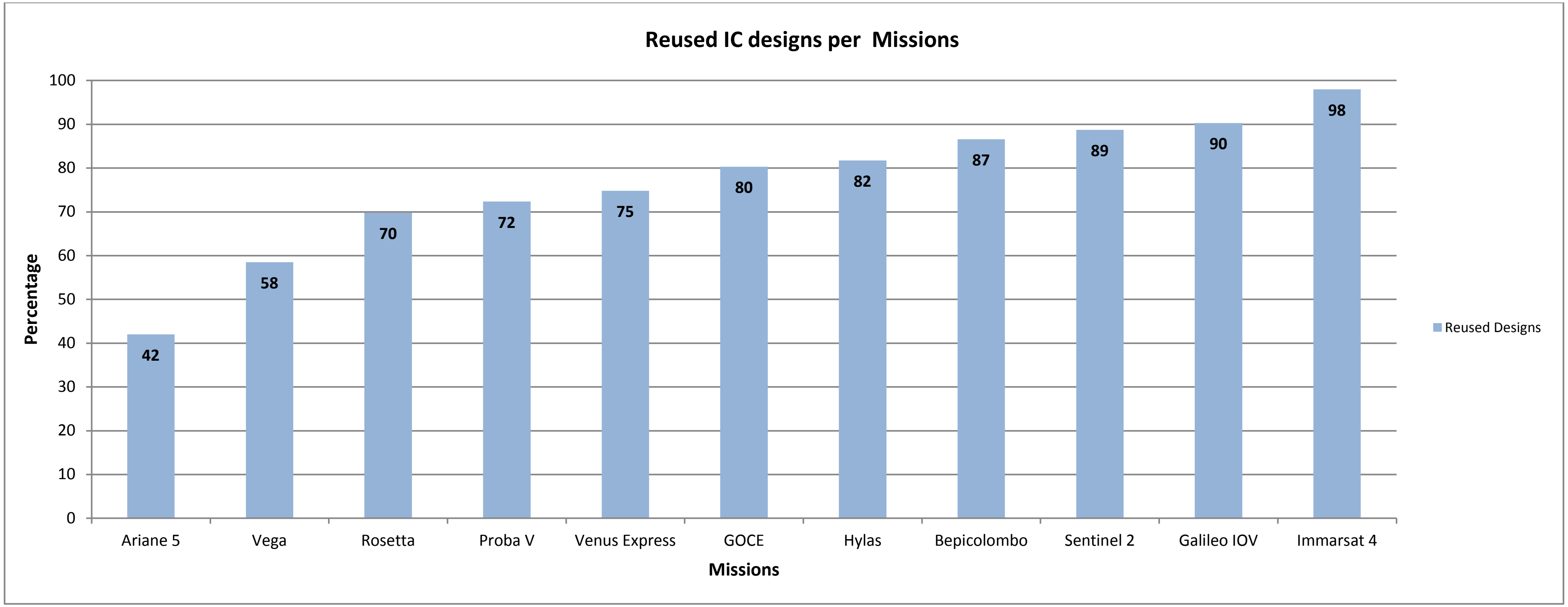

Figure 27: Reused IC designs per Missions (Percentage)

The range of reused IC designs moves from 70 % to almost 95% with an average of around 80%, with the exception of launchers (Ariane 5 and Vega) that have a lower reusability (42% and 58%, respectively). This means that for every 2 different IC designs there is an average of 8 chips that are a repeat (the same ASIC, Microprocessor or Std. ASIC, or the same FPGA with the same IC design inside)

In Sentinel 2, there is a high percentage (89%) of reused IC designs both in the Payload and the Platform, this means that from the 266 ICs counted in the mission there are only 30 different designs.

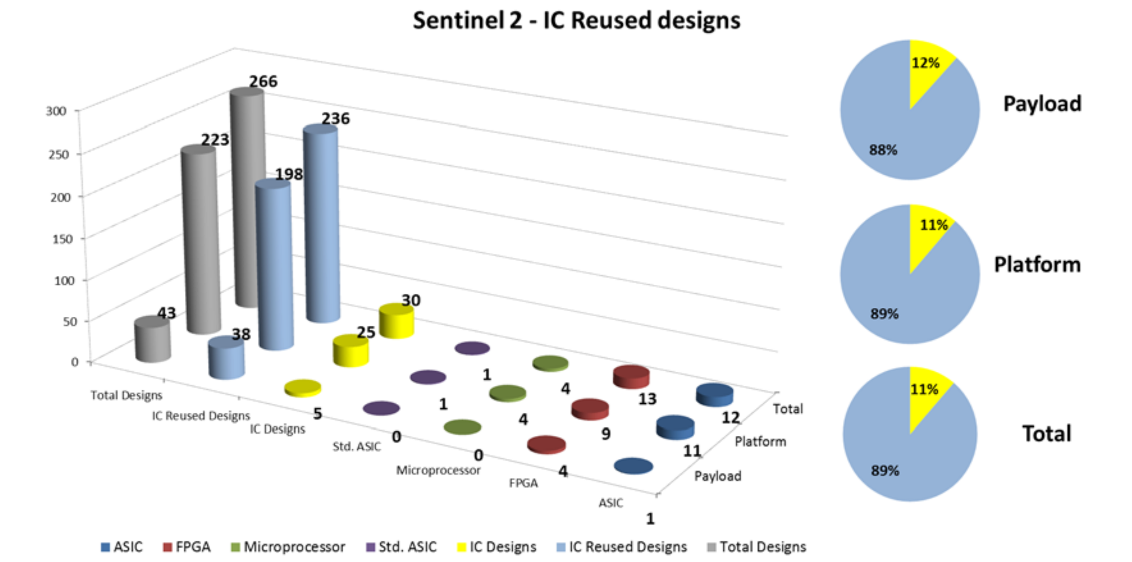

Figure 28: Sentinel 2 Reused IC designs

From the other missions included in this research it is possible to observe the following particularities with respect to the use of reused IC designs:

- **Ariane 5** and **Vega** launchers have a low percentage of reuse of IC designs, 42% and 58% respectively. That can be explained because they have only platform units and in general they do not need to repeat the same functions many times (as it is often the case in the experiments in the payloads) so they need integrated circuits with unique designs.
- **Immarsat 4** has the particularity that a very small number of ASICs are reused hundreds of times its payload. This could be explained because ASIC solution consumes less power, is more integrated and have higher performance in processing data as it has been explained before. The reason why the reusability is so high could be because global functions are processed by a large array of sub functions that are repeated many times in order to process the big amount of data in every channel.

The conclusions of the reuse of designs in complex integrated circuits observed in the space missions included in this research can be summarised in the following points:

- The percentage of reuse of complex IC designs in the space missions included in this research move in a range of 70 to 95 percentage with an average of 80%, with the exception of the launchers Ariane 5 and Vega, with a percentage of 42% and 58% respectively. This high percentage can be due to the approach of subdividing complex global functions (for the entire platform or payload) of data handling and signal processing into smaller functions (e.g. per time or space channel, per beam, etc.) that then are repeated and interconnected in order to achieve the total functions at satellite level

4.1.4 IC Technology vendor country

This column chart shows in increasing order the percentage of complex ICs provided by US vendors used in the space missions studied in this research.

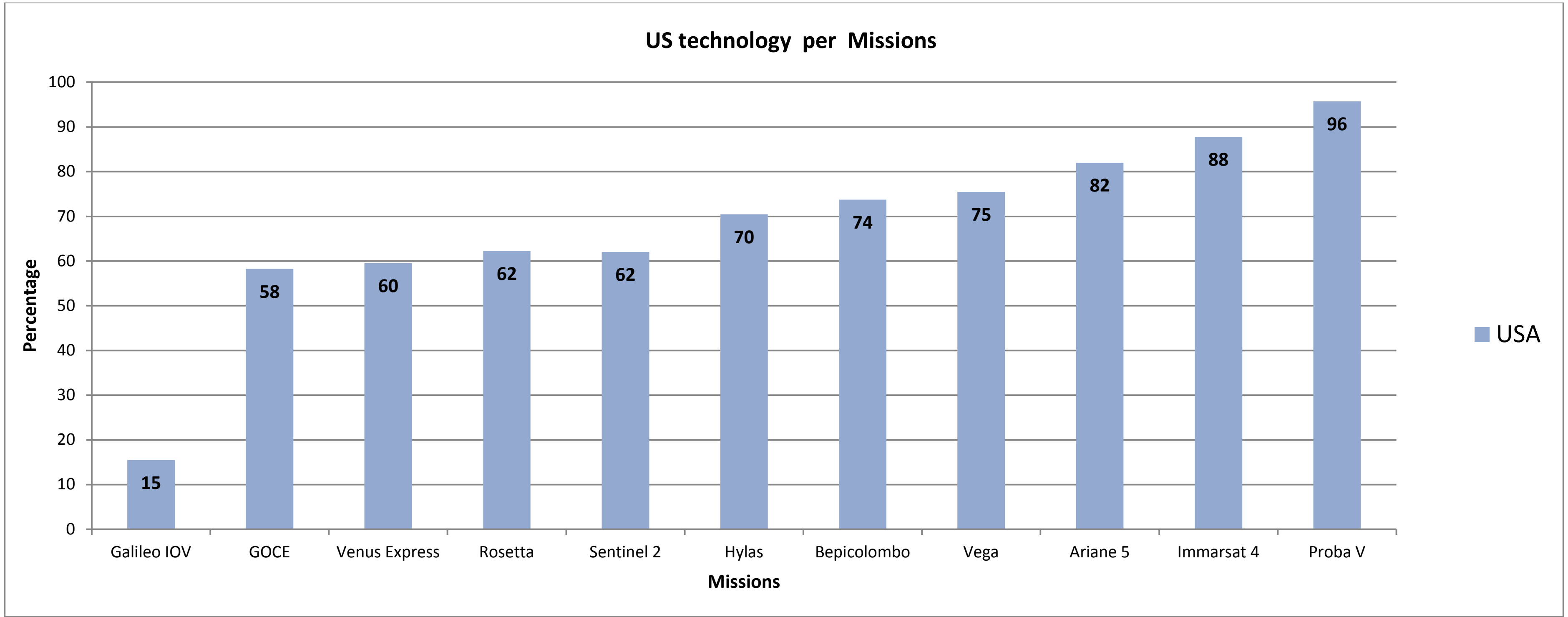

Figure 29: IC Technology vendor per Missions (Percentage)

There is big dependence on US technology in the European space missions included in this study with a range from the 60% to almost 95% of its complex integrated circuits provided by US vendors. The only exception is Galileo IOV as it was defined as a European key mission so there was a big effort to try to use only European technology and components.

In Sentinel 2 all ASICs and Microprocessors used in the satellite are supplied by Europe vendors while FPGAs and Std. ASIC are based in US technology. It is important to highlight that France is the main vendor country in Europe with a 90 % of ASICs and a 100% of Microprocessors.

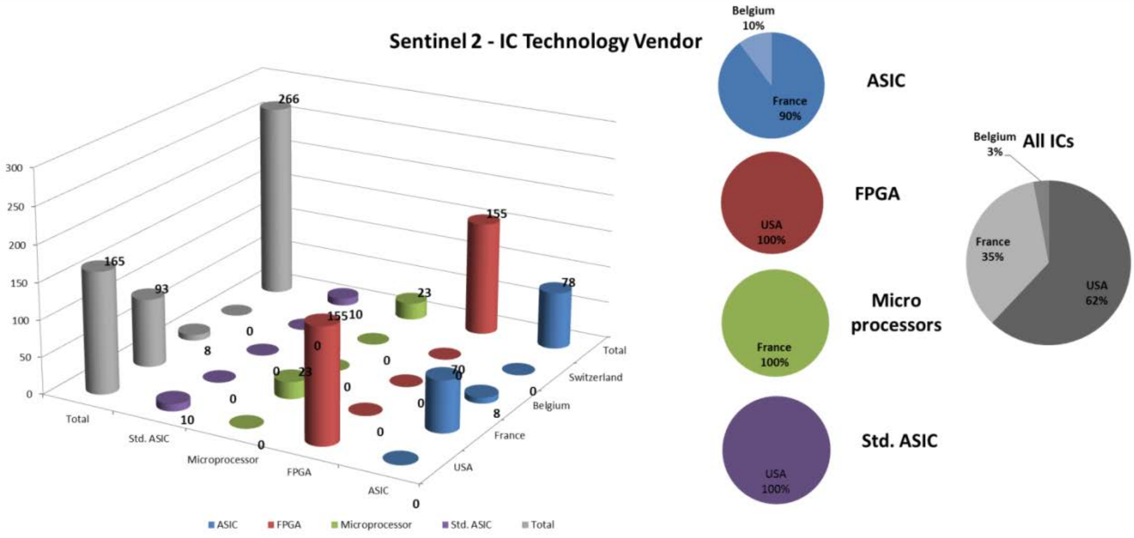

Figure 30: Sentinel 2 IC Technology vendor country

The total distribution of complex ICs pie shows that the percentage of US components (62%) is higher than European components (38%) and it can be explained by the predominance of FPGAs in this space mission which is all supplied by a US vendor.

The particularities observed in other missions are explained in the next points:

- **Galileo IOV** uses a very small quantity of US components compare to the other mission studied in this research, only 15%, because it is a key European navigation mission and a big effort was done to reduce its dependency to the American technology. In this satellite, the 74% of the complex ICs are supplied by France, 24% by USA and 2% by Austria.
- **Hylas** mission uses and important percentage of complex ICs provided by UK vendors (30%) and the rest of components come from USA. This is interesting because in general the European complex ICs used in these space missions come from France and very small number from other countries like Sweden or UK in this case.

In general terms the use of US and European complex IC technology in the space missions included in this research can be summarized in the following points:

- USA is dominant in the space complex IC market and a range of 60% to 90 % of the total ICs used in the European space missions included in this research are provided by USA vendors. This means a big dependence of Europe from USA technology and ITAR restrictions. Even though Europe is making efforts to reduce this dependence, the graphs show that USA components use is increasing. Galileo IOV is the only exception with only 15% of USA integrated circuits.

- FPGA technology is generally provided by US vendors, ASIC by European vendors and Microprocessors and Std. ASIC is shared in different percentage depending on the space mission.
- The most important European complex IC supplier is established in France but in some mission there are ASICs and Microprocessors provided by vendors in UK or Sweden.

4.2 Trends and patterns of use of AFMS in space missions

The aim of this chapter is to explore to which extent the quantities of AFMS used in the space missions included in this research and their technical parameters are influenced (or not) or follow any obvious trends or patterns when observing certain mission characteristics such as the launch date, lifetime, mass, cost, space programme or satellite orbit. Former chapter 3.3 explains the methodology applied to explore the data and get to the results that are now presented in this chapter.

It is important to note that the trends and patterns displayed in this chapter are not statistically significant due to the relatively small number of cases studied and the high dispersion and noise of the data. In consequence, the p-value is lower than a predetermined significance level, but this does not mean that the effects described have no practical significance[32], and can be used to support decisions In the policy management field.

According to Roger E. Kirk, statistical significance is concerned with whether a research result is due to chance or sampling variability and practical significance is concerned with whether the result is useful in the real world[33]. The substantive or practical significance has nothing to do with the p-value and everything to do with the estimated effect size. Only knowing about the context of the results, it will be possible to interpret its meaning and so speak to the substantive significance of the results [34]

The coefficient of determination (R^2) which indicates the fraction of the total variance in the dependent variable that is explained by the model ([35], has been used to make a diagnostic how well future outcomes are likely to be predicted by the. In conclusion, it is important to highlight that all the trend lines displayed in this research are hypotheses for future growth that are not substantiated by the data exploration.

In order to maximise the practical significance of any observed trends or patterns, it was decided to eliminate the huge data dispersion that some few exceptional cases would bring into some of the charts. This is why the data from Immarsat 4 and the launchers (Ariane 5 and Vega) has been omitted in the X-Y charts.

Immarsat 4 is a very particular commercial telecommunications satellite with a huge quantity (more than 1500) of ASICs in the payload. In the case of the launchers, they have been omitted because their cost, mass and lifetime is not comparable to other satellites. However, and even if they do not appear in the graphs, their data will be commented and analysed when it is considered as valuable and of practical significance for the research results.

In conclusion, the trends and patterns observed in this research are not statistically significant but they can be practically significant as they are useful for ESA technology policy managers to have more information and visibility on the evolution of the use of complex ICs in European space missions.

4.2.1 Trends of use of AFMS technologies in space missions in the timeline

a) IC overview vs. Launch date:

This is one of the most important graphs of this study because it shows the evolution of use of ASIC, FPGA, Microprocessor and Std. ASIC in the timeline (from 2004 to 2014) from the space missions included in this research.

Totals:

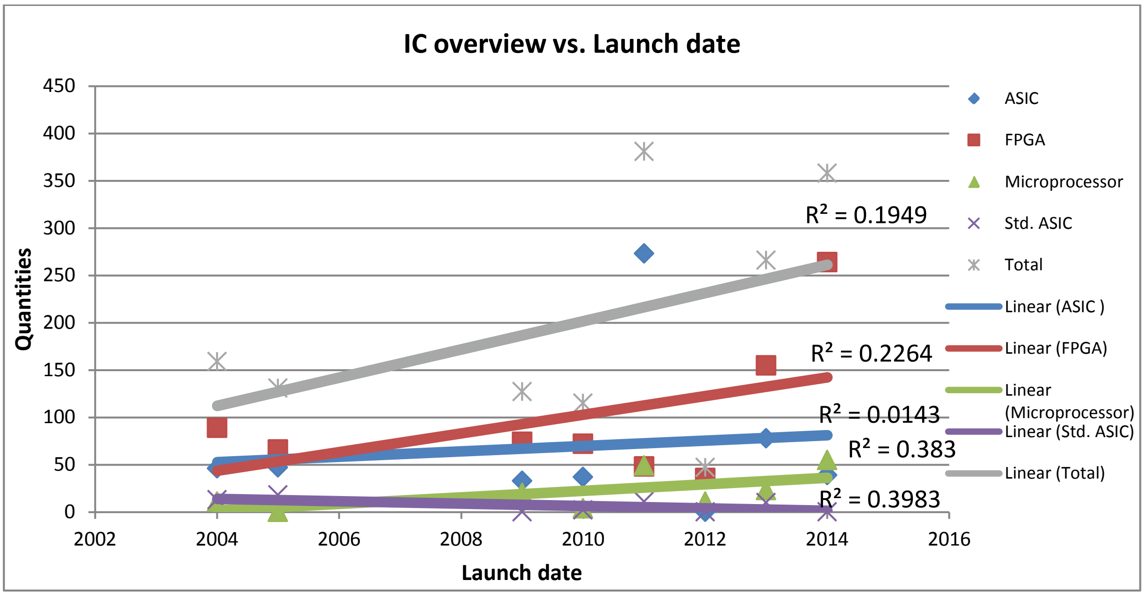

Figure 31: IC Overview vs. Launch date (Totals)

The data represented in this chart shows that the total amount of complex integrated circuits used in these European satellites has been increasing in the last years, and very likely will continue to grow in the future. More specifically, it shows that FPGAs are the integrated circuits used in largest quantities in these space missions and the ones which may have a stronger growth in terms of use.

ASICs might be also growing in time but not as much as FPGAs and they seem to be now in second position of use behind the programmable components. Microprocessor and Std. ASIC are used in much lower quantities than ASICs and FPGAs and it is difficult to appreciate if its usage has been increasing or decreasing in the last years.

These trends show that FPGA technology is increasingly taking a larger of the complex IC technology used in the space sector in the last years, in detriment of the ASIC market (with exceptional cases)as it can be better observed in the following percentage chart:

Percentage:

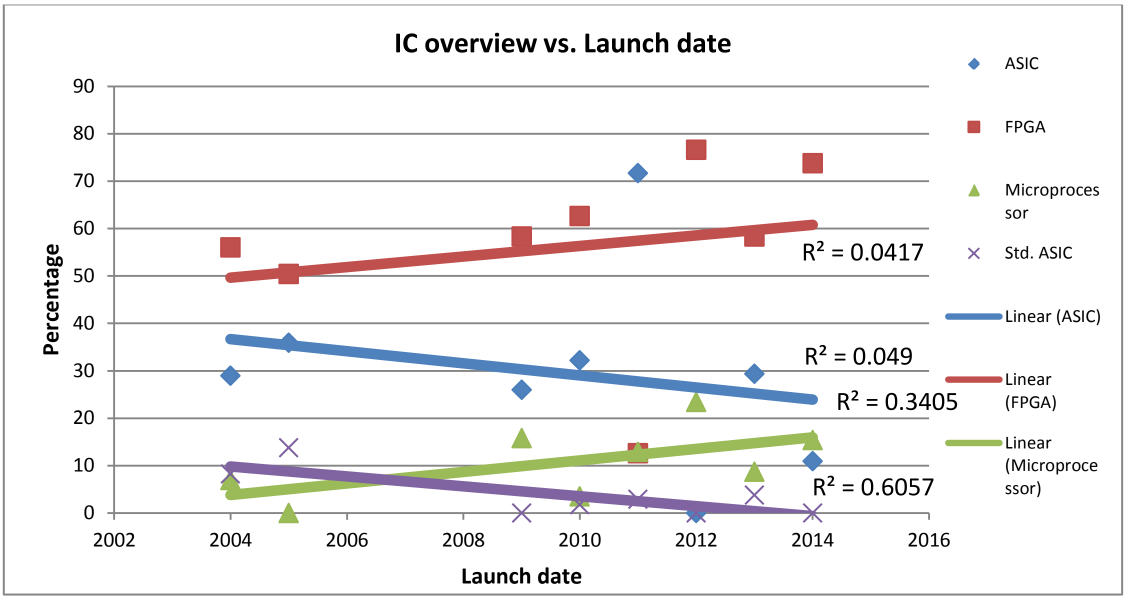

Figure 32: IC Overview vs. Launch date (Percentage)

In addition, exploring the evolution of use of complex integrated circuits by establishing groups of missions according to their overall cost shows that high cost missions (above 800 MEUR) sometimes have a higher percentage of use of ASICs than FPGAs. This could be explained because space missions with higher budgets can afford to spend more in developing customized and more expensive complex integrated circuits (ASICs).

In the chart below, it is shown the 5 space missions of this study sample (Ariane 5, Rosetta, Immarsat 4, Galileo IOV and Bepicolombo) that fall into this category of “high cost” missions. The space missions that use larger quantities of ASICs than FPGAs are Immarsat 4 and Galileo IOV.

High cost:

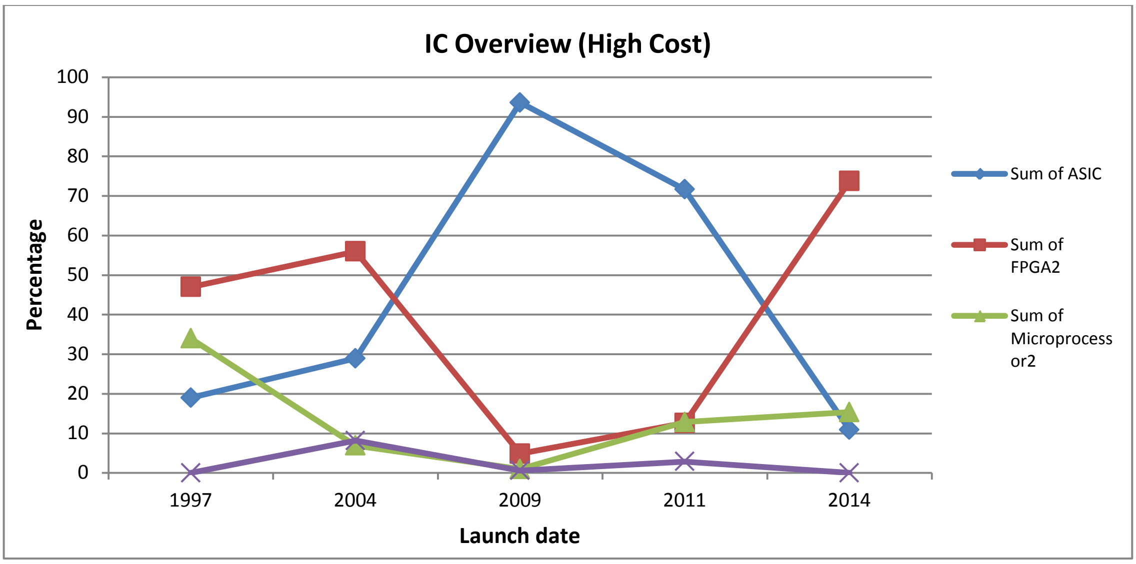

Figure 33: IC Overview - High cost (Percentage)

b) Programmable/Non-programmable vs. Launch date:

The graph below shows the percentage of use of programmable (FPGA) versus Non-programmable (ASIC + Microprocessor + Std. ASIC) in the timeline (from 2004 to 2014) from the space missions included in this research.

Percentage:

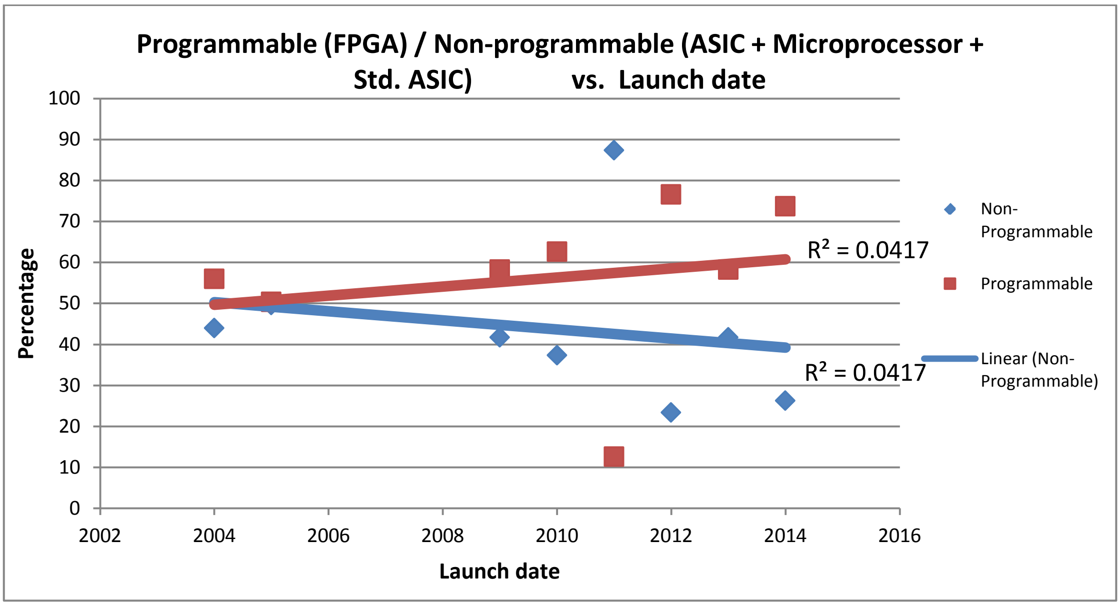

Figure 34: Programmable/Non-programmable vs. Launch date (Percentage)

The trends of this graph shows that 10 years ago programmable and non-programmable components were used in a similar percentage (around 50%) while in the last years programmable ICs are taking market share to non-programmable with a today's average percentage of FPGA around 60% in front the 40% average of ASIC, Microprocessors and Std. ASICs together. Again, these are trends of practical, rather than statistical significance, given the relatively small sample of missions´ data gathered for the analysis.

The following graph shows a different way to present the same figures of number of FPGAs and number of ASICs (including microprocessors and standard ASICs) as above, but indicating also the missions from which the numbers were taken, and giving absolute qualtities of parts procured for each mission, as reflected in the mission DCLs.

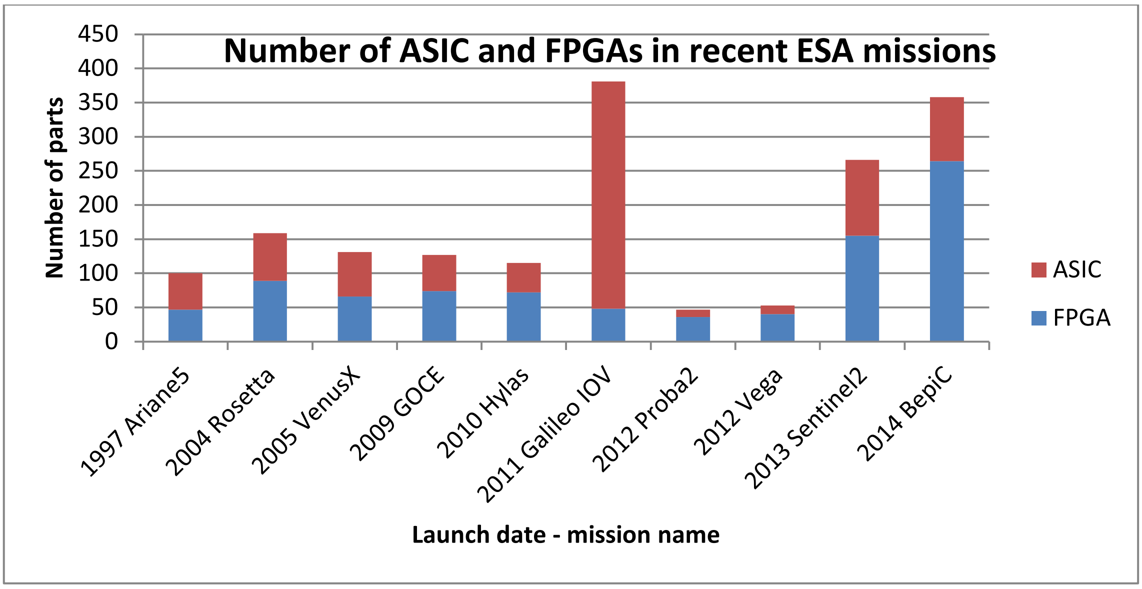

Figure 35 Programmable/Non-programmable vs. Launch date with mission source (Absolute quantities)

c) **Reused IC designs vs. Launch date:**

The graph below shows the total quantities of the reuse of IC designs in the timeline (from 2004 to 2014) from the space missions included in this research.

Totals:

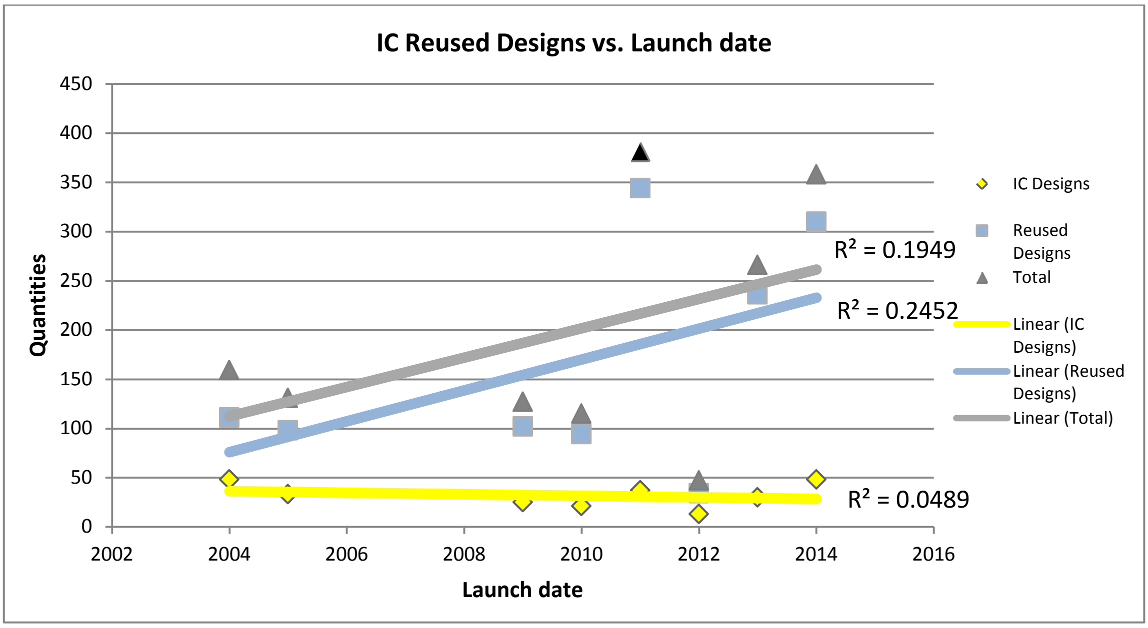

Figure 36: Reused IC designs vs. Launch date (Totals)

This chart shows that the quantities of IC designs that are reused (repeated) inside the space missions seem to be increasing in the timeline. It is interesting to see that the number of different IC designs used in the satellites remains stable (yellow points) while the repeated use of those designs seems to be increasing in the timeline (blue points). Again, more data from more missions would be needed to give statistical significance and credibility to this conclusion.

d) IC Technology vendor country vs. Launch date:

This graph shows the evolution of the use of complex IC technology indicating the countries of the vendor that provide the IC technology.

Totals:

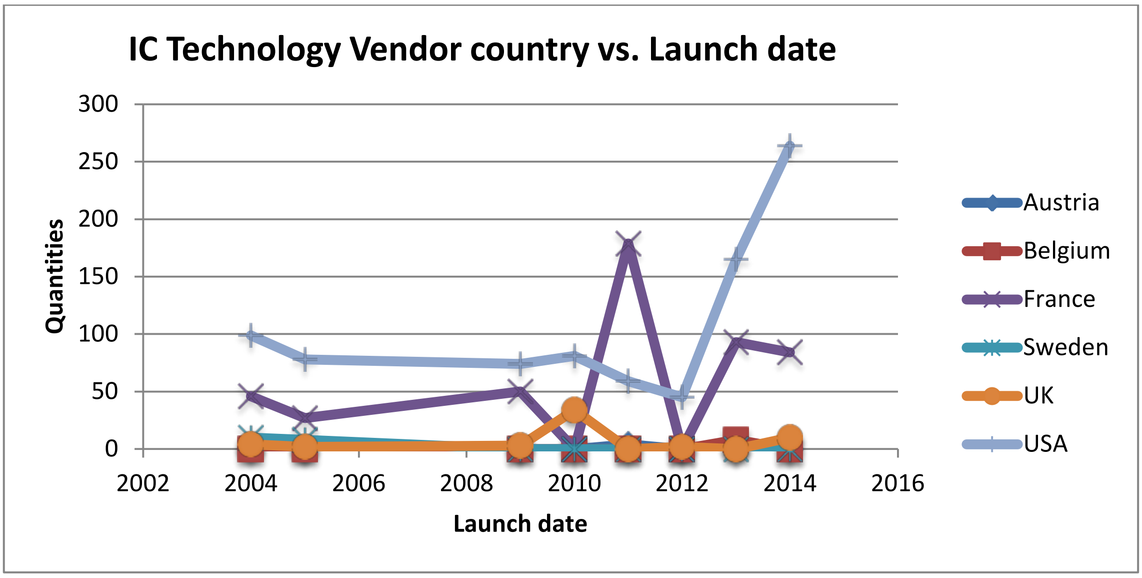

Figure 37: IC Technology vendor vs. Launch date (Totals)

In general, complex integrated circuits provided by USA vendors are predominant in the European space missions included in this research confirming that USA IC technology has a big influence in the European space sector.

Another clear observation is that France is the country that provides most of the European complex integrated circuits come from at a big distance from the other European IC vendors like UK, Sweden, Belgium and Austria.

The chart also shows that the three satellites subject of this study that will be launched between 2012 and 2014 (Proba V, Sentinel 2 and Bepicolombo) use high quantities of complex ICs from USA vendors. This data, though not statistically significant, shows practical evidence that dependency in US technology for complex ICs is a reality for some of the most recent ESA missions, and very likely a trend to continue unless European technology space programmes (see chapter 2.2.3) start to produce alternatives.

4.2.2 Patterns of use of AFMS in space missions with respect to the mission lifetime

a) IC Overview vs. Lifetime:

This graph shows the relation between the use of AFMS in the space missions include in this research (except Immarsat 4, Ariane 5 and Vega) with respect to the lifetime of the satellites.

Percentage:

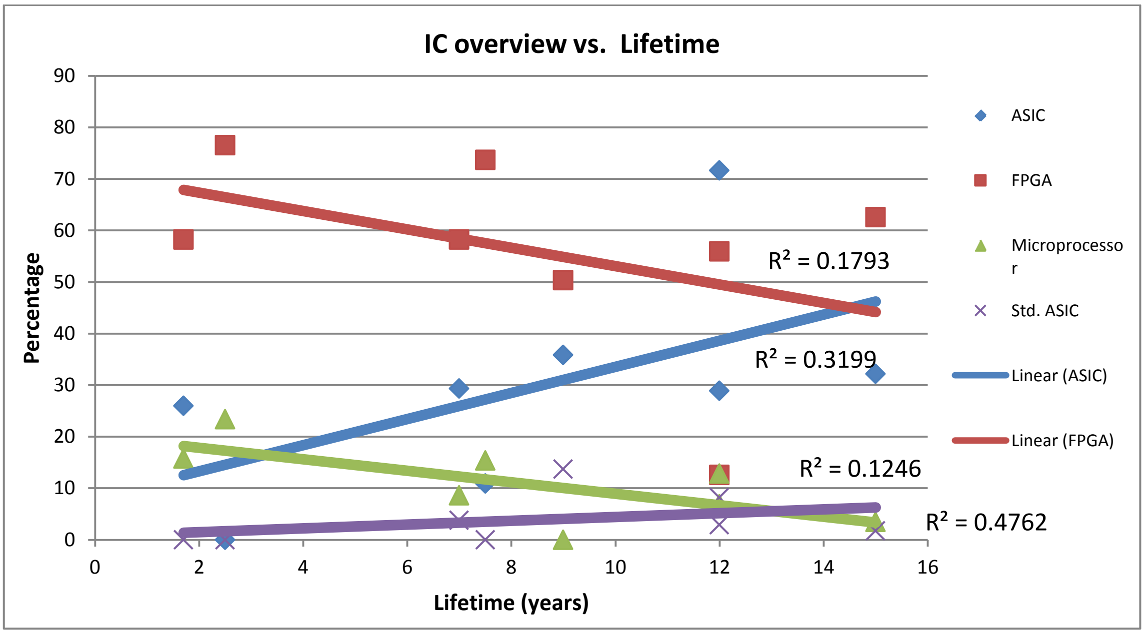

Figure 38: IC Overview vs. Lifetime (Percentage)

As relatively soft trends observed in this graph we see that missions with longer duration seem to use more ASICs (and fewer FPGAs and Microprocessors) than missions with shorter duration.

Possible explanations behind these patterns could be that ASIC technology, on average, are chosen as highly reliable, high performance devices which the designer and final customers can control, customise and adapt (at least to a larger extent than what FPGAs and other off-the-shelf devices can be adapted to) to the actual mission´s quality and technical requirements. Longer mission lifetimes is often associated to Telecommunication and deep space missions, often associated with larger mission costs and budgets, and therefore, missions that can afford more expensive IC solutions, as ASICs normally are.

As it was said before, Immarsat 4 is not represented in this figure but it somehow reinforces the pattern observed as it is a satellite with a lifetime of 13 years and a percentage of 93% of ASIC use.

4.2.3 Patterns of use of AFMS in space missions with respect to the mission overall cost

a) IC Overview vs. Cost:

This graph shows the relation between the use of AFMS in the space missions include in this research with respect to the overall cost of the satellites.

Percentage:

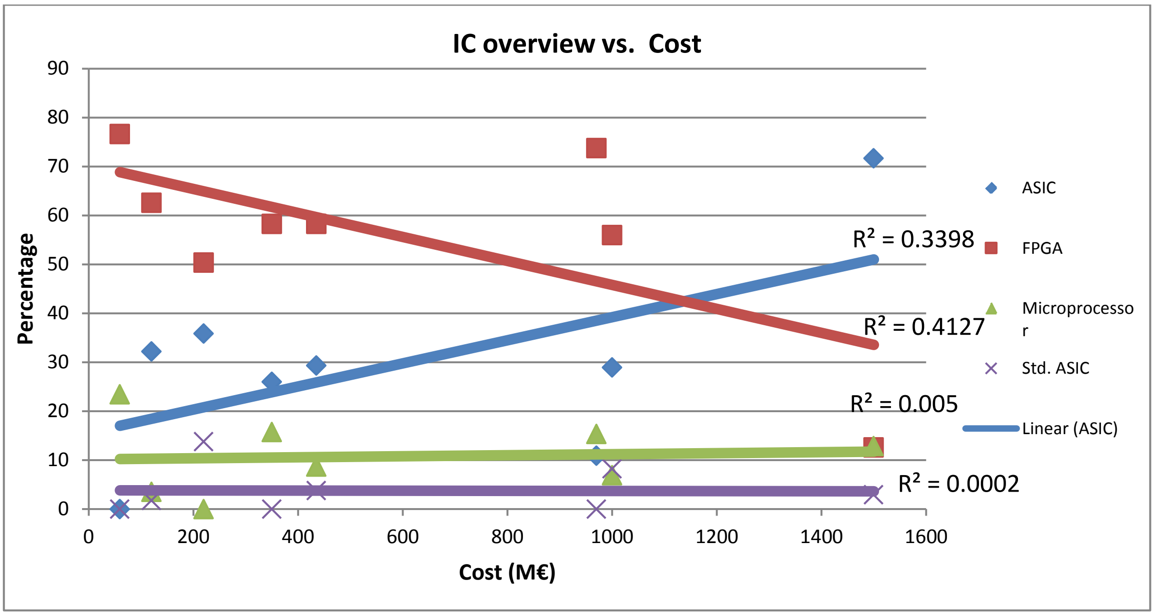

Figure 39: IC Overview vs. Cost (Percentage)

There is a possible soft trend in this graph that shows that when the cost of a mission increases the use of ASICs also grows while the use of FPGAs decreases. One of the reasons to explain this trend could be that space missions with a reduced budget tend to use more FPGAs as they are cheaper (on average, and certainly when used in low volumes, than ASICs).

These results are in line with the ones described above in chapter 4.2.2. In any case, this soft trend is not substantiated by enough statistical evidence, and more data from more missions would help to see if there really is a pattern associated to mission lifetime and choices of complex ICs.

4.2.4 Patterns of use of AFMS in space missions with respect to the satellite mass

a) IC Overview vs. Mass:

This graph shows the relation between the use of AFMS in the space missions include in this research with respect to the satellite mass.

Percentage:

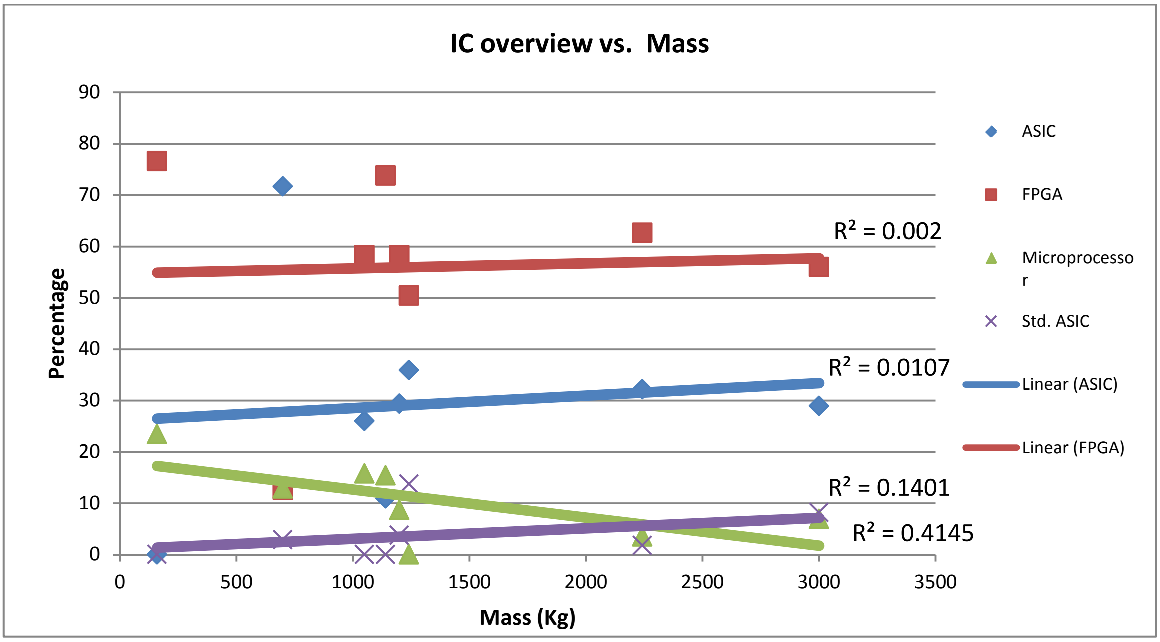

Figure 40: IC Overview vs. Mass (Percentage)

Looking at this graph it is difficult to see any particular trend and it is possible to conclude that there is no special relation between the mass of a satellite and the use of different types of integrated circuits, at least not for the mission sample subject of this study.

4.2.5 Patterns of use of AFMS in space missions with respect to the space programmes

This graph shows the average quantities of different types of complex ICs used in the 11 space missions included in this research by space programme. The number below the programme name gives the quantity of missions per group analysed, which, again, is not statistically significant.

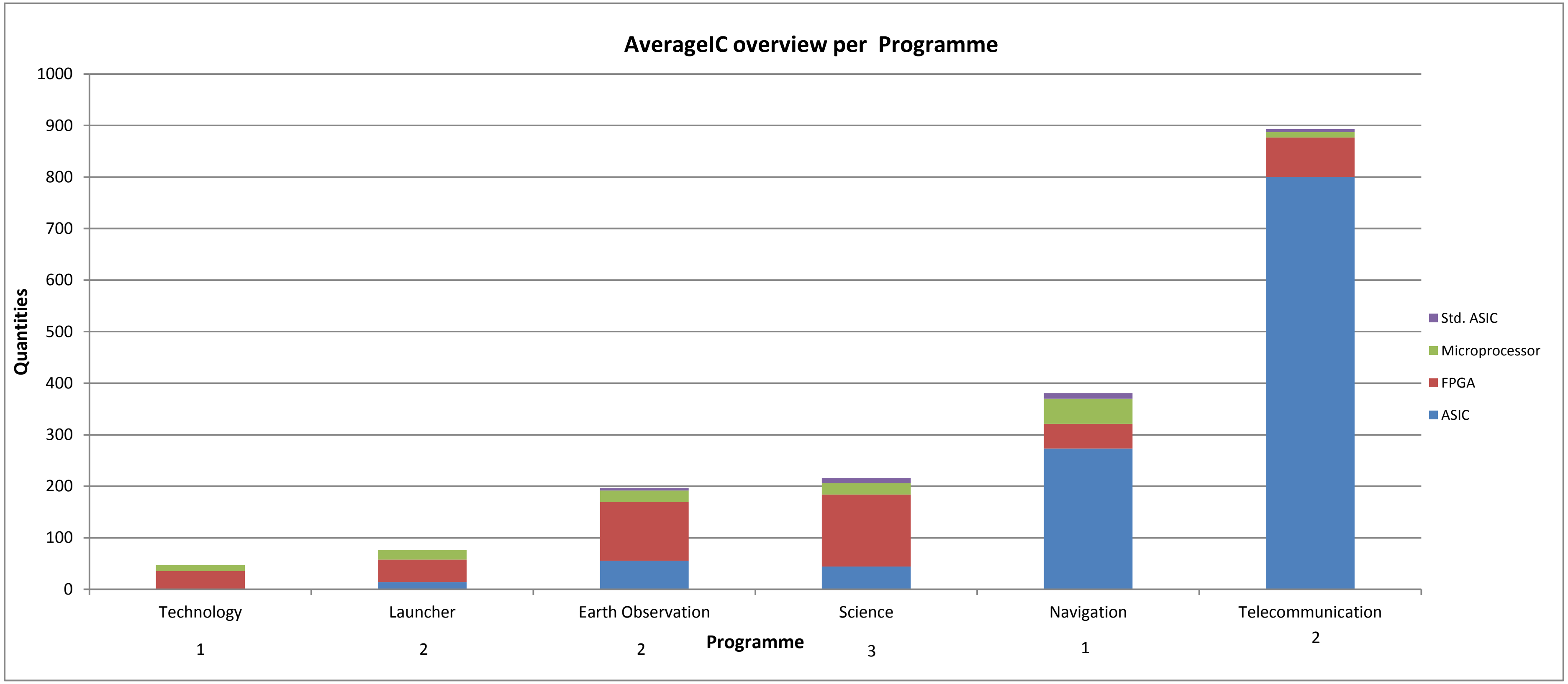

Figure 41: IC Overview per Programme (Totals)

As a result, it can be said that telecommunications and navigation space missions use the largest quantities of integrated circuits (400 to 1500) and the largest percentage of ICs being ASICs. For Earth Observation and Science missions the number of ICs used is around 200 and have similar ASIC-FPGA proportionality (25%-75%). Launchers use relatively low quantities of complex ICs (compared to the other mission classes) because they have no payload. Lastly, the so-called Technology missions are typically the smallest ones, and that already justifies the very few complex ICs inside, being their main objective to prove new technologies (in general, not only IC) in space. In the three missions analysed, and possibly true for other cases in these mission categories, Launchers and Technology spacecraft seem to use less than 100 complex ICs per spacecraft.

4.2.6 Patterns of use of AFMS in space missions with respect to the satellite orbit

This graph shows the average quantities of complex ICs used in the space missions included in this research by satellite orbit. The number below the columns gives the quantity of missions per group analysed.

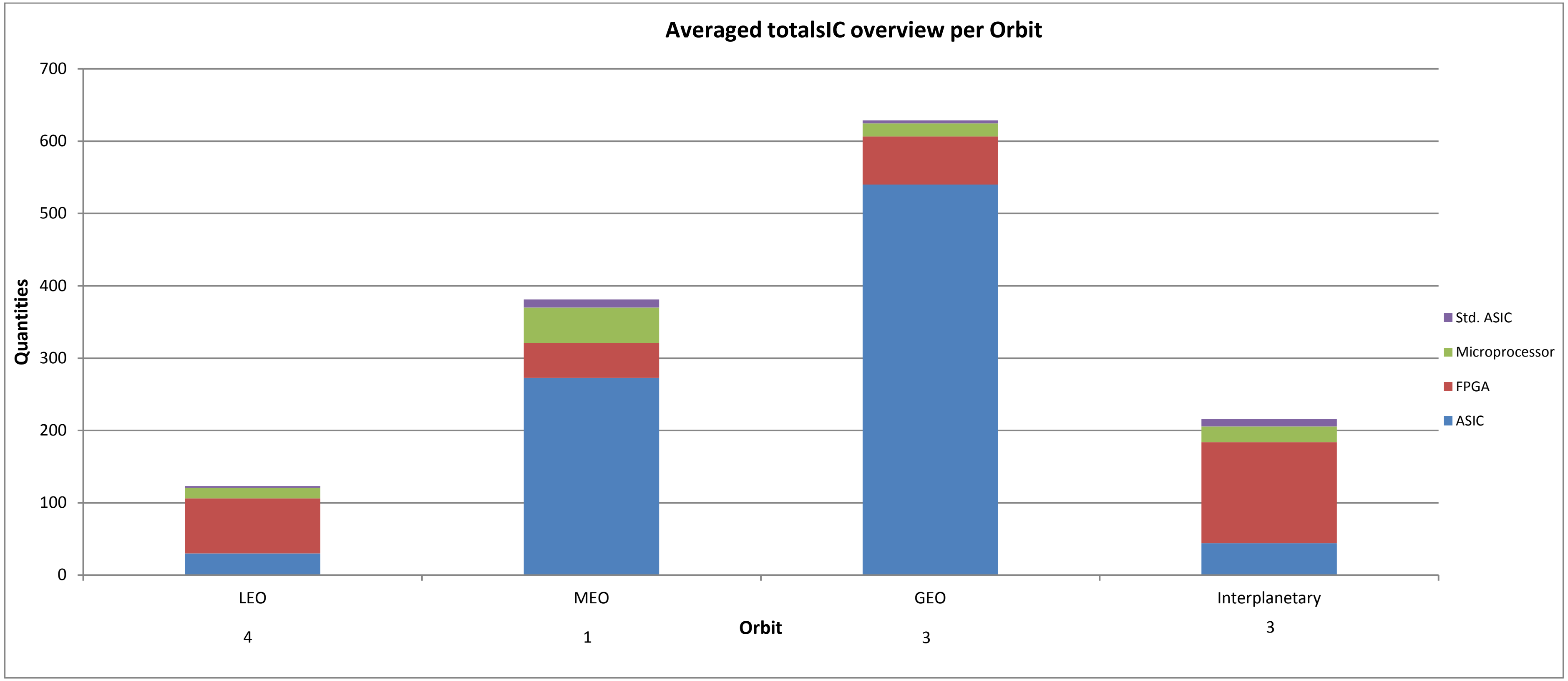

Figure 42: IC Overview per Orbit (Totals)

The IC Overview per Orbit chart shows that the farther is the distance from Earth of an orbit, the larger the quantities of complex integrated circuits that seem to be used, on average. This can be explained because Telecommunication and Navigation missions are located in MEO and GEO orbits while Earth Observation and Technology mission tend to be in LEO orbits. It is also observed that interplanetary orbit missions seem to use, on average, a smaller amount of complex ICs, and a larger percentage of FPGAs than ASICs, while the average number of Microprocessors and Std. ASIC does not seem to fluctuate much when comparing the mission orbits.

5 VALIDATION OF RESEARCH RESULTS

Research validity can be broadly defined as the level of confidence that can be taken with regard to the truth of a particular research. Campbell distinguished among four types of validity, which can be explained in a concise manner by looking at the questions underlying the four types[37]:

- **Statistical conclusion validity:** is there a relationship between the two variables?
- **Internal validity:** given that there is a relationship, is it plausibly causal from one operational variable to another?
- **Construct validity:** given that the relationship is plausibly causal, what are the particular cause and effects constructs involved in the relationship?
- **External validity:** given that there is probably a causal relationship from construct A to construct B, how generalizable is this relationship across persons, settings and times?

This chapter will try to validate the results obtained in this research by answering these four types of validity adapted to the particularities of this research.

5.1 Statistical conclusion validity

According to[37], statistical conclusion validity refers to the appropriate use of statistics to infer whether the presumed independent and dependent variables covary.

As explained above in the Results (see chapter 4.2), the trends and patterns investigated in this research are not statistically significant due to the small number of samples explored, in this case 8 space missions, and the high dispersion and noise of the data.

The "coefficient of determination", R^2, has been used to assess how well the statistical model, in this case the regression lines, explains and fits the data explored. This coefficient indicates the fraction of the total variance in the dependent variable that is explained by the model ([35]. In the simple linear regression, the coefficient of determination ranges from 0 to 1; R^2 of 1 indicates that the regression line perfectly fits the data. The R^2 observed in the exploration of this research moves from the 0,0002 to 0,6057 (see graphs in chapter 4.2).

The trends and patterns of this research are not statistically significant and they are used as hypotheses of what could be the trend of growth in the future of the use of AFMS technologies. The low statistical significance of the research results is also due to the small number of missions used to infer trends. The initial target was to explore and extract data from around 17 missions. However, due to the limited research time and after further omitting Immarsat 4 and the two launcher missions in the regressions to prevent even higher dispersion of the data, the final number of missions used in the trend analyses was reduced to 8 missions.

However, the results presented in this study can have practical significance as they can be used to support decisions in the policy management field, and more concretely in the selection and decision processes of the technology programmes where new technology development activities are defined, proposed and eventually approved and implemented.

5.2 Internal validity

Internal validity is the validity of causal inferences in scientific studies, usually based on experiments as experimental validity. Applied to this research it is explained what is the confidence in the data collected and what are the assumptions and possible errors made during the research.

The main possible errors and mistakes done in this research can be focused in the Data collection process (see chapter 3.2) where the confidence in the data collected is discussed in the next points:

a) DCL collection

In this phase of the data collection process, there are some procedures used to obtain the documents that could cause some errors or gaps.

For example, there is no certainty that all the Declared Component Lists (DCLs) from a mission have been collected. As explained before (see chapter 5.1.3), there are consolidated DCLs that integrate all the DCLs of a mission, but in other it is necessary to collect the DCLs of all the units in a mission one by one.

The confidence in having reached completeness in collecting the data relied in:

- Cross-checking that the DCLs for all the mission units (as described in each mission's ESA intranet website) have been collected in as much as possible or available
- Ensuring with the relevant mission PA managers that those DCLs were indeed the last versions available

b) DCL exploration

When exploring and extracting the information from the Declared Component Lists, there are some errors and mistakes that can be done.

It can happen that while using the "AFMS search algorithm" (described in chapter 3.2.3) in the DCL some components that should be identified as AFMS in the DCL lists are not properly identified. This could happen because the characteristics of the component are not well specified in the DCL or because there has been a human error reading the document (the AFMS algorithm is applied by reading) or because the DCL was incomplete or contained some mistakes.

The confidence in the DCL data extraction completeness and accuracy was enhanced by several independent revisions (second readings and visual inspections) of anomalies (reading or writing mistakes, spotting erroneous information) in the Excel AFMS database (and the resulting graphs) done by experts in the microelectronics section. In addition, some of the apparently incomplete or mistaken information was cross-checked against existing ASIC and FPGA databases[38]; [39] created and maintained by the Microelectronics section, independently from the DCL originators.

Based on the experience detecting missing or erroneous information during these independent reviews, and granting a reasonably high trust to the component experts who created and validated the DCLs, it is estimated that the number of components that could have been missed when extracting them from the DCLs and transferring them to our research excel AFMS database could be around 5% or 10%.

The field “quantity” in the DCLs is another parameter that needed special attention because it is information which is not mandatorily requested (by ESA) and therefore always included in the DCLs. In addition, and even if the quantity of the components was given in the DCL, sometimes in the DCLs there was no field description of the “quantity” information meant, which means that it is not possible to know what that quantity makes exactly reference to:

- the total quantity of parts procured for the development of the unit (prototypes and final flight units) or
- the quantity used per unit in one Flight Model (parts that are actually flying) or
- the actual quantities used plus the attrition (spares).

In most cases however it has been assumed, except in the cases that this information was otherwise explicitly stated in the DCL, that the quantities that appear in these documents make reference to the total quantities used per unit on-board the satellite.

In several cases (e.g. Bepicolombo, GOCE, Galileo IOV, Sentinel 2 and Proba V) the quantity information has been ascertained directly with ESA engineers who have been involved in the technical supervision of the developments of the units, and had access to architectural documents (or simply remembered) how many complex ICs were present in the unit in question.

c) Data completion

During this phase it is important to remember that most of the information received to complete the database comes from engineers involved in the design or the procurement of the components and the units and systems where they are hosted. They know the information of the quantities used or the technical parameters using their memory or reaching to architectural design documents (when available) that sometimes contain the additional details needed.

Sometimes, the additional information was collected by phone calls or informal interviews which could lead to misunderstandings in collecting the data correctly. The use of a few internal databases maintained by the Microelectronics Section at ESA[38],[39] was very useful when trying to ascertain the nature and some of the missing technical characteristics of some of the complex ICs found in the DCLs.

5.3 Content validity

Content validity refers to the extent to which a measure represents the variable that wants to be measured. In this research it will be checked how the indicators used to measure and respond the research questions are suitable or not and in what extent the data collected is reliable.

The indicators chosen to explore the quantities and types of AFMS used in space mission can be checked from three different points of view, where the research scope was in some cases narrowed (for the types of ICs and its quantities) and in other widened (for the types of missions) in order to, among other things, maximize the overall research and content validity:

a) Which quantities

The quantity indicator chosen to be studied in this research is the total quantity per component used on-board the satellite.

However, the total quantity of complex IC procured per mission, including attrition and spares of all the initial prototypes and engineering models, was another interesting indicator to be explored as it gives information about the potential market volume of these components in the space sector and can be used to anticipate customer demand and, for example, achieve better agreements with the chip suppliers. This option was declined because of the difficulties to obtain this data. It would have consumed a lot of additional research and data mining time.

b) Which complex IC types: ASIC, FPGA, Microprocessor and Std. ASIC

As explained in the Methodology (see chapter 3.1.1), this research only includes ASIC, FPGA, Microprocessor and Std. ASIC with more than 40 pins in the package. This limit was defined to only include the most complex ICs and to delimitate and simplify the scope of the research. However, using this indicator of complex ICs, some relatively small analogue ASICs in particular (e.g. converters, drivers, etc.) and other small ICs that would also be interesting to be explored are omitted of the research.

Narrowing the focus to fewer IC types for the limited time of this research enhanced the reliability and quality of the data being retrieved and analysed, as a yet wider scope of ICs would have meant less time to confirm and cross-check the validity data being collected and processed.

c) Which space missions (satellites and spacecraft to be investigated)

The space missions included in this research were selected looking at some key characteristics like the launch date, lifetime or type of space programme in order to diversify and have a wide range of missions with different characteristics, covering as many mission types as possible.

This selection was done also anticipating some known problems to obtain the data for some missions in the initial and long mission list. For example, it was anticipated that the older the mission the more difficult could be to find complete and easy to process DCLs. Likewise, some of the missions seemed to be in a position to deliver more easily the necessary information, because for example there was recent interaction between the mission team and some of the Microelectronic section experts where this research work has originated.

Alternatively, this selection could have been done using other more restrictive criteria and then the main results obtained in the research would have been possibly different and more dedicated to a group of missions, for example only Telecommunication satellites, or only to small low budget satellites.

In this case it was decided to cover a wide range of cases, to look at the global complex IC picture, and paying attention to those exceptional cases, depending on the IC type or parameter under scrutiny that would undermine the validity of the regressions or the trends being explored. This is why some data coming from Telecommunication and Launcher missions was carefully taken apart when evaluating the results, preserving and maximising the validity of the group data.

5.4 External validity

External validity is the validity of generalized causal inferences in scientific studies. Applied to this research, it is checked if the results obtained from the missions included in this research can be generalized to any space missions in general.

As mentioned above, the sample of space missions selected to be included in this research is limited. From the 17 space missions chosen at the beginning of the research as top priority only 11 of them have been possible to be completed due to the complexity to obtain the data and the research time limitations.

In general, the results obtained in this research cannot be extrapolated to other space missions because each space mission is designed and built in a very specific context and have a lot of particularities.

However, the data collected of the use of AFMS for each mission is very valuable for further studies. Also, the current analysis of trends and patterns can be used with caution to provide background information and to support future decisions affecting technology roadmaps and work plans proposals taking into account the limitations and shortcomings of the present study. The results of this study and its conclusions can be improved by studying more missions and more IC parameters which were left incomplete due to lack of time in a future work.

6 FUTURE WORK

This research explores and gives results of the use of complex ICs in European space missions in the last years. However, some space missions and IC technical parameters initially planned to be studied in this research have been not included due to time limitations and the difficulties in the data collection process.

This chapter explains what IC technical parameters and space missions need to be completed and suggests new improvements for the research in order to raise the statistical and practical significance of the results and conclusions.

6.1 IC technical parameters

The integrated circuit technical parameters of the components used in space missions are collected and explored in order to give answer to the research questions defined in the Research objectives (see chapter 1.2). Some of these technical parameters could not be studied and in consequence not all the research questions have been answered in this report. Particularly, the research questions from 1.4 to 1.9 and the part of the research question 2 related with IC technical parameters are not completed.

These are the IC technical parameters not completed in this research:

- **FPGA type and product name**

The objective of studying these parameters is to answer the research questions 1.4 and 1.5 about the use of different types and families of FPGA, Microprocessors and Std. ASIC in space missions. Their results are not presented in this report as the Data completion phase (see chapter 3.2.4) was not finished because there was not enough time to look for all the standard names and classify them per type or family.

- **Feature size and Analogue & Mixed-signal/Digital**

The objective of studying these parameters is to answer the research questions 1.6 and 1.7 about the different complex IC technologies used in space missions. Their results are not presented in this report as the Data completion phase (see chapter 3.2.4) was not finished because there is a big complexity to find this technical information from the datasheets and other design documents of the component or ask to the engineers who designed it.

- **Pin count and design house country**

The objective of studying these parameters is to answer the research questions 1.8 and 1.9 about the AFMS technology complexity used in space missions and the country where they were designed or used. Their results are not presented in this report as the Data exploration (see chapter 3.3) was not completed due to lack of time and the complexity to explore their graphs (with more than 6 data series: 41 to 150 pins, …, to more than 650).

In a future work, it will be need more time and efforts to finish collecting and exploring these IC technical parameters in order to meet all the objectives of this research but with the advantage that the Methodology to do it is already established.

This is a suggestion of a new IC parameter that could be included in this research:

- **Space or not space**

The objective of this IC parameter is to compare in the European space missions the use of components built and qualified specifically for space applications with the ones that are designed and manufactured for commercial use but which have also been used in space missions.

The range of complex ICs could also be expanded in future works, including some of the IC types excluded in this study (e.g. image sensors, memories, pin outs larger smaller than 40, distinguishing between different Microprocessors types such as Digital Signal Processors, 8 , 16 or 32 bit microprocessors). That would require a complete revision of the DCLs and a much longer research exercise.

6.2 Space missions

From the 17 space missions selected at the beginning of the research as top priority only 11 of them could be completed. The missions not included are in a different status of completeness as it is shown in the table above:

Mission	Phase	Status (%)
Ariane 5	Complete	Complete (100%)
Proba 1	DCL collection	50%
Artemis	DCL collection	30%
Envisat	DCL collection	40%
Rosetta	Complete	Complete (100%)
Venus Express	Complete	Complete (100%)
Immarsat 4	Complete	Complete (100%)
ATV	Data Completion	50%
GOCE	Complete	Complete (100%)
Herschel-Planck	Data Completion	70%
Proba 2	Data Completion	70%
Hylas	Complete	Complete (100%)
Galileo IOV	Complete	Complete (100%)
Vega	Complete	Complete (100%)
Proba V	Complete	Complete (100%)
Sentinel 2	Complete	Complete (100%)
Bepicolombo	Complete	Complete (100%)
TOTAL: 17		**11 completed (100%)**

Table 8: Mission completeness status

Future work would aim to finish collecting and exploring the data of the missions selected that could not be completed this time. It is important to note that the Excel spread sheet has been designed in order to make easy the modification or addition of new data in the database. All Excel tables and graphs are immediately and automatically updated with the entry of new data, as well as, the graphs presented in the report.

Once the top priority space missions are completed (6 of 17 to be finished), the results of this research can be improved by collecting and exploring data of more ESA space missions taking into account the criteria defined in the Methodology (see chapter 3.1.3) include and have data from as many missions as possible in the research with the ultimate ideal objective to include all the space missions launched by ESA, at least until the existing records allow, and to keep on adding data as new missions appear.

6.3 General review phase

To completely validate the confidence in the data, it is very important that after presenting this research in ESA and possibly to the European space community, a general review phase opens in order to collect the feedback and comments of the engineers and managers involved in the use of complex ICs in space missions. They could report errors and mistakes done during the research and help to fill the missing data and gaps of the Excel AFMS database, as well as, giving some suggestions of how this or other similar/continuation studies could be improved in the future.

7 CONCLUSIONS

The aim of this research is to quantify the number of ASICs, FPGAs, Microprocessors and Std. ASICs used in the last years in the European Space Agency missions in order to find trends and patterns of use, and relate those results to the current technology roadmap activities driven by the Microelectronics Section in ESA.

From the results of this research (see chapter 4) it is shown that the quantities used of AFMS in the space missions included in this research move in a range of 50 to 400 per mission, with the exception of Immarsat 4 that uses more than 1500. FPGAs are used in larger quantities than ASICs with a percentage of 50% to 30%, respectively, and seem there is a trend to continue growing. Microprocessors and Std. ASICs have a general percentage of use around 15% and 5%, respectively.

At the beginning of the research very ambitious and specific research objectives were defined (see chapter 1.2) related to the study of the technical parameters of the complex ICs used in the European space missions. However, due to time limitations (5 months research) and the complexity of the data collection process (see chapter 3.2), it has been only possible to study 4 of the 10 IC technical parameters in 11 of the 17 space missions initially selected to be subject of study in this research.

For the validation of these results it is important to note that the trends and patterns presented in this research are not statistically significant because of the small number of space missions explored and the high dispersion and noise of the data. However, the results of this research can have practical significance as they might be useful to ESA technology policy managers to have more information and visibility on the evolution of the use of complex ICs in European space missions.

To conclude, this study remains open to further improvements by completing the missing data and especially by adding more European space missions and IC technical parameters to the research. This will lead to better and more comprehensive and reliable results in order to help ESA policy managers make more educated decisions of the development of complex IC technologies for space applications.

Hopefully, this research has been just a first step and it will be completed, continued and updated in the future.

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