Design and ASIC Implementation of a Reconfigurable Fault-Tolerant ALU for Space Applications

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***Abstract*— Electronic devices operating in space suffer from damage due to cosmic rays, hence for such applications, radiation effects are the primary concern. With technology scaling, semiconductor devices are achieving high performance, low power, and less area, but it increases the radiation degradation and makes the integrated circuit vulnerable to error. In this paper, we have discussed the phenomena of Single Event Upset (SEU) and proposed a reconfigurable Arithmetic Logic Unit (ALU) to mitigate the degradation due to SEU. The designed ALU can be configured to either work in *'normal_mode'* or *'RadHard_mode'* based on a control signal. The design has three identical ALUs; in *'normal_mode'* of operation, only one ALU is active, and in *'RadHard_mode'* it uses two redundant ALUs to mitigate the effect of SEU. Errors were inserted during the simulation to test the fault tolerance capability of the design. ASIC (Application Specific Integrated Circuit) implementation was done using 180nm CMOS technology; the reported area was 69013µm^2 and power was 4.035mW. This approach may be power efficient compared to the traditional TMR (Triple Modular Redundancy) approach in which all the redundant blocks are always active, independent of operating environment.**

Keywords—Reliable computing, Fault-tolerant ALU, Single Event Upset, Radiation hardened design.

I. INTRODUCTION

Due to advances in semiconductor technology, the performance of Application Specific Integrated Circuits (ASICs) has improved significantly [1]. The digital chips are able to attain high frequency while consuming low power and less area. However, the reliability of such devices is a big concern while operating in a high radiation environment [2]. The technology scaling of the semiconductor devices provides high performance with low power and less area, but it increases the radiation degradation and makes the Integrated Circuit vulnerable to error [3]. Due to the strike of high energy particles on CMOS devices, electron-hole pairs are generated and can change an information bit in a digital circuit. Such events are called Single Event Upsets (SEUs) and are a primary concern for space equipment designers [4]. SEUs have a significant impact on electronic systems operating in deep space/ interplanetary space missions[5]. In heavy-ion experiment, it is reported that SEU sensitivity is increasing due to the increasing frequency and decreasing size of electronic devices.

In this work, the impact of radiation on semiconductor devices are investigated and its effect on digital devices in the form of SEU is explored. A reconfigurable, power-efficient radiation-hardened (RadHard) ALU is designed to mitigate the impact of radiation. The designed ALU contains three identical units and it can be configured to work in two modes *'normal_mode'* and *'RadHard_mode'*. One ALU unit, named '*org*' is always active independent of the mode of operation. The other two ALU units named '*dup1*' and '*dup2*' are active only in *RadHard_mode*. A simple MEMS sensor can be used to sense the intensity of radiation, and it can be fed as input to ALU to work either in *'normal_mode'* or in *RadHard_mode*. When the control is 1, indicating high intensity of radiation, the ALU works in *RadHard_mode* else it works in *'normal_mode'*.

II. SINGLE EVENT UPSET ON SEMICONDUCTOR DEVICES

Single event upset happens due to the strike of a single particle on semiconductor devices. The interaction of a particle with high kinetic energy may cause degradation in an electronic circuit. When a heavy ion strikes a semiconductor device, it interacts with the atoms present in the material and loses its kinetic energy throughout the travel in the material [6]. In a semiconductor material, the transferred energy break the covalent bonds, and electron-hole pairs are generated [4]. The generation of electron-hole pair is along the track of the ion and forms a charge funnel, as shown in Fig. 1. The energy required to generate an electron-hole pair for silicon is 3.6eV, and for SiO2, it is 17ev [5].

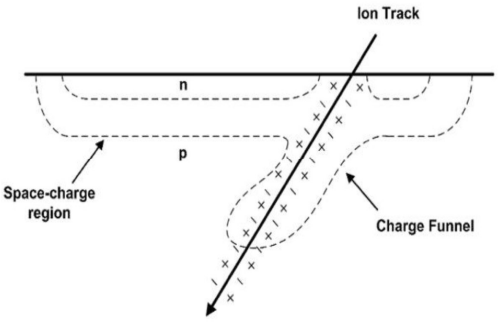

Fig. 1. Charge funnel in Silicon due to heavy ion strike.

As an ion transverses the CMOS device or any other material, the charged particle slows down and loses the kinetic energy. The energy loss of the ion throughout the ion track is measured in the form of Liner energy transfer (LET) [7]. LET has a strong dependence on kinetic energy and mass of the incident particle. To estimate the LET and generate the current profile for an ion TRIM or forcast software can be used. The average difference between the LET value measured and obtained from TRIM is 2-6% with 95% accuracy.

$$LET = \frac{d\mathrm{E}}{d\mathrm{x}}$$

Where, E is the energy of the incident particle.

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For an 80MeV Hydrogen, surface LET graph is shown in Fig. 2.

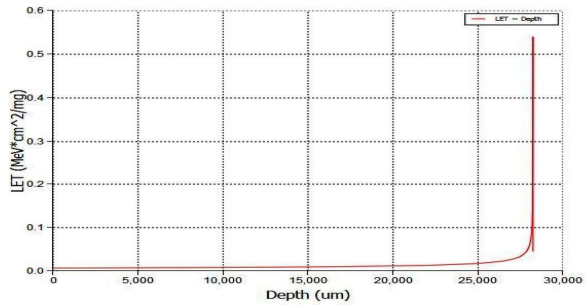

Fig. 2(a). Linear energy transfer for 80MeV Hydrogen by Forcast.

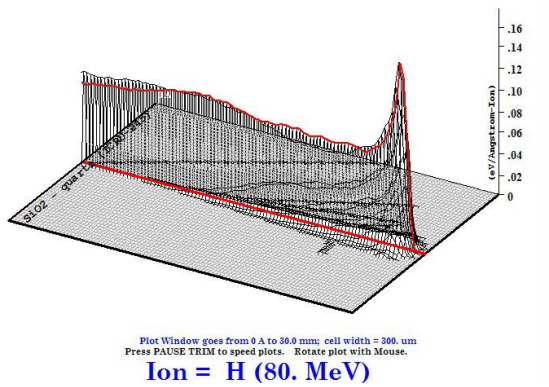

Fig. 2(b). Linear energy transfer for 80MeV Hydrogen by TRIM.

Due to these generated charges in a CMOS device, it may change the value of a bit from '0' to '1' and it is known as single event upset or single event transient (SET). This change in a single bit may lead to the failure of a digital device.

III. Design of *RadHard* ALU

The designed radiation-hardened ALU consists of three separate ALU units and was implemented using Verilog HDL. The ALU can be configured with the help of a MEMS sensor to work either in *'normal_mode'* or *'RadHard_mode'*.

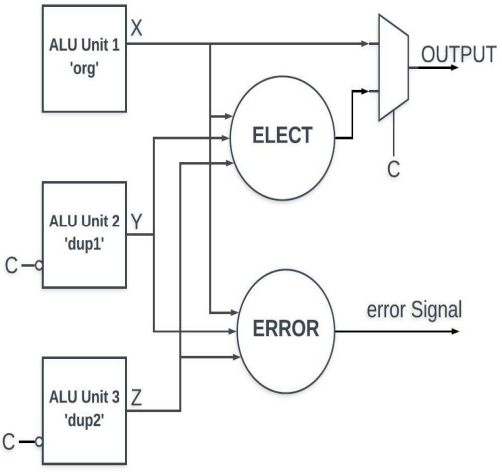

Fig. 3(a). Architecture of designed RadHard ALU.

One ALU unit of design, named *'org'* is always active independent of operating mode, the other two ALU units *'dup1'* and *'dup2'* are active when the design is operated in *'RadHard_mode'*. The ALU units *'dup1'* and *'dup2'* are not active when the design is operated in *'normal_mode'*, and it allows the design to use less power compared to the conventional TMR approach. The architecture of the designed RadHard ALU is shown in Fig. 3(a). The control signal 'C' may be generated by a MEMS sensor. When the design works in *'normal_mode'*, means control signal 'C' is '0' then the two redundant ALU units *'dup1'* and *'dup2'* will be in standby mode and will perform no operations. In such a case, the result generated by ALU unit *'org'* will be the final result from design. In other case when the design works in *'RadHard_mode'* means, control signal 'C' is '1' then all the ALU units will function and the output will be generated by comparing the results of all three ALU units.

In *'RadHard_mode'*, the outputs of all three ALU units are compared. The fault-tolerance approach is based on the idea that if one ALU unit suffers from SEU and generates a wrong result, then while comparing, the results of the other two ALU units will match, and it will be passed at output. As long as the output of any two ALU units matches, or output of all the ALU units matches, the ELECT block will generate the output of the device. The simplified circuit for ELECT is given by-

$$ELECT = XY + YZ + ZX$$

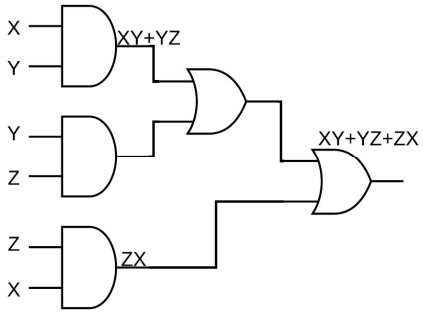

Fig. 3(b). Circuit to implement ELECT Block.

When all the ALU units generate different results in *'RadHard_mode'*; which may be the case of single event transient in more than one ALU unit at the same instant, then this architecture will fail to provide correct output. And in such cases, it will generate an error signal to inform the processor that the generated result of RadHard ALU may not be correct. The ERROR circuit can be implemented by –

$$ERROR = X'Y + Y'Z + Z'X$$

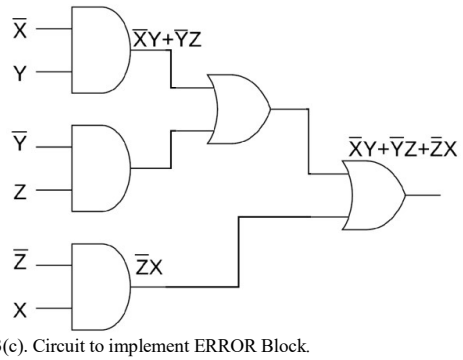

Fig. 3(c). Circuit to implement ERROR Block.

Although the ALU unit1 named *'org'* has special significance since it works in both *'normal_mode'* and *'RadHard_mode'*, it is important to keep in mind that it has no special weight while using in *'RadHard_mode'*. In RadHard_mode, all three ALU units, *'org'*, *'dup1'* and *'dup2'* are of equal importance.

IV. RTL Simulation and Verification of *RadHard* Feature

The RTL code of design was simulated using *vcs* tool of synopsys. Simulation results are given in Fig. 4(a). The *alu_ctrl* is the control signal which guides ALU to perform addition or subtraction or multiplication etc. The function of *alu_ctrl* is given in Table1.

TABLE I: Functions of *'ALU_CTRL'* signal.

Function	alu_ctrl	Description
ADD	0000	Addition of in1 and in2
SUB	0001	Subtraction of in1 and in2
MUL	0010	Multiplication of in1and in2
BWAND	0011	Bit wise AND Operation
BWOR	0100	Bitwise OR Operation
BWXOR	0101	Bitwise XOR Operation
SRA	0110	Arithmetic Right Shift
SRL	0111	Logical Right Shift
SLL	1000	Logical Left Shift
LESS	1001	in1 less than in2 (signed)
LESSU	1010	in1 less than in2 (unsigned)

The input signal C is to reconfigure the design weather to be used in *'normal_mode'* or *'RadHard_mode'*. For simulation purpose, the name used for input signal 'C' is 'mode_sel'. Fig. 4(a) shows that when 'mode_sel' is 0 means device is in *'normal_mode'* of operation, the output of the design is generated by only *'org'* unit while *'dup1'* and *'dup2'* units are not active. When mode_sel' is 1, means device is working in *'RadHard_mode'*, all the three alu units *'org'*, *'dup1'* and *'dup2'* are active and results are generated by ELECT block and ERROR block.

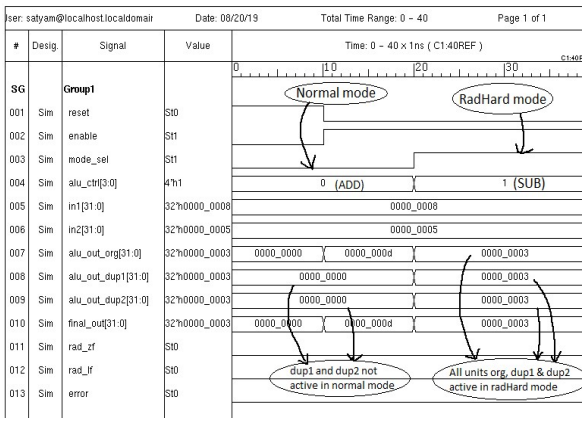

Fig. 4(a). Simulation of designed ALU in normal_mode.

To test the radiation hardening feature, it is assumed that the *'dup2'* unit suffers from SEU from 40ns to 50ns, for a period of 10ns. To test the radiation hardening, force constant feature of tool is used. It is shown in Fig. 4(b) that when '*dup2*' is suffering SEU the final output of the design, *final_out* is correctly generated by *ELECT* block.

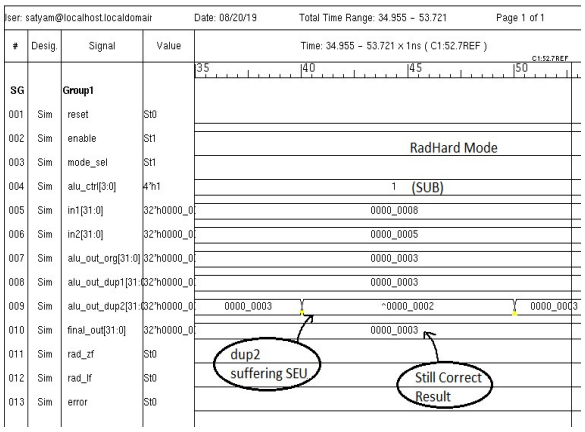

Fig. 4(b). Simulation of designed ALU under SEU on dup2.

The radiation hardening feature of this architecture is based on the idea that SEU occurs at any one ALU unit at a time. The limitation of this architecture is that it is unable to mitigate the impact of radiation when more than one ALU units suffer from SEU at the same instant. If SEU occurs in more than one ALU units at the same instant, then it generates an error signal.

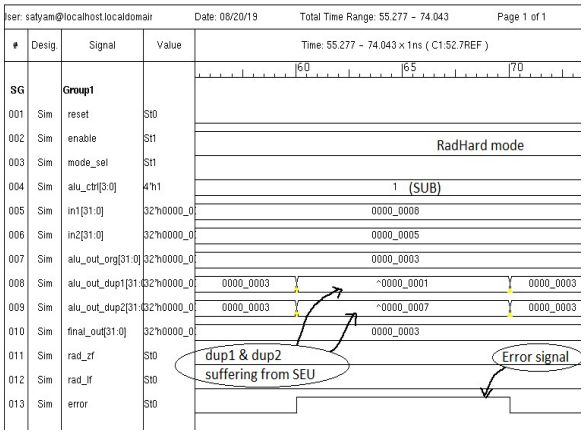

Fig. 4(c). Simulation of ALU under SEU on dup1 and dup2.

In Fig. 4(c) it is shown that from 60ns to 70ns, *dup1* and *dup2* both ALU units are under influence of SEU; so, in that case, an error signal is generated indicating processor that the output might be incorrect.

V. ASIC Implementation

The design is implemented on 180nm CMOS technology. *Design_compiler* tool from Synopsys was used for synthesis. The gate-level netlist was extracted from *design_compiler*, and post-synthesis simulation was performed using *vcs* tool to verify the correctness of synthesis. The post-synthesis simulation is shown in Fig. 5.

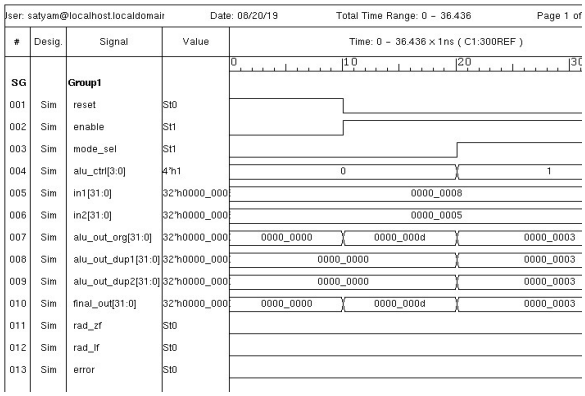

Fig. 5. Post-synthesis simulation of designed RadHard ALU.

The netlist and .sdc files are taken from *design_compiler* and is incorporated in innovus tool of cadence for physical design. The layout of designed RadHard ALU is shown in Fig. 6. The reported area and power after physical design is given in Table II and Table III. For physical verification, calibre tool is used.

TABLE II. AREA REPORTED AFTER PHYSICAL DESIGN.

Unit/Block name	Area (μm^2)
'Org' unit	22412.992
'*Dup1'* unit	22412.992
'*Dup2'* unit	22412.992
ELECT and *ERROR* Block	1774.976
Total	69013.952

TABLE III. POWER REPORT AFTER PHYSICAL DESIGN.

Type	Power
Internal Power	1.729mW
Switching Power	2.305mW
Leakage Power	700.6uW
Total Power	4.035mW

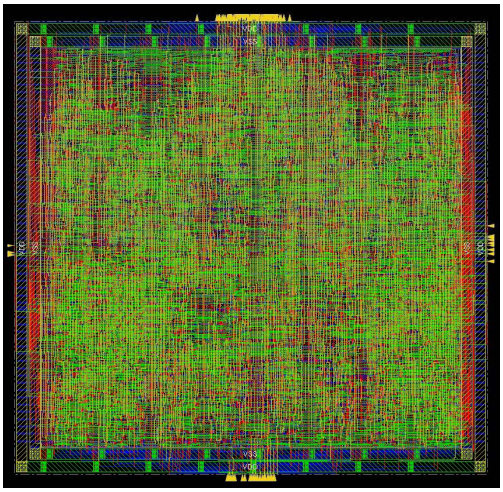

Fig. 6. Layout of designed RadHard ALU using innovus.

VI. CONCLUSION

Blocks such as multipliers, adders are the most power-hungry blocks in processors, and all copies of such blocks are always active in the conventional TMR approach. The designed *RadHard* ALU attempts to save power due to its reconfigurable feature. The design efficiently mitigates the single event upset when a single ALU unit suffers from SEU. The limitation of this architecture is that if two units out of *org*, *dup1* and *dup2* suffer from SEU at same instant then this approach fails; however, it generates an error signal in such cases to inform the processor that generated result from ALU may be incorrect. Since the SEU is soft errors and the damage due to SEU is not permanent, the chances of getting two faulty units at the same instant are rare. Area report after physical design shows that the area consumed by ELECT and ERROR blocks (1775 μm^2) is very less compared to area of a single ALU unit (22413μm^2). The power consumption after physical design is reported to be 4mW.

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