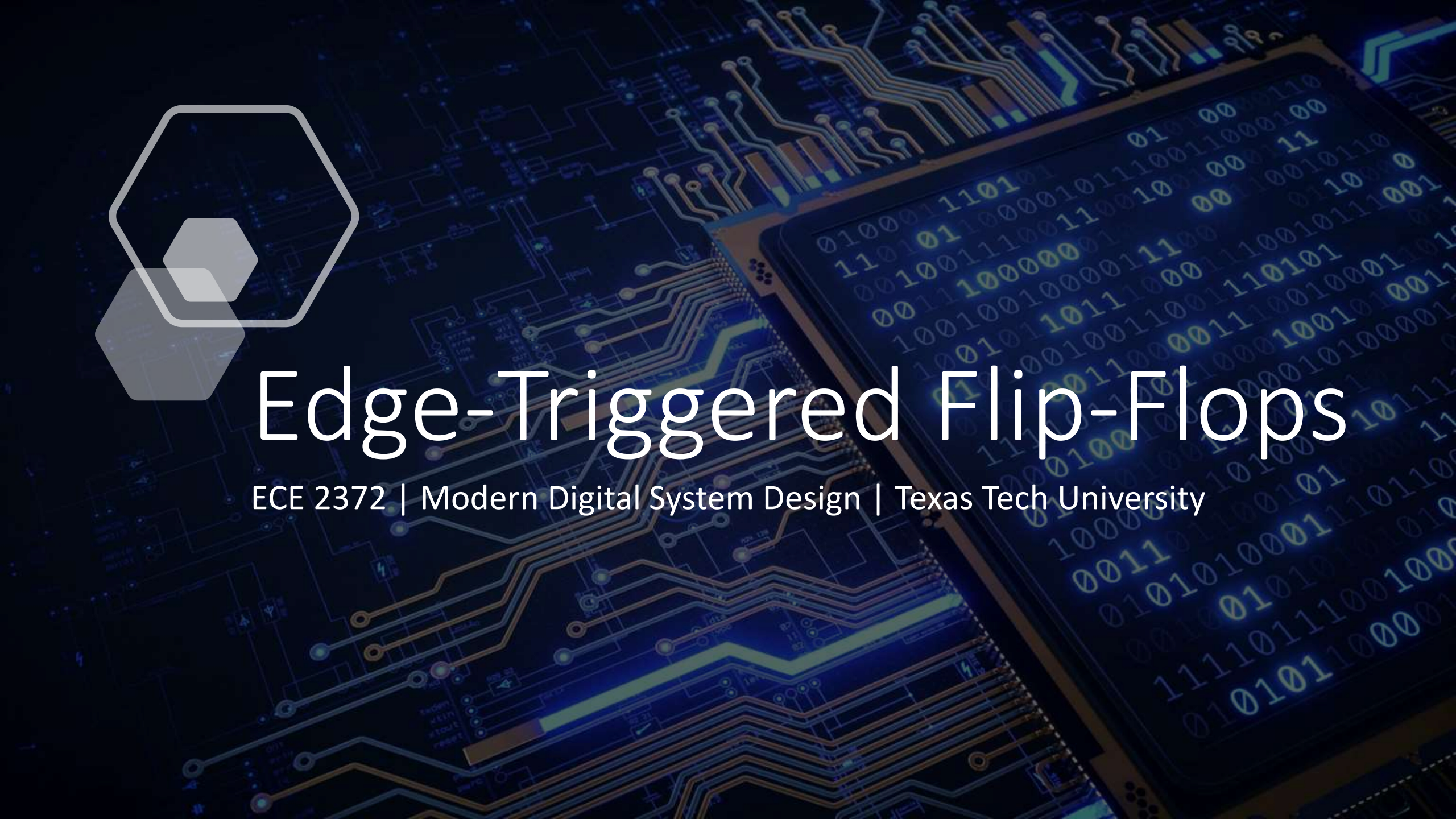
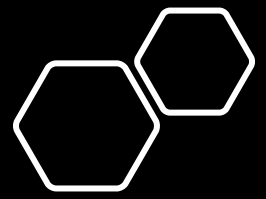


Edge-Triggered Flip-Flops

ECE 2372 | Modern Digital System Design | Texas Tech University

Lecture Overview

- The Data (D) Latch
- Edge-Triggered D Flip-Flop
- S-R Flip-Flop
- J-K Flip-Flop
- T Flip-Flop

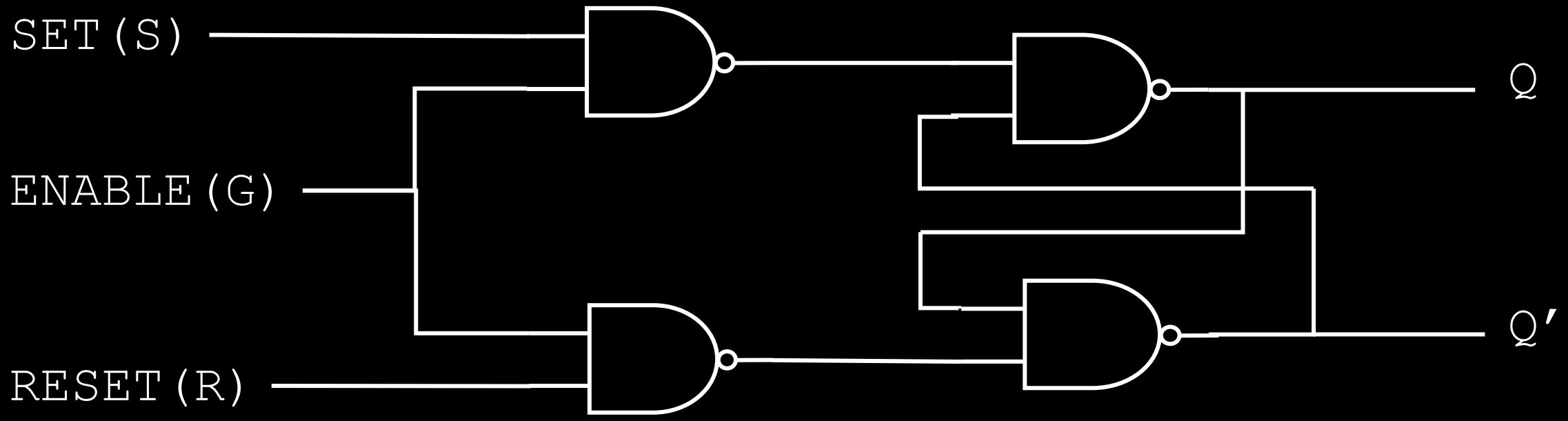


The Data (D) Latch

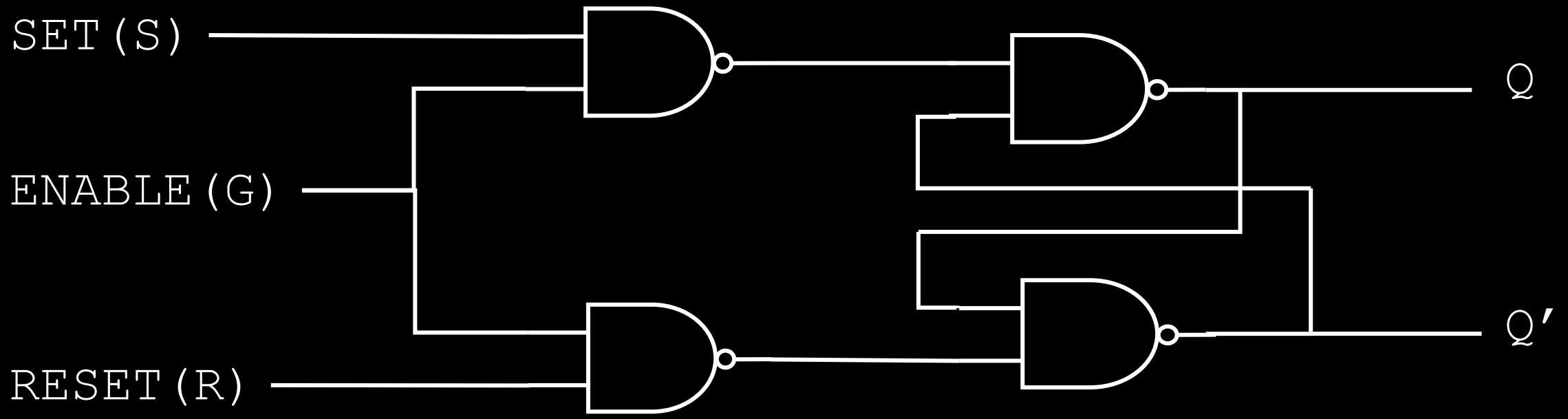
Edge-Triggered Flip-Flops | Modern Digital System Design

The Data (D) Latch

Before we can look at Flip-Flops, we need to make a change to our Gated S-R Latch.

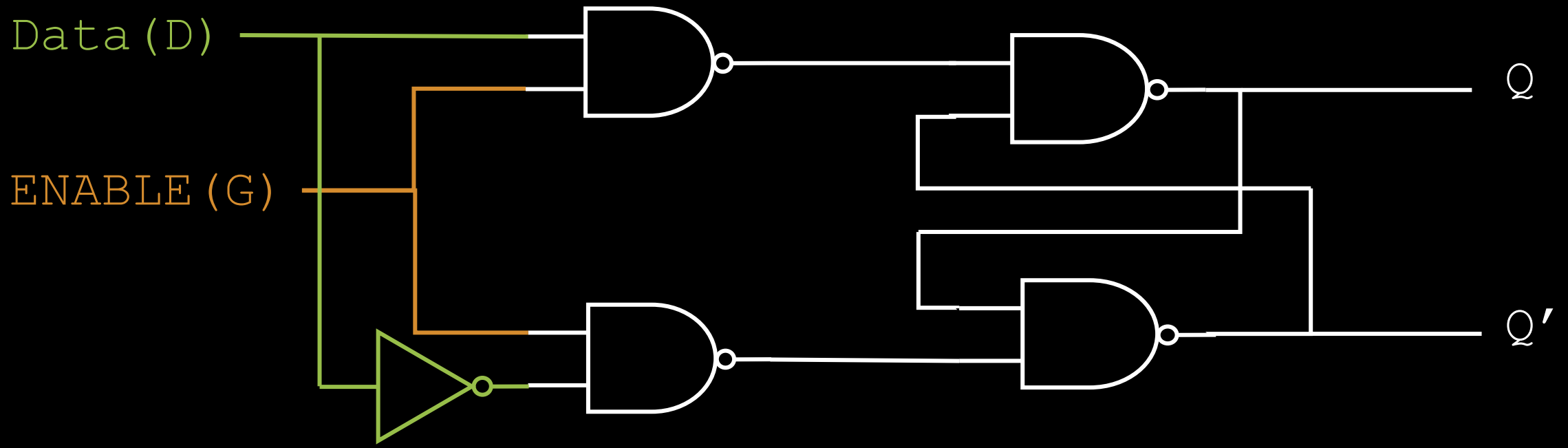


The Data (D) Latch



This latch can still be put in an invalid state (Q = 1, Q’ = 1).

The Data (D) Latch



By Inverting D, we force S and R to be opposite

What questions do you have?

EXAM QUESTION | The Data (D) Latch

What will the state of a D Latch be at the end of the following sequence of inputs?

A. SET
B. RESET
C. INVALID
D. UNDEFINED

G	D
0	0
0	1
1	1
1	0
0	1
0	0

EXAM QUESTION | The Data (D) Latch

What will the state of a D Latch be at the end of the following sequence of inputs?

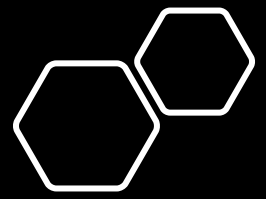
~~A. SET~~

B. RESET

~~C. INVALID~~

~~D. UNDEFINED~~

G	D	
0	0	UNDEFINED
0	1	UNDEFINED
1	1	SET
1	0	RESET
0	1	RESET
0	0	RESET

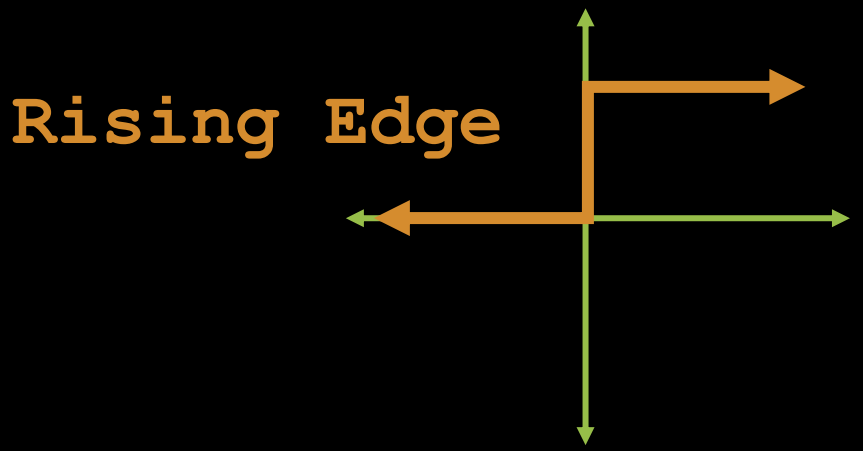


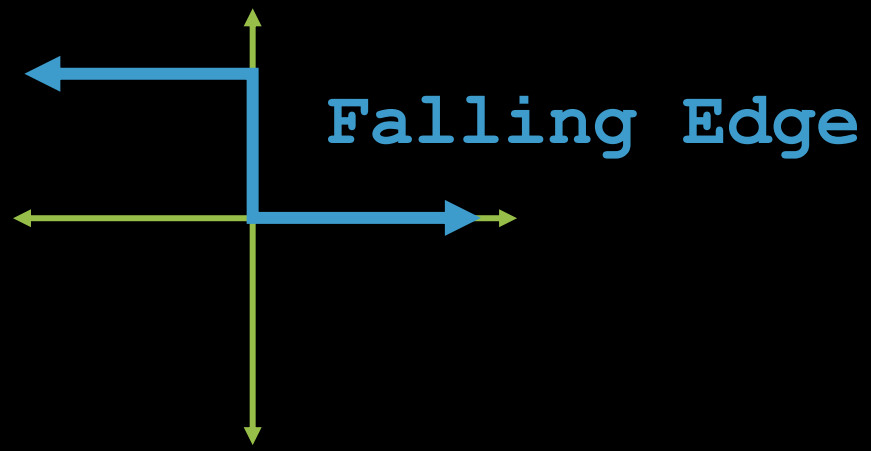
Edge-Triggered D Flip-Flop

Edge-Triggered Flip-Flops | Modern Digital System Design

Edge-Triggered D Flip-Flop

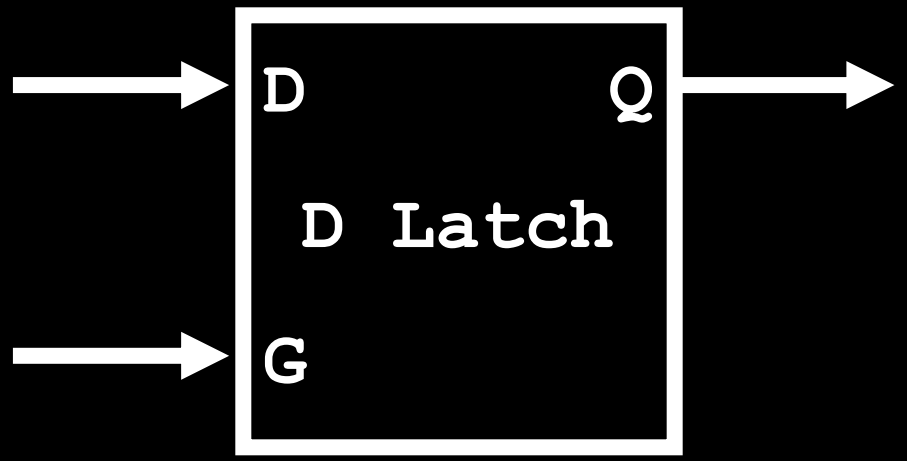
- We'll use this flip-flop most of the time.
- The Data (D) flip-flop helps to synchronize the storage of data by tightly controlling when the state can be updated.
- The D flip-flop will only update on the rising/falling edge of the gate.



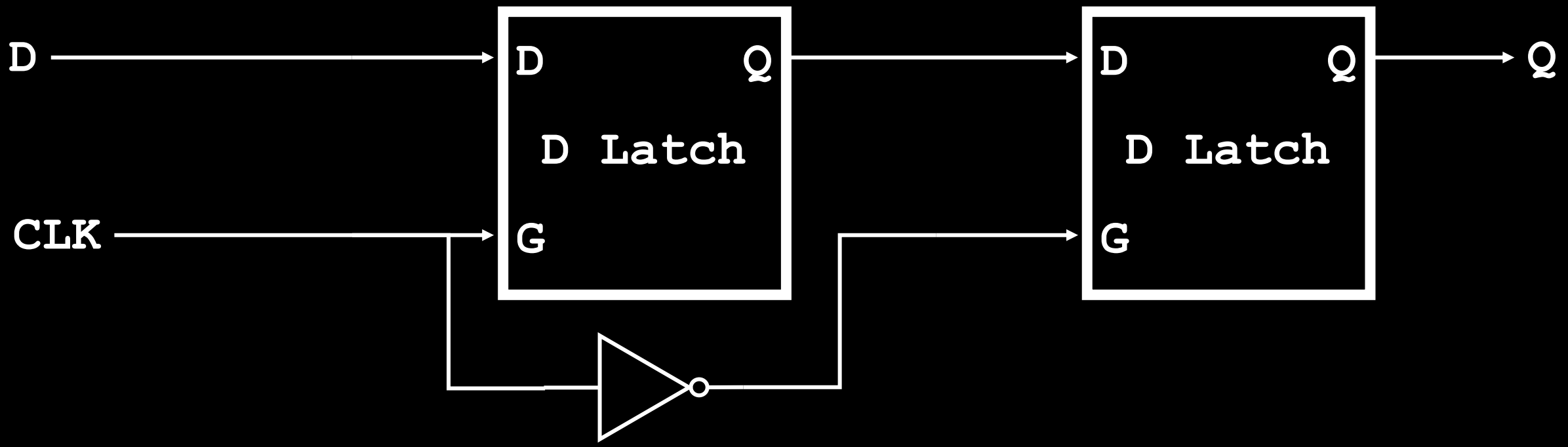


Edge-Triggered D Flip-Flop

First, lets package up our D latch.

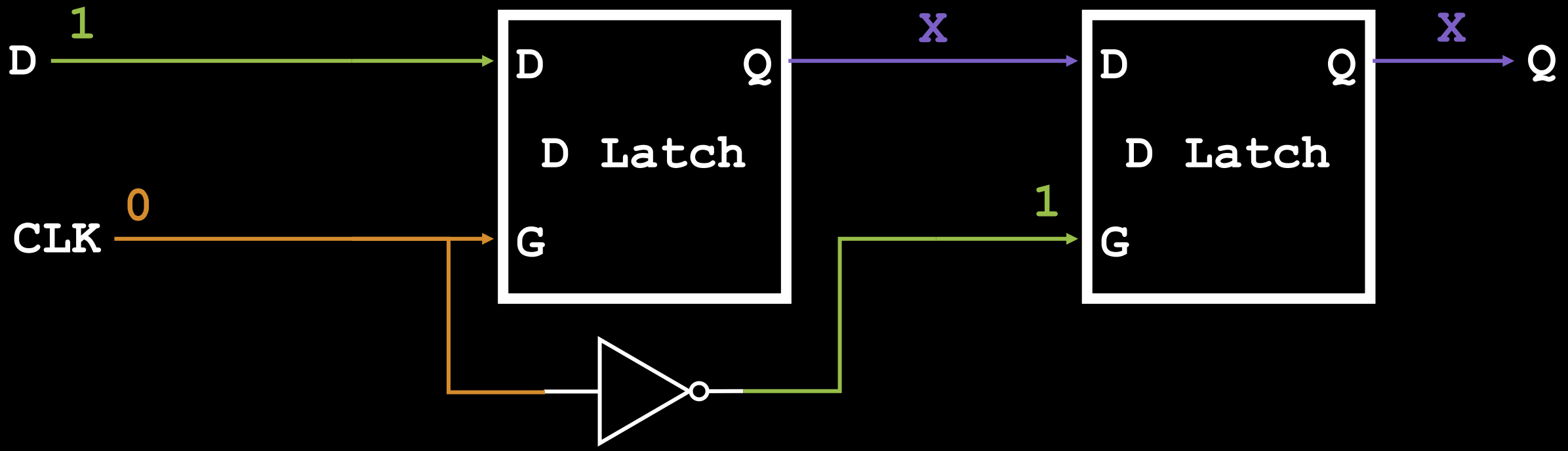


Edge-Triggered D Flip-Flop



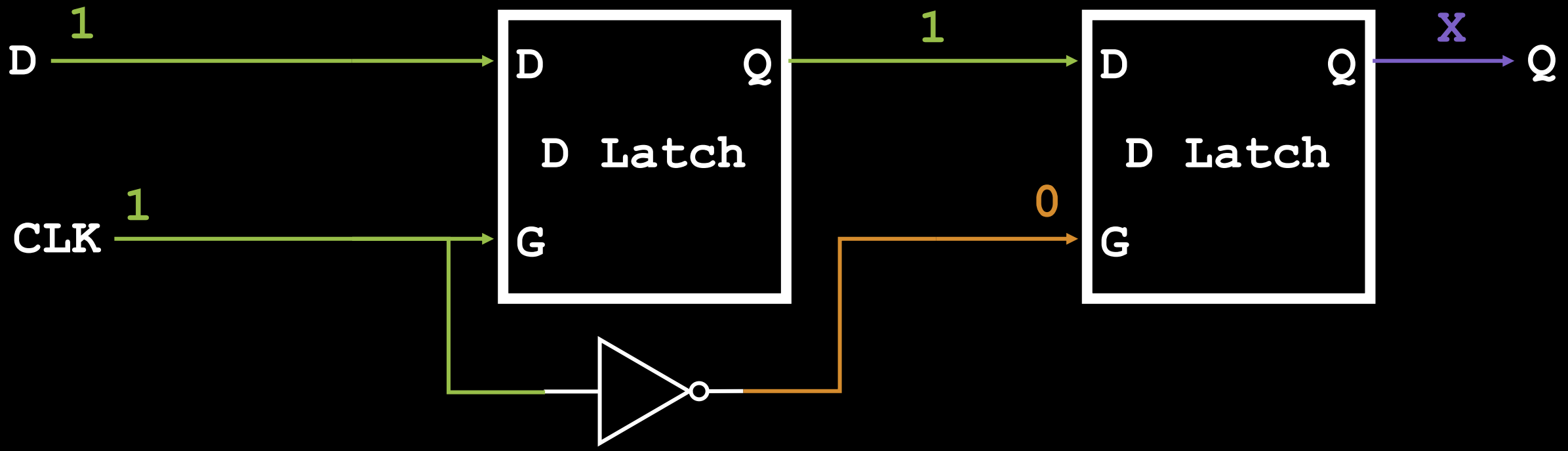
Edge-Triggered D Flip-Flop

1 | 0



Edge-Triggered D Flip-Flop

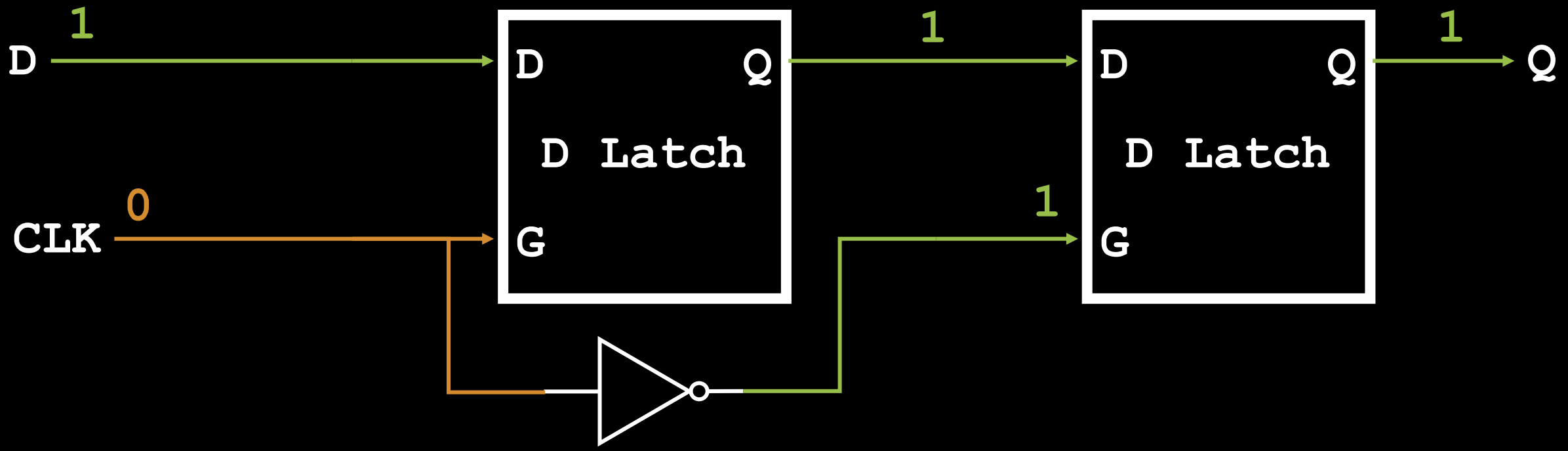
1 | 0



Edge-Triggered D Flip-Flop

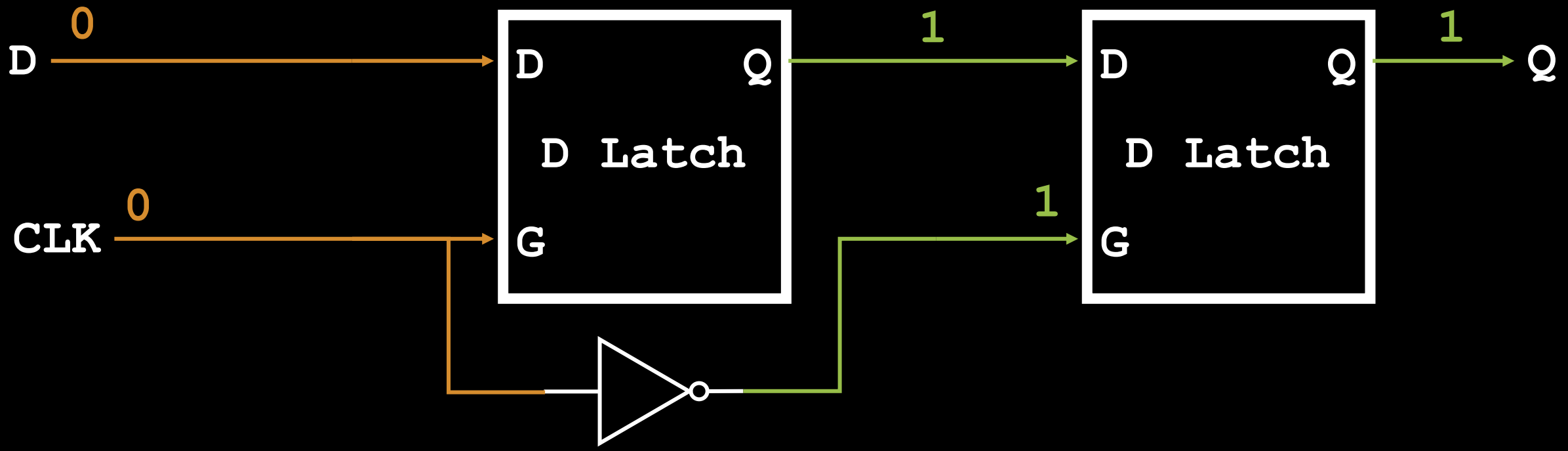
1 | 0

It's only when the CLK goes from 1 to 0 that the flip-flop updates.



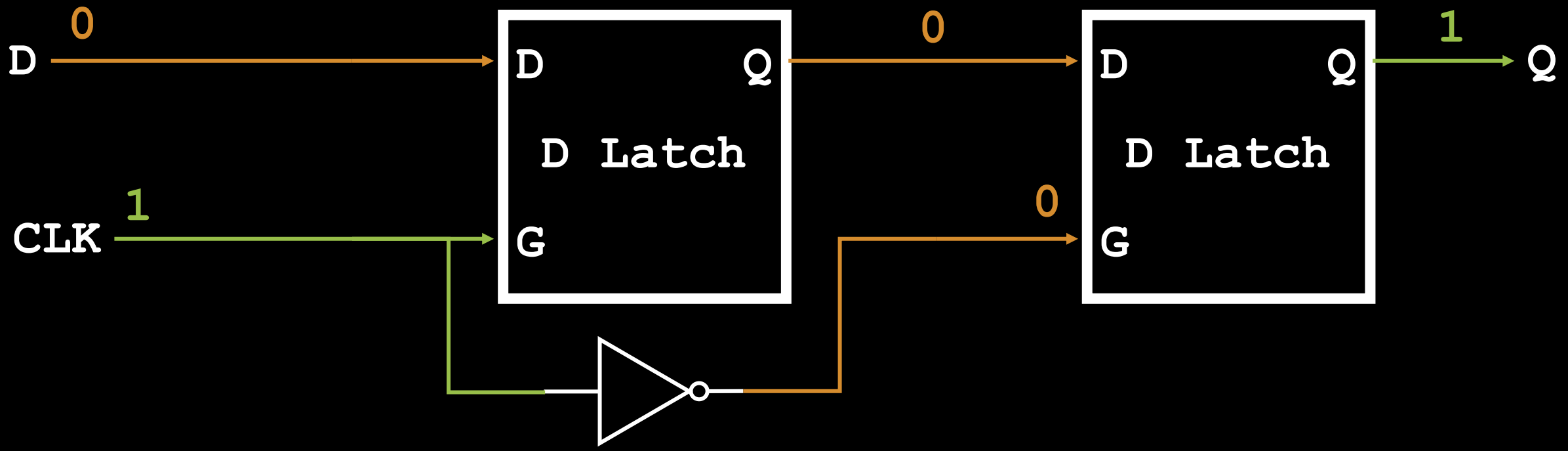
Edge-Triggered D Flip-Flop

1 | 0



Edge-Triggered D Flip-Flop

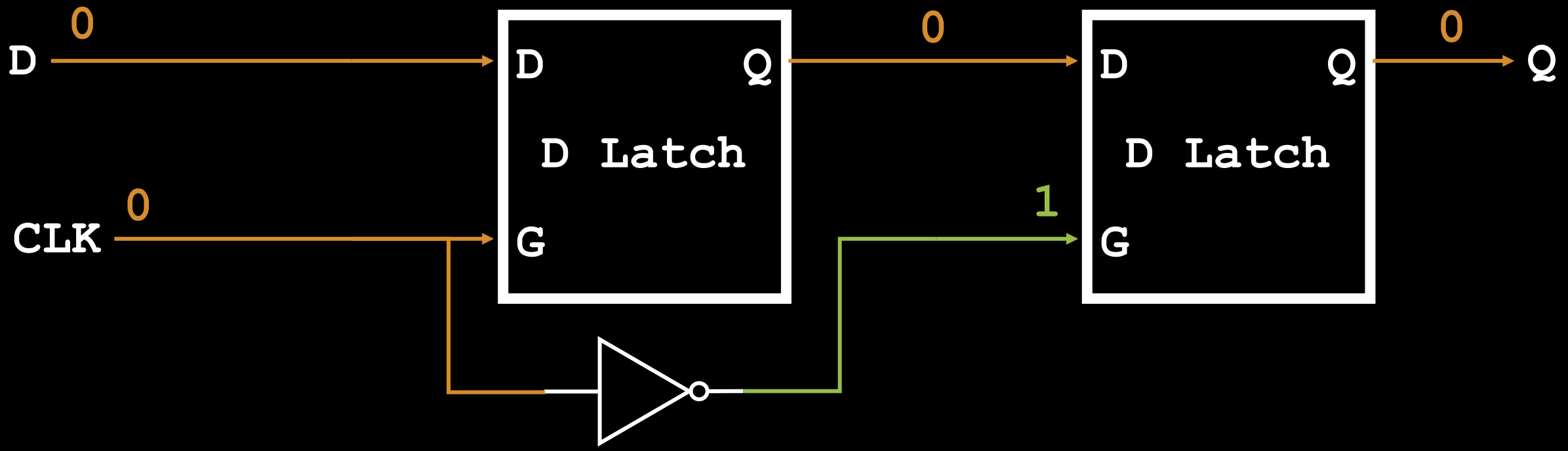
1 | 0



Edge-Triggered D Flip-Flop

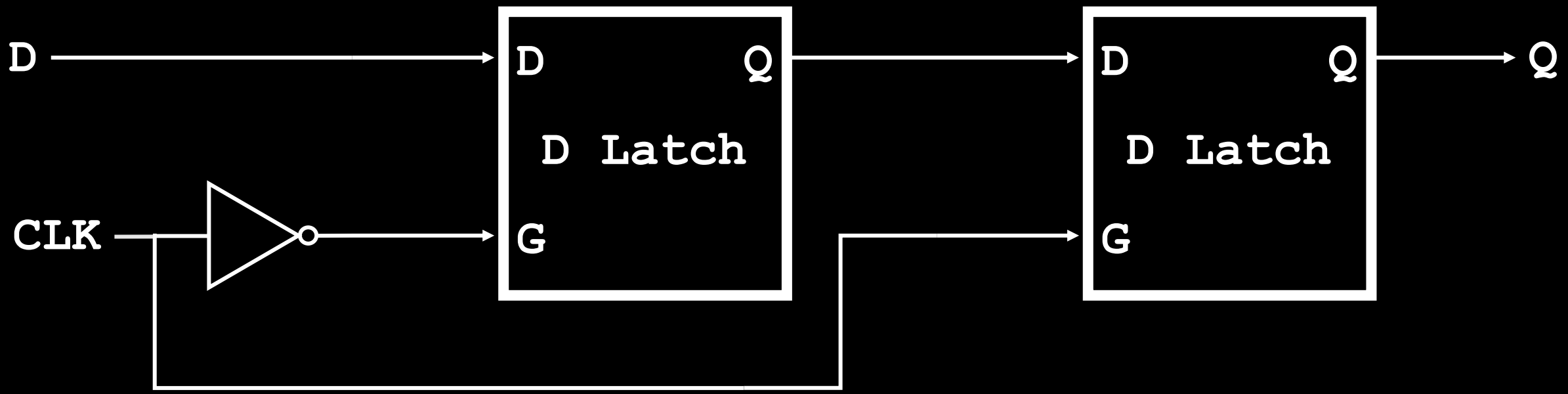
1 | 0

This is a **Falling Edge-Triggered D Flip-Flop**.



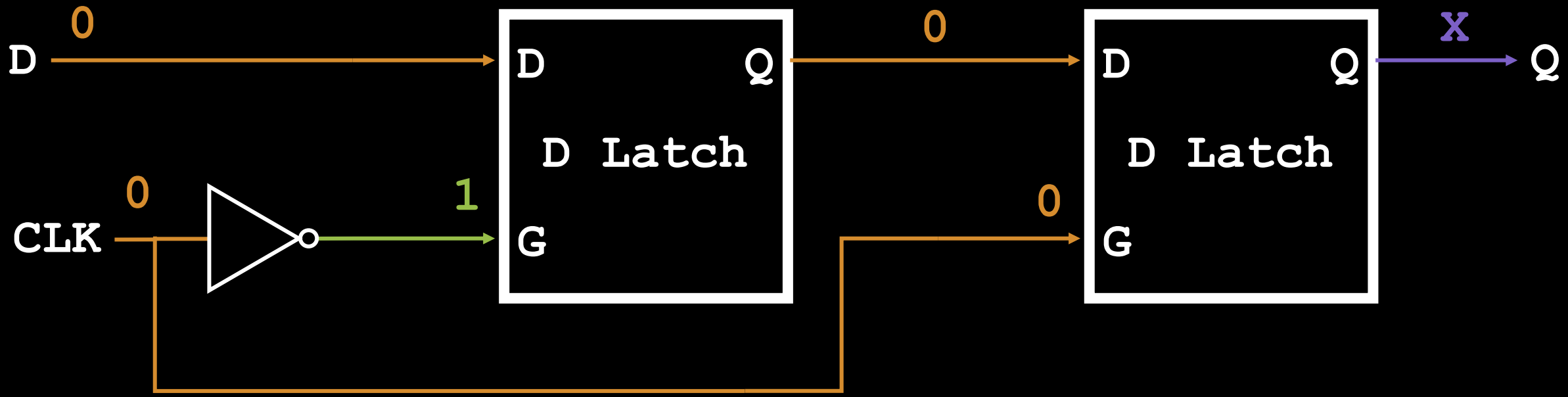
Edge-Triggered D Flip-Flop

We can convert to a rising edge-triggered D flip-flop by moving the inverter.



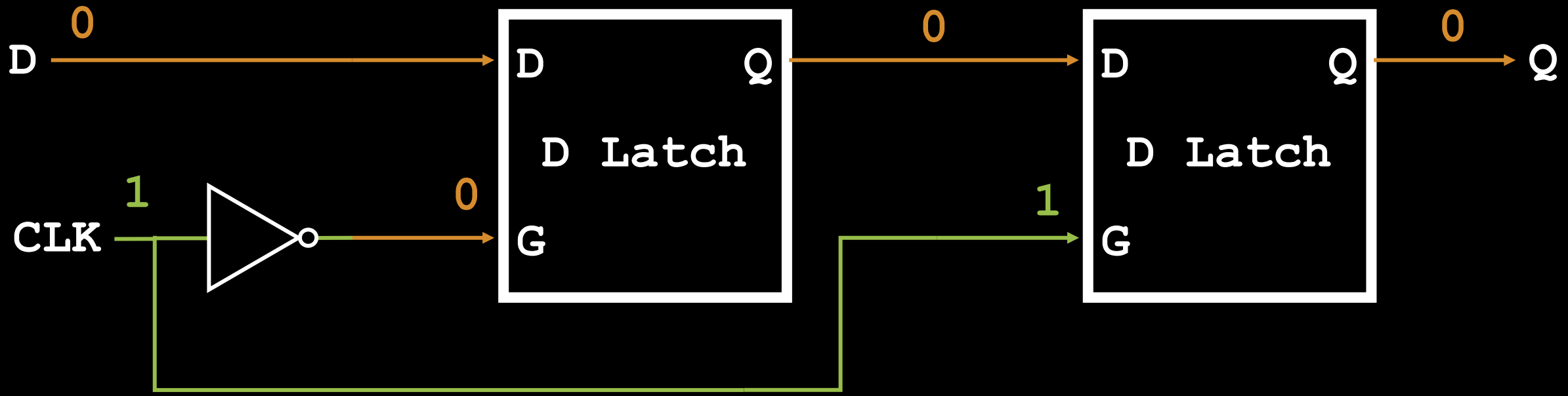
Edge-Triggered D Flip-Flop

We can convert to a rising edge-triggered D flip-flop by moving the inverter.



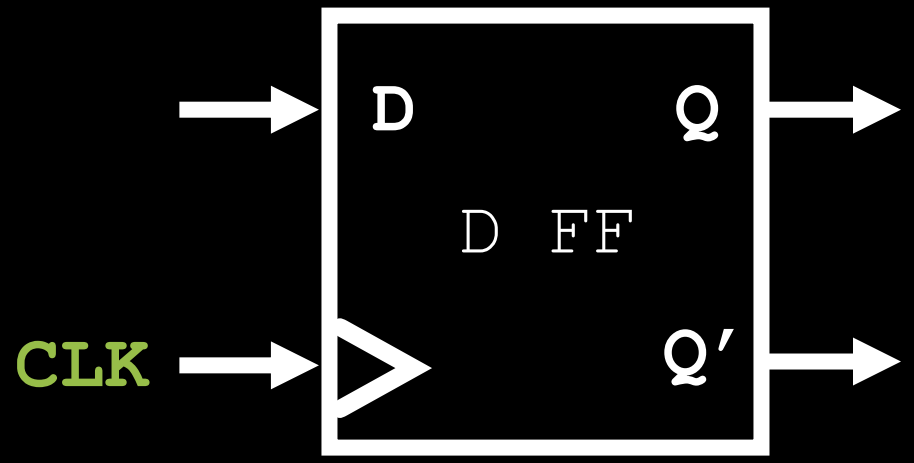
Edge-Triggered D Flip-Flop

We can convert to a rising edge-triggered D flip-flop by moving the inverter.



Edge-Triggered D Flip-Flop

Finally, let's package the D Flip-Flop so we can use it later.



$$Q^+ = D$$

This is called the Next State Equation.

What questions do you have?

EXAM QUESTION | Edge-Triggered D Flip-Flop

What will the state of a rising edge-triggered D flip-flop be after the following input sequence?

A. SET
B. RESET
C. INVALID
D. UNDEFINED

CLK	D
0	0
1	1
0	1
1	0
0	0
1	0

EXAM QUESTION | Edge-Triggered D Flip-Flop

What will the state of a rising edge-triggered D flip-flop be after the following input sequence?

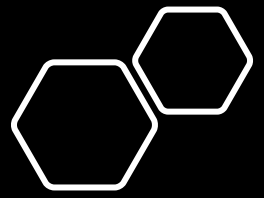
~~A. SET~~

B. RESET

~~C. INVALID~~

~~D. UNDEFINED~~

CLK	D	
0	0	UNDEFINED
1	1	RESET
0	1	RESET
1	0	SET
0	0	SET
1	0	RESET

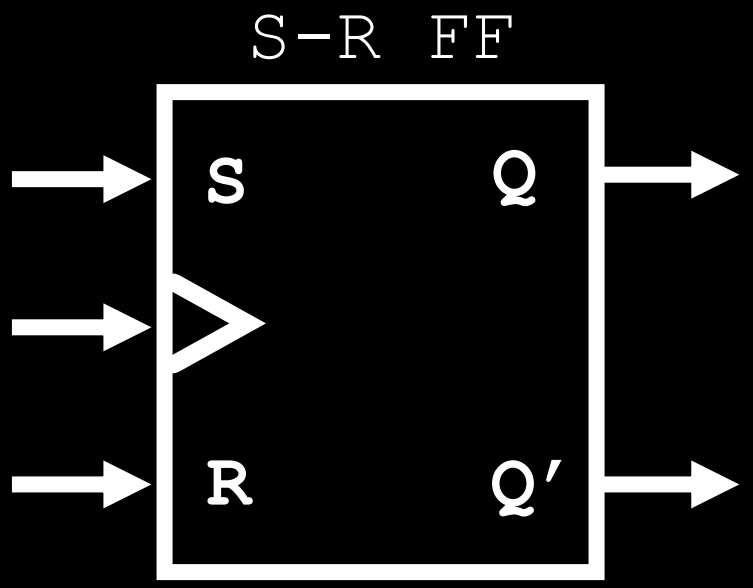


S-R Flip-Flop

Edge-Triggered Flip-Flops | Modern Digital System Design

S-R Flip-Flop

The S-R Flip-Flop allows us to keep the flexibility of the S-R Latch but keep the edge-trigger.



Input	Output
S = R = 0	No Change
S = 1, R = 0	SET (After CLK Edge)
S = 0, R = 1	RESET (After CLK Edge)
S = R = 1	INVALID (After CLK Edge)

$$Q^+ = R'S + R'Q$$

S-R Flip-Flop

$$Q^+ = R'S + R'Q$$

Let's unpack this next state equation.

$$R = 0, S = 0$$

$$Q^+ = (0)'(0) + (0)'Q$$

$$Q^+ = (1)(0) + (1)Q$$

$$Q^+ = 0 + Q$$

$$Q^+ = Q$$

S-R Flip-Flop

$$Q^+ = R'S + R'Q$$

Let's unpack this next state equation.

$$R = 0, S = 1$$

$$Q^+ = (0)'(1) + (0)'Q$$

$$Q^+ = (1)(1) + (1)Q$$

$$Q^+ = 1 + Q$$

$$Q^+ = 1$$

S-R Flip-Flop

$$Q^+ = R'S + R'Q$$

Let's unpack this next state equation.

$$R = 1, S = 0$$

$$Q^+ = (1)'(0) + (1)'Q$$

$$Q^+ = (0)(0) + (0)Q$$

$$Q^+ = 0 + 0$$

$$Q^+ = 0$$

S-R Flip-Flop

$$Q^+ = R'S + R'Q$$

Let's unpack this next state equation.

$$R = 1, S = 1$$

$$Q^+ = (1)'(1) + (1)'Q$$

$$Q^+ = (0)(1) + (0)Q$$

$$Q^+ = 0 + 0$$

$$Q^+ = 0$$

What questions do you have?

EXAM QUESTION | S-R Flip-Flop

What will the state of a falling edge-triggered S-R flip-flop be at the end of the following sequence of inputs?

A. SET
B. RESET
C. UNDEFINED
D. INVALID

CLK	S	R
0	1	0
1	0	1
0	0	1
1	1	0
0	1	1
1	0	0

EXAM QUESTION | S-R Flip-Flop

What will the state of a falling edge-triggered S-R flip-flop be at the end of the following sequence of inputs?

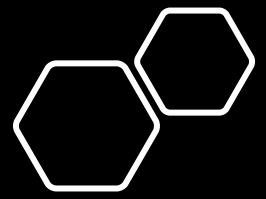
A. SET

~~B. RESET~~

~~C. UNDEFINED~~

~~D. INVALID~~

CLK	S	R	
0	1	0	UNDEFINED
1	0	1	UNDEFINED
0	0	1	RESET
1	1	0	RESET
0	1	1	SET
1	0	0	SET

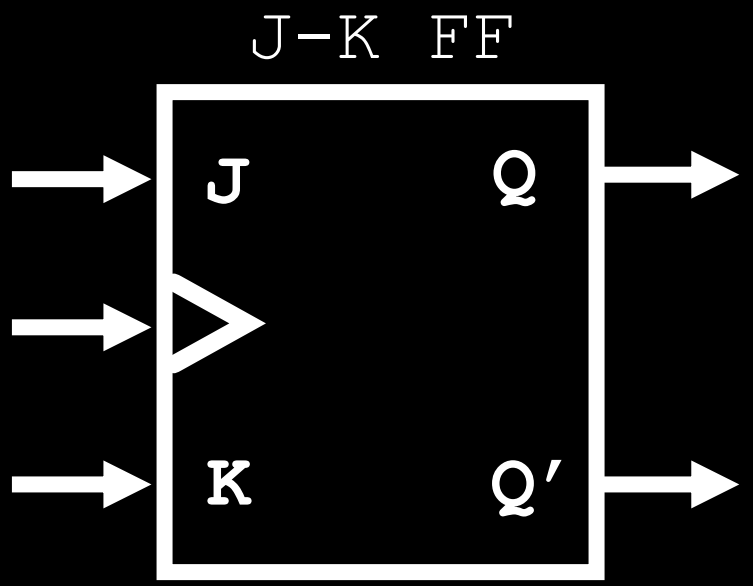


J-K Flip-Flop

Edge-Triggered Flip-Flops | Modern Digital System Design

J-K Flip-Flop

The J-K flip-flop adds some additional functionality to the S-R Flip Flop

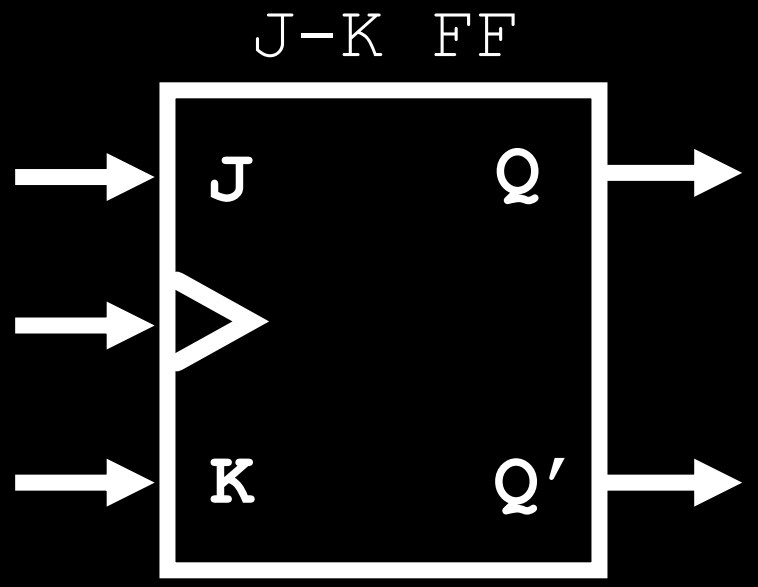


Input	Output
J = K = 0	No Change
J = 1, K = 0	SET (After CLK Edge)
J = 0, K = 1	RESET (After CLK Edge)
J = K = 1	TOGGLE (After CLK Edge)

J-K Flip-Flop

J	K	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$$Q^+ = JQ' + K'Q$$



What questions do you have?

EXAM QUESTION | J-K Flip-Flop

What will the state of a rising edge-triggered J-K flip-flop be at the end of the following sequence of inputs?

A. SET
B. RESET
C. UNDEFINED
D. INVALID

CLK	J	K
0	1	0
1	0	1
0	0	1
1	1	0
0	1	1
1	0	0

EXAM QUESTION | J-K Flip-Flop

What will the state of a rising edge-triggered J-K flip-flop be at the end of the following sequence of inputs?

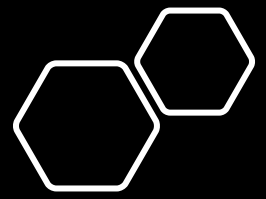
A. SET

~~B. RESET~~

~~C. UNDEFINED~~

~~D. INVALID~~

CLK	J	K	
0	1	0	UNDEFINED
1	0	1	SET
0	0	1	SET
1	1	0	RESET
0	1	1	RESET
1	0	0	SET

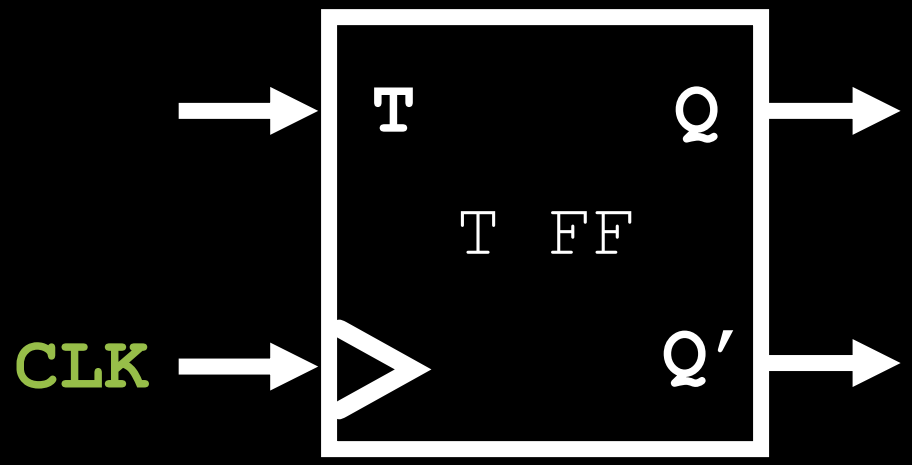


T Flip-Flop

Edge-Triggered Flip-Flops | Modern Digital System Design

T Flip-Flop

The Toggle (T) Flip-Flop is used for binary counters.



Input	Output
T = 0	No Change
T = 1	Toggle Q (After CLK Edge)

T Flip-Flop

T	Q	Q+
0	0	0
0	1	1
1	0	1
1	1	0

$$Q^+ = T \oplus Q$$

What questions do you have?

EXAM QUESTION | T Flip-Flop

Assuming that the flip-flop is initially in the SET state, what will the state of a falling edge-triggered T flip-flop be at the end of the following sequence of inputs?

A. SET
B. RESET
C. INVALID
D. UNDEFINED

CLK	T
0	0
1	1
0	1
1	0
0	1
1	0

EXAM QUESTION | T Flip-Flop

Assuming that the flip-flop is initially in the SET state, what will the state of a falling edge-triggered T flip-flop be at the end of the following sequence of inputs?

~~A. SET~~

B. RESET

~~C. INVALID~~

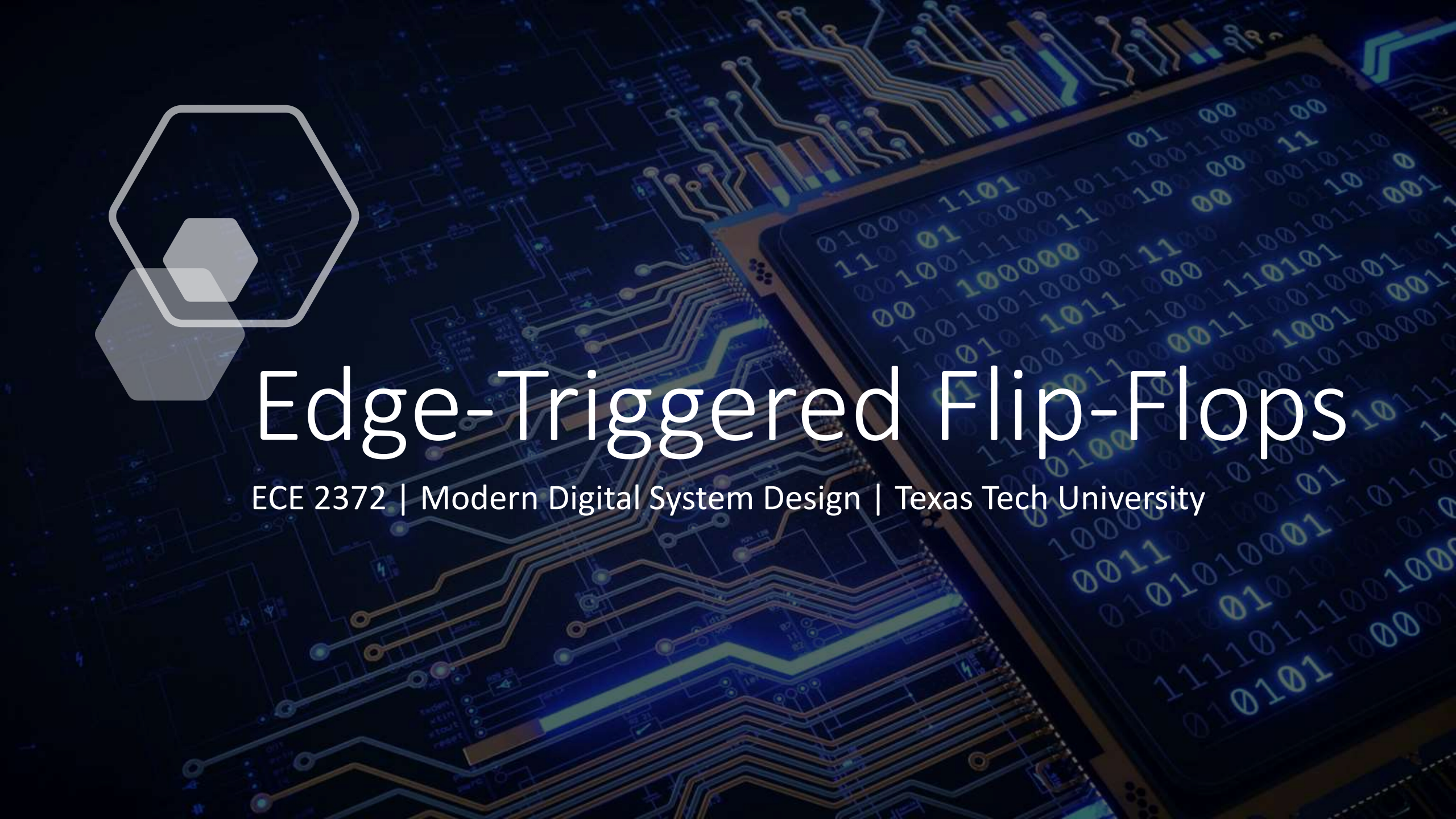
~~D. UNDEFINED~~

CLK	T	
0	0	SET
1	1	SET
0	1	RESET
1	0	RESET
0	1	RESET
1	0	RESET

Lecture Overview

- The Data (D) Latch
- Edge-Triggered D Flip-Flop
- S-R Flip-Flop
- J-K Flip-Flop
- T Flip-Flop

What questions do you have?



Edge-Triggered Flip-Flops

ECE 2372 | Modern Digital System Design | Texas Tech University