Registers and Register Transfers

ECE 2372 | Modern Digital System Design | Texas Tech University

Lecture Overview

- D Flip-Flop Register
- Registers with Clear and Load Enable
- Data Transfer Between Registers
- **Example:** Parallel Adder with Accumulator

D Flip-Flop Register

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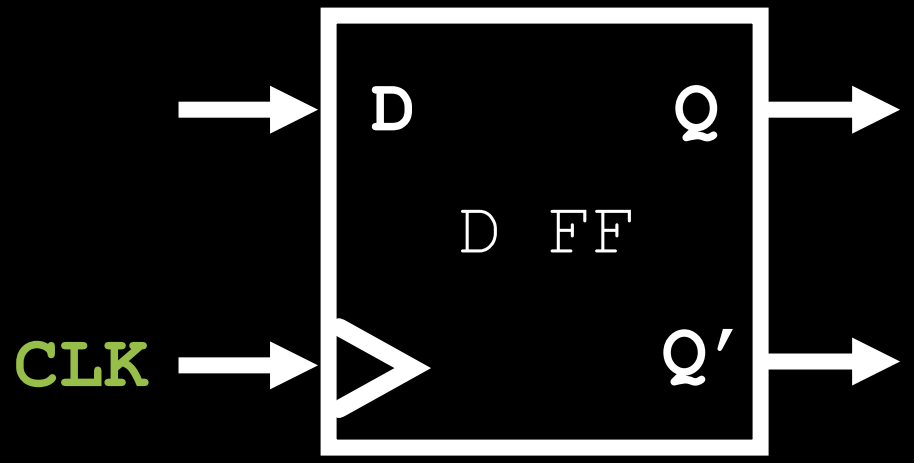
D Flip-Flop Register

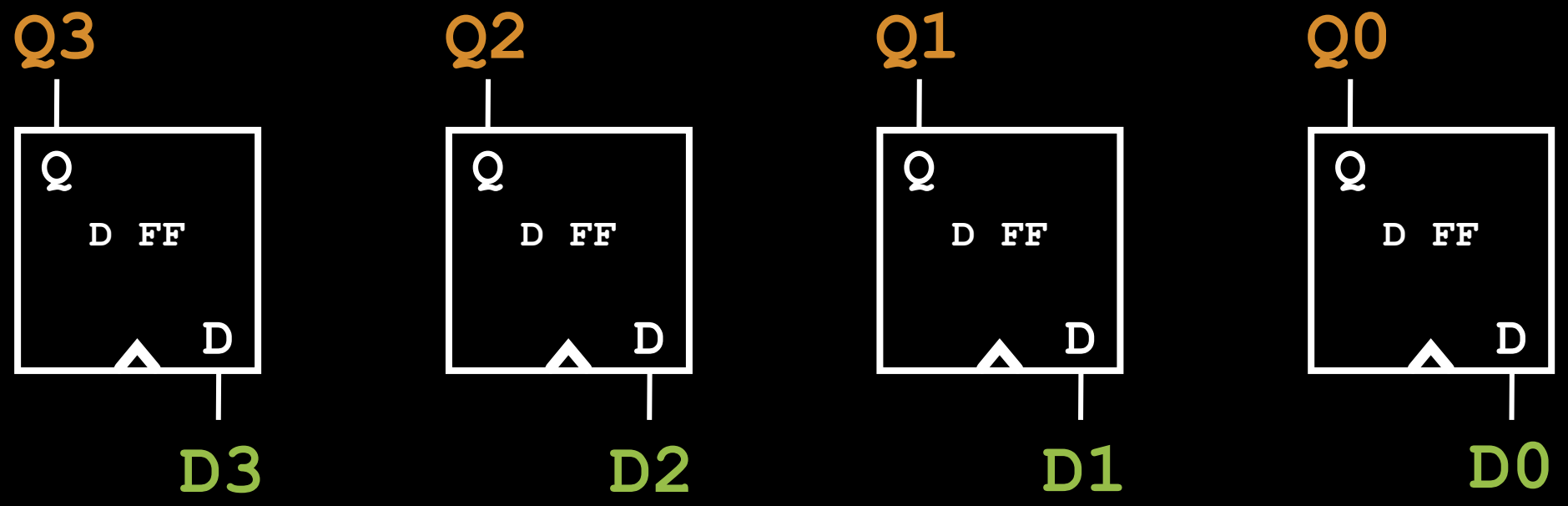
- We have seen that a D Flip-Flop can be used to store a single bit.



$$Q^+ = D$$

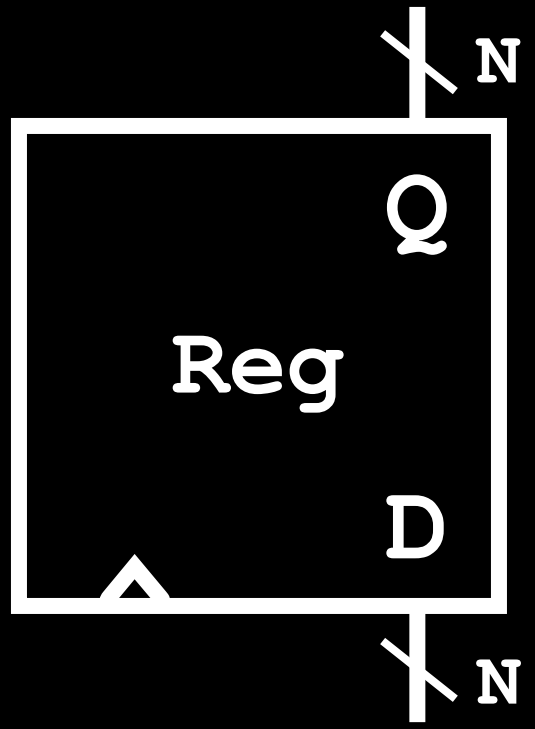
D Flip-Flop Register

- To store an N-bit binary number, we simply need N, D Flip-Flops.



D Flip-Flop Register

- We can package up our register to keep our schematics simpler.



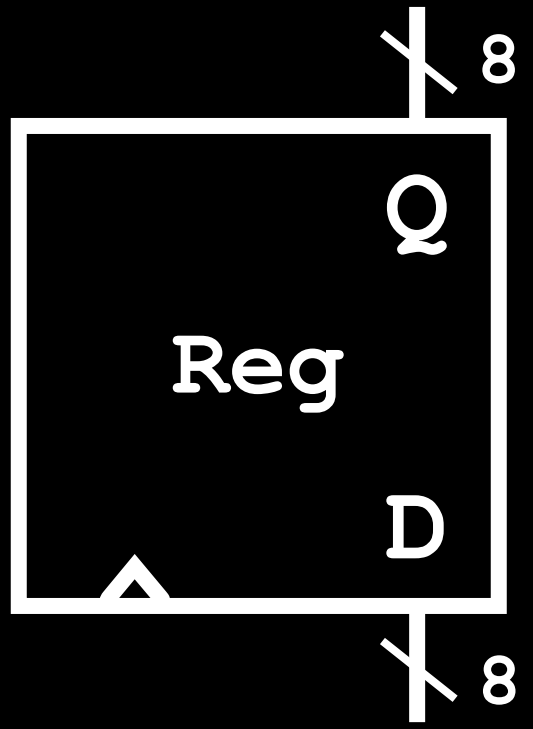
The crossed line labeled “N” indicates an N-bit bus.

What questions do you have?

EXAM QUESTION | D Flip-Flop Register

How many D Flip-Flops are present in the given register?

A. 1
B. 4
C. 8
D. 16



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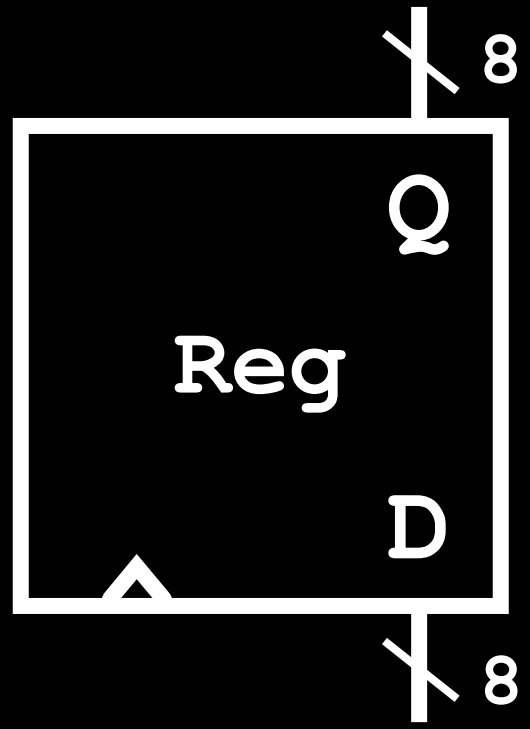

Registers with Clear and Load Enable

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Registers with Clear and Load Enable

- In addition to being able to store binary data, there are two additional bits of functionality that we want to add.

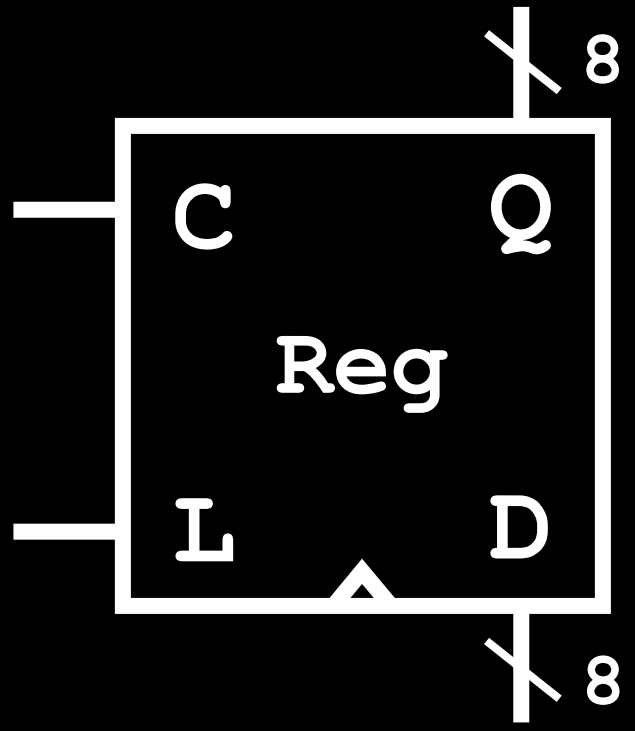
1. The ability to control when data may be written to the register.
2. The ability to quickly write zeros to all the flip-flops.

Registers with Clear and Load Enable

Let's add two control inputs to the register table.

Clear	Load	Data	Q+
0	0	0	Q
0	0	1	Q
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Registers with Clear and Load Enable



What questions do you have?

EXAM QUESTION | Clear and Load Enable

What will the next state of a register be with the following inputs?

A. Q
B. D
C. Zeros
D. X

```
C = 0
L = 1
```

EXAM QUESTION | Clear and Load Enable

What will the next state of a register be with the following inputs?

~~A. Q~~

B. D

~~C. 0~~

~~D. X~~

```
C = 0
L = 1
```

Data Transfer Between Registers

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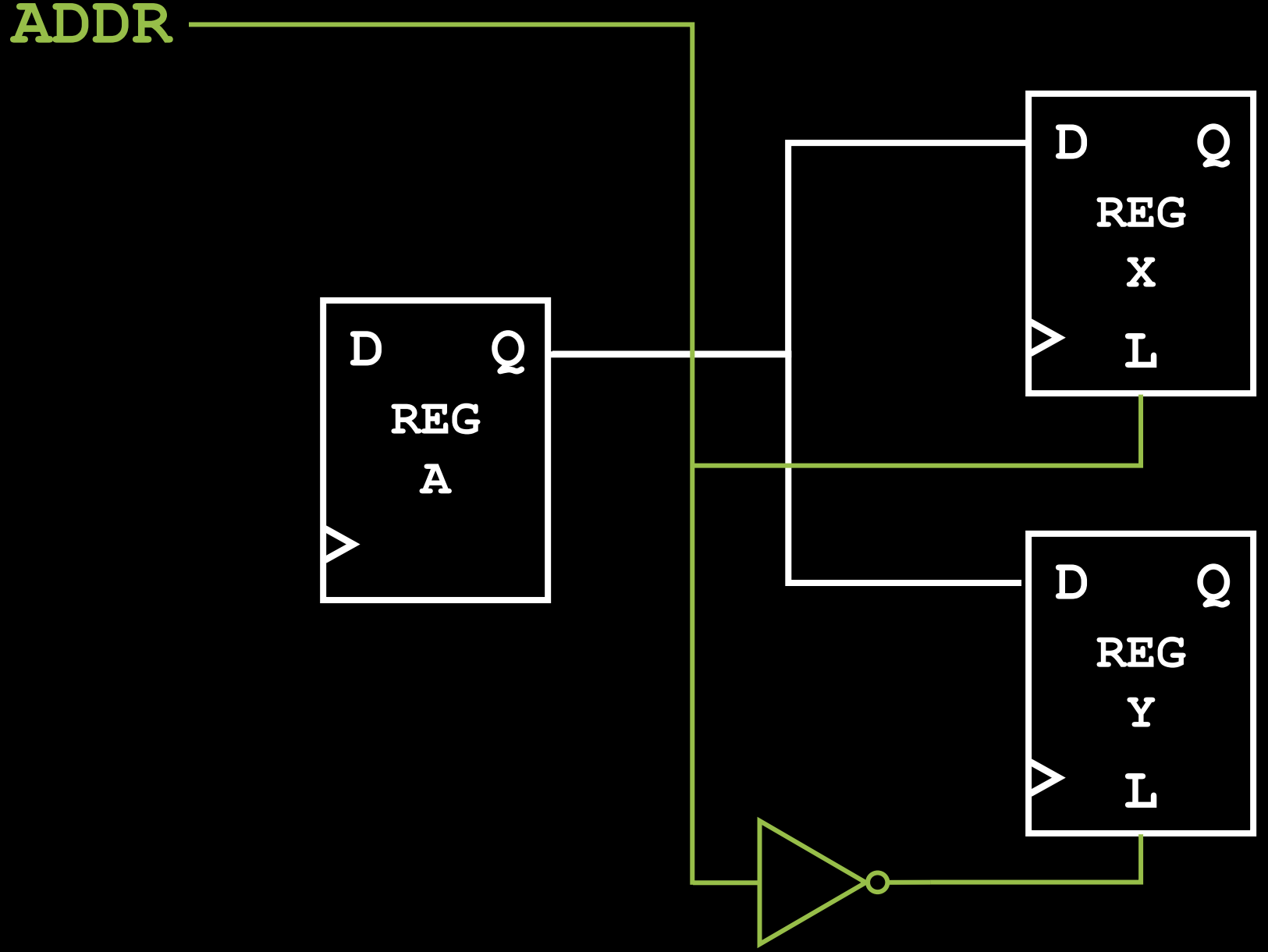
Data Transfer Between Registers

The majority of the work done in digital systems is simply passing binary data between different registers.

This work is called Register Transfer Operations.



If ADDR is 1, Reg X will be loaded with the value stored at A.

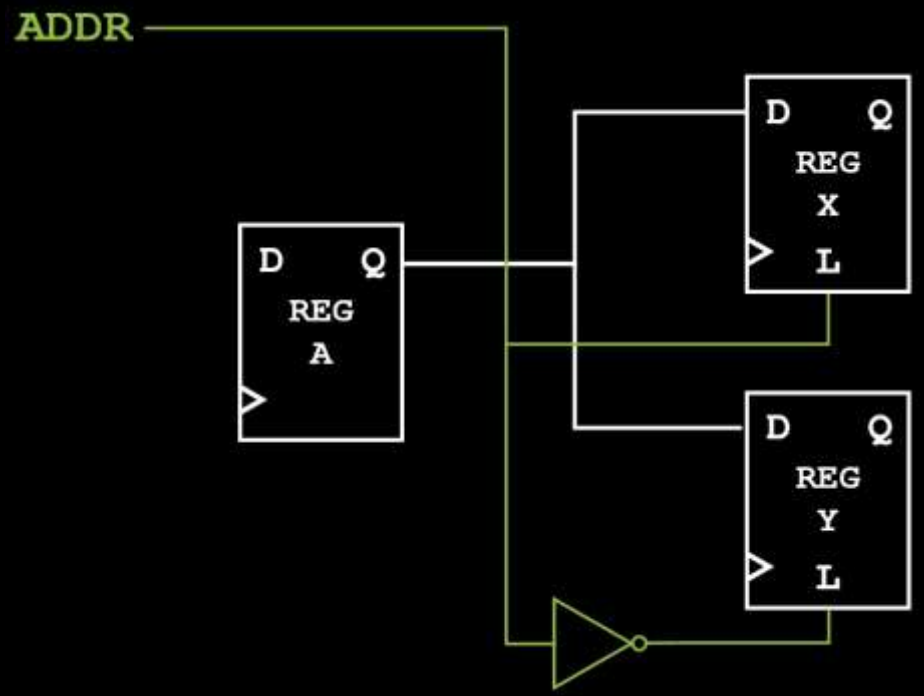
If ADDR is 0, Reg y will be loaded with the value stored at A.

Data Transfer Between Registers

Consider the following commands, what effect will they have on the circuit from the previous slide?

```
LOAD X;

LOAD Y;
```

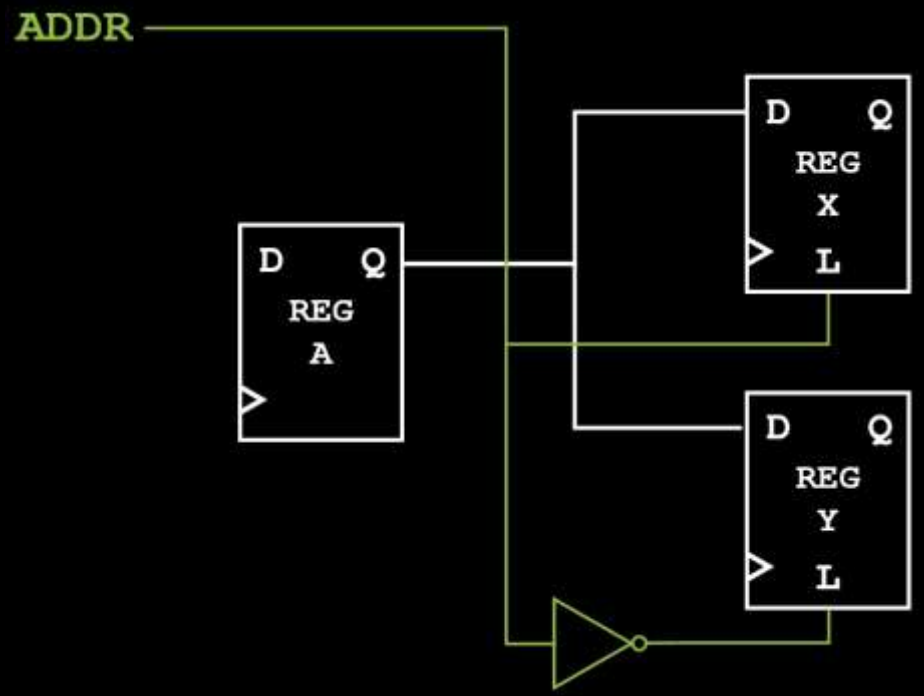


Data Transfer Between Registers

Consider the following commands, what effect will they have on the circuit from the previous slide?

```
LOAD X;
```
Sets ADDR = 1

```
LOAD Y;
```

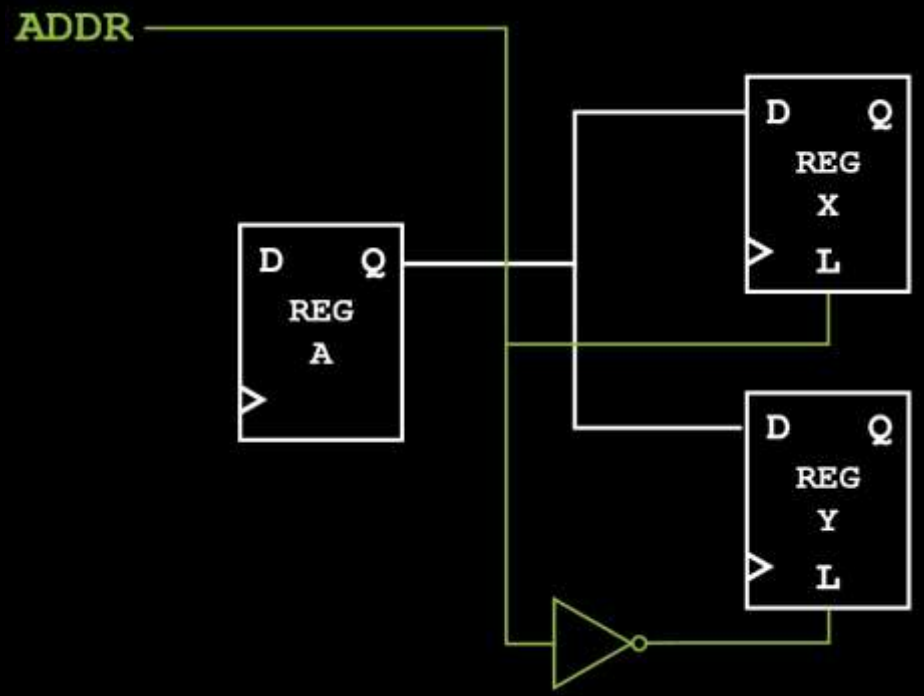


Data Transfer Between Registers

Consider the following commands, what effect will they have on the circuit from the previous slide?

`LOAD X;` Sets ADDR = 1

`LOAD Y;` Sets ADDR = 0



Congratulations!

We have finally written our first line of code!

```
LOAD X;
```

It’s not much, but it counts.

This type of low-level programming is called **ASSEMBLY**.

What questions do you have?

EXAM QUESTION | Register Transfers

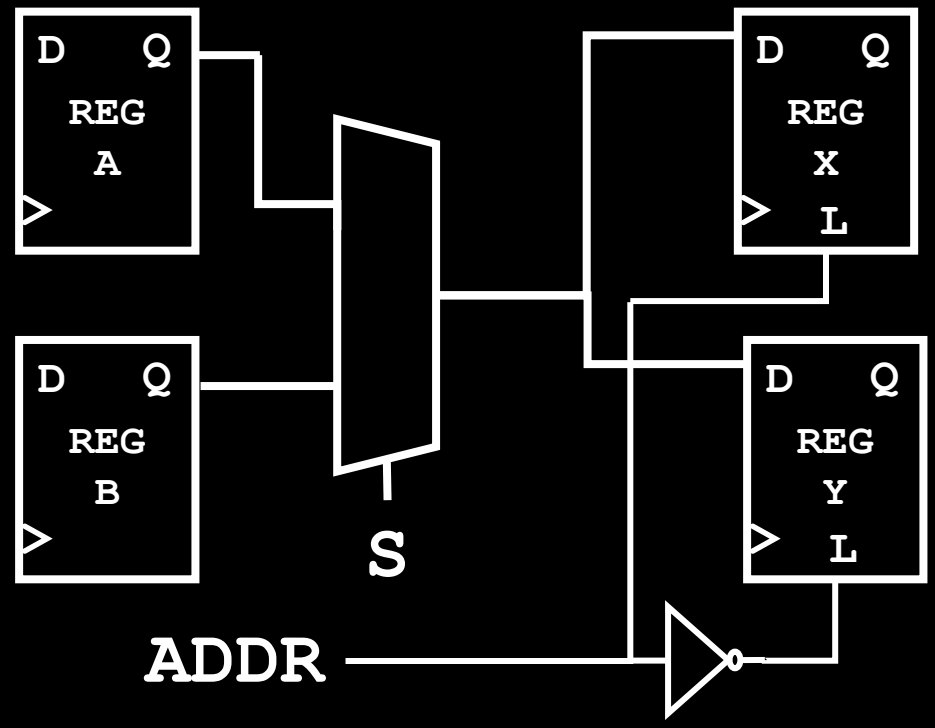
For the given register circuit, how will the command `LOAD X B;` effect the control inputs `S` and `ADDR`?

A. `S=0,ADDR=0`

B. `S=0,ADDR=1`

C. `S=1,ADDR=0`

D. `S=1,ADDR=1`



EXAM QUESTION | Register Transfers

For the given register circuit, how will the command `LOAD X B;` effect the control inputs `S` and `ADDR`?

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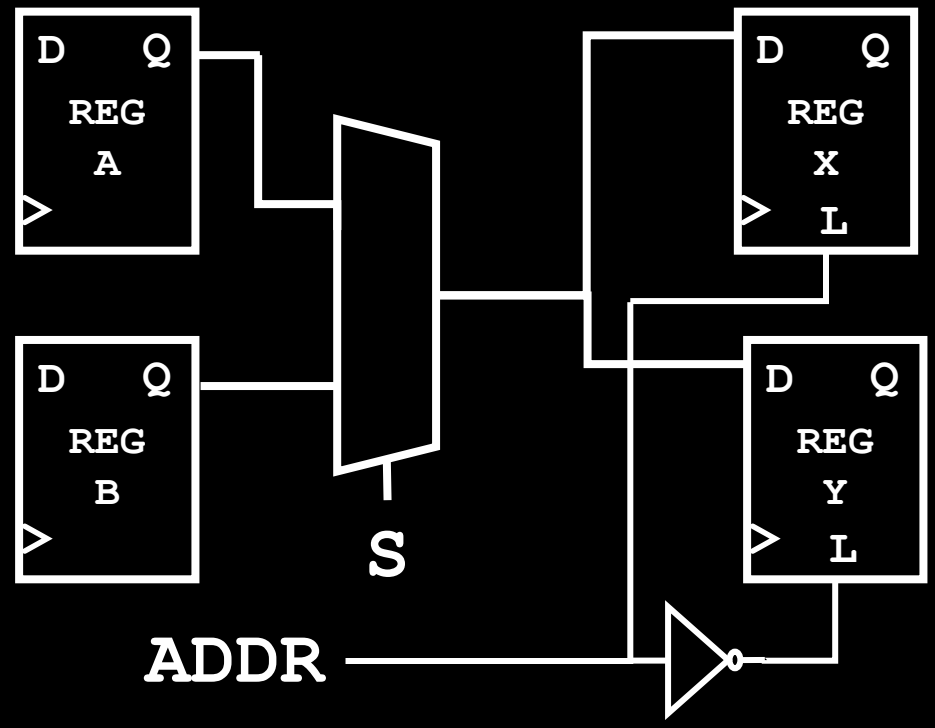
~~B. S=0,ADDR=1~~

~~C. S=1,ADDR=0~~

D. S=1,ADDR=1



Example: Parallel Adder with Accumulator

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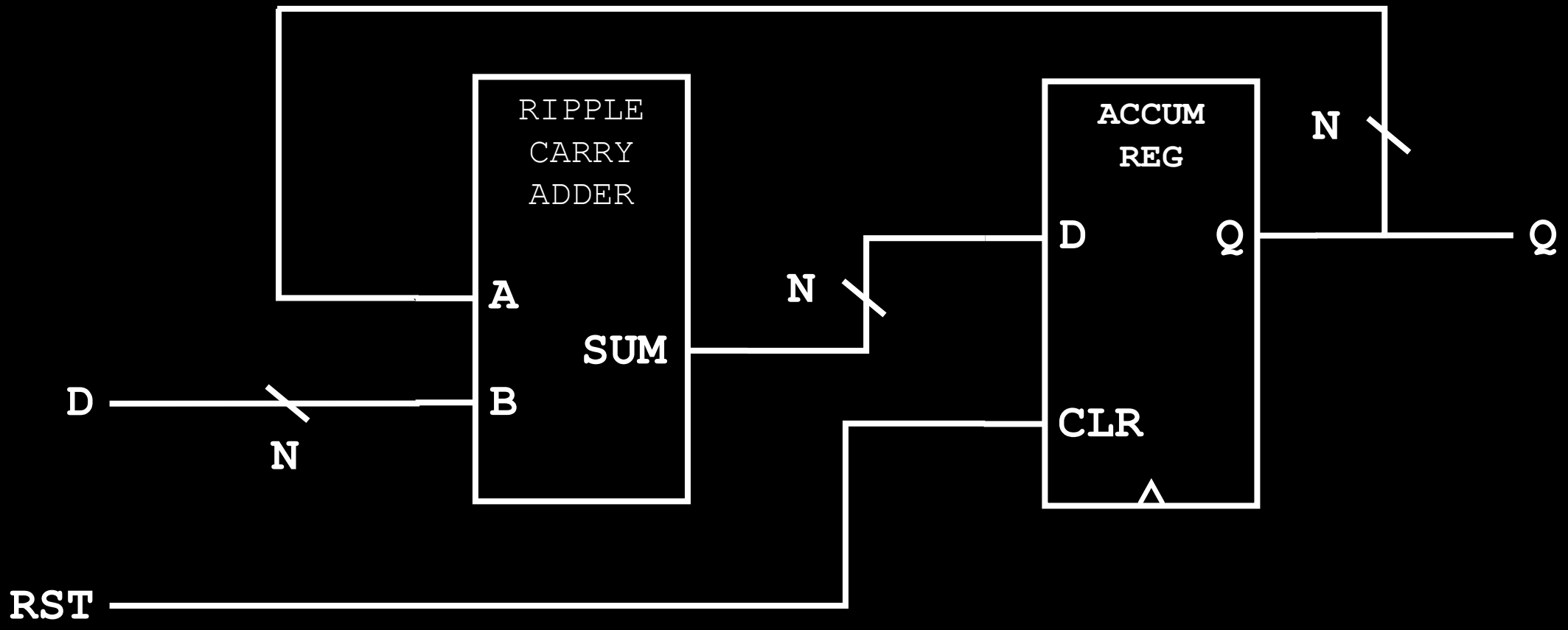
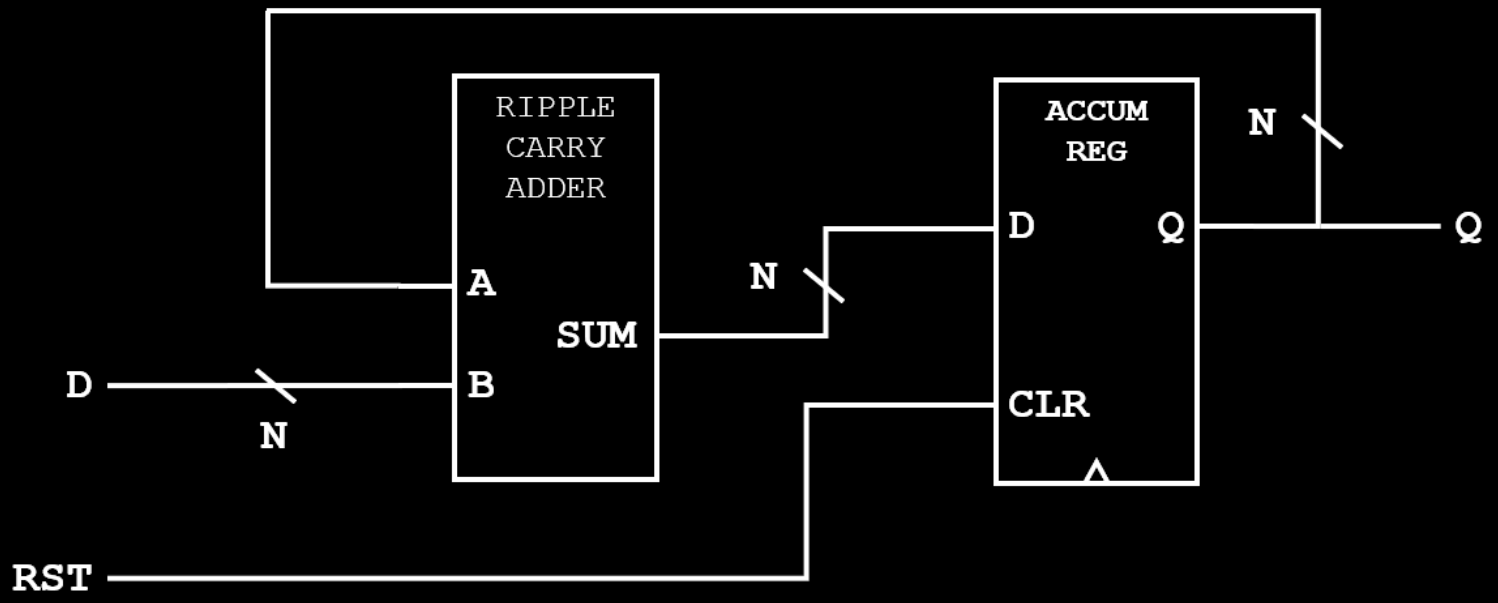
Parallel Adder with Accumulator

- Let's expand on our Ripple-Carry Adder and give it the ability to store the results in an accumulator.

Parallel Adder with Accumulator



What sequence of inputs will result in the operation 3 x 3 = 9?



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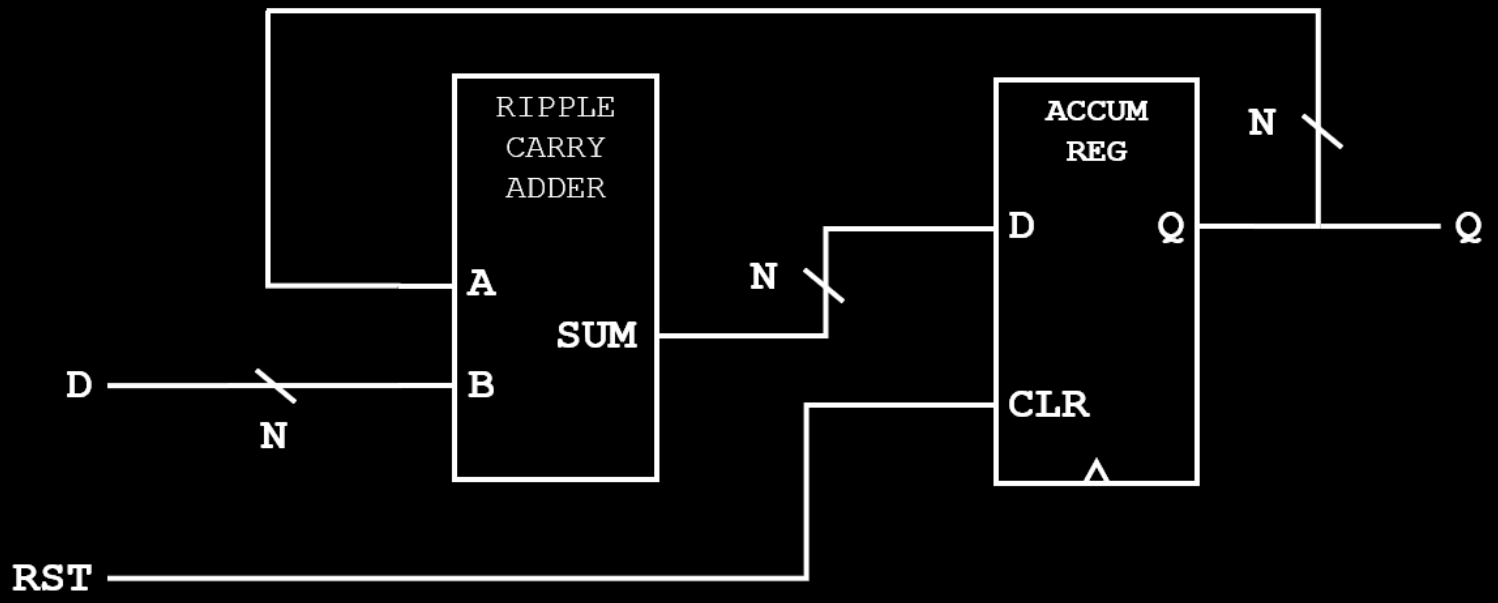

D	RST	Q

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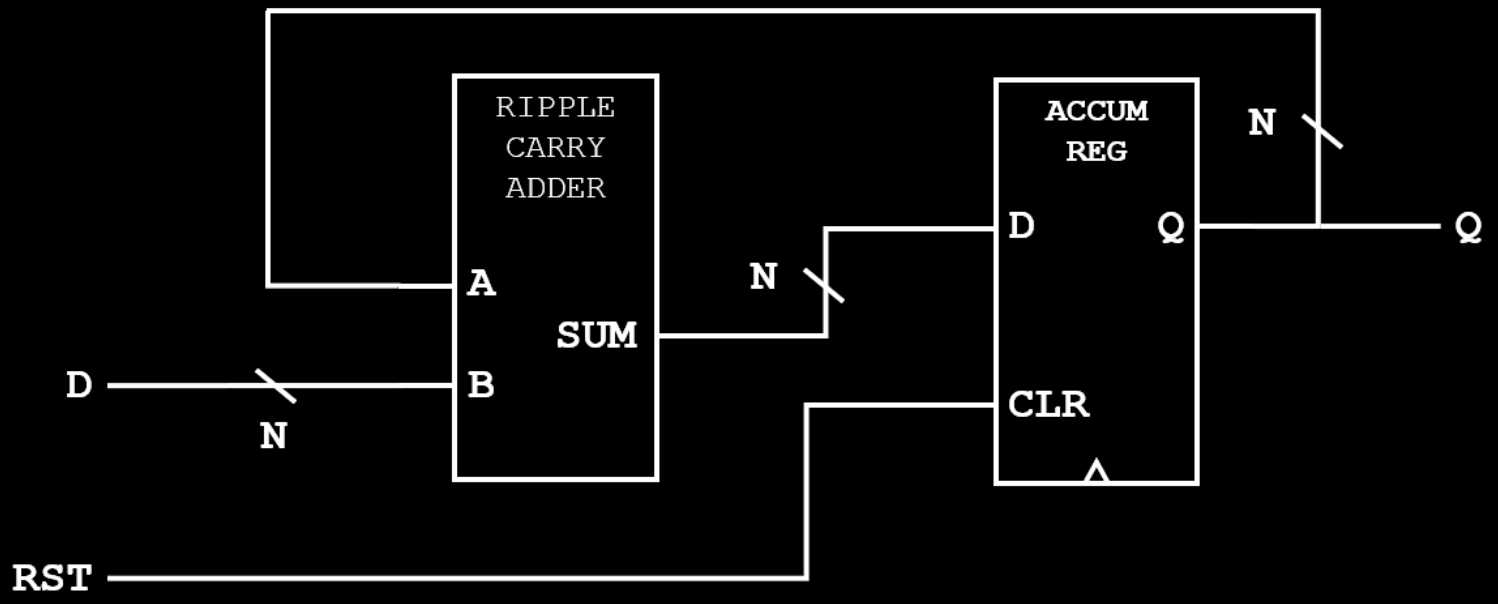
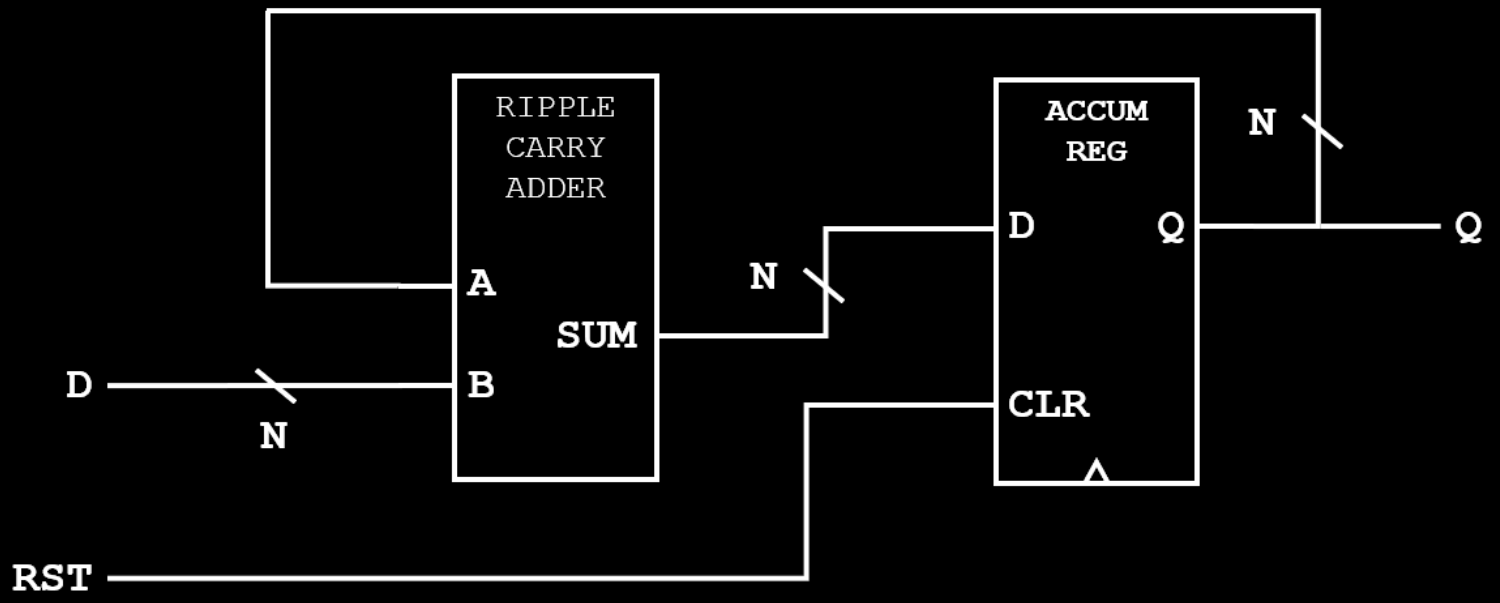


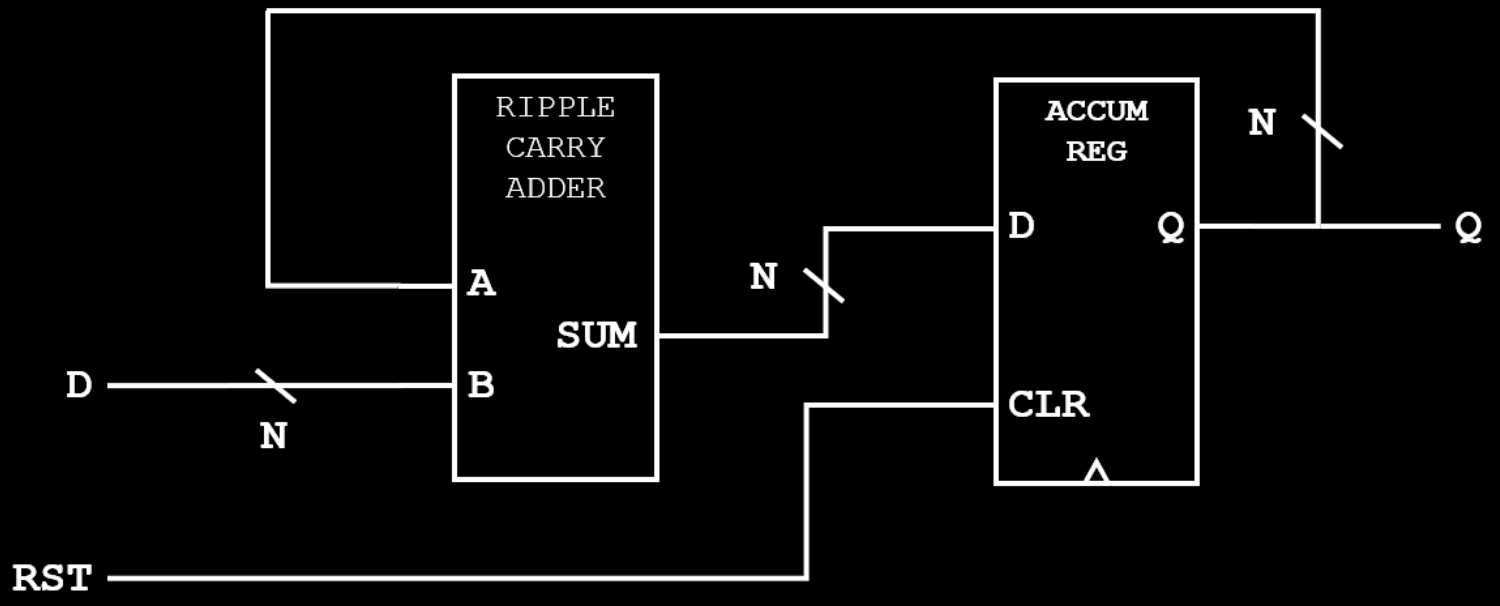
D	RST	Q
X	1	0

What sequence of inputs will result in the operation 3 x 3 = 9?



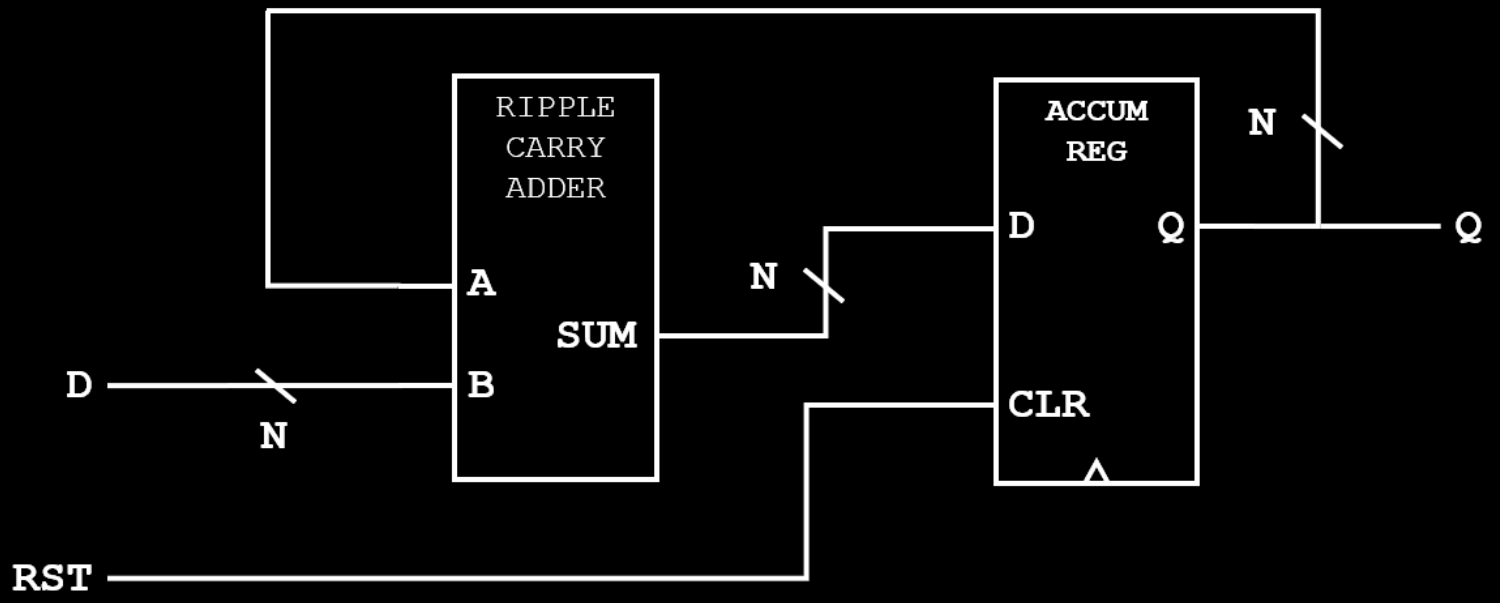
D	RST	Q
X	1	0
3	0	3

What sequence of inputs will result in the operation 3 x 3 = 9?



D	RST	Q
X	1	0
3	0	3
3	0	6

What sequence of inputs will result in the operation 3 x 3 = 9?



D	RST	Q
X	1	0
3	0	3
3	0	6
3	0	9

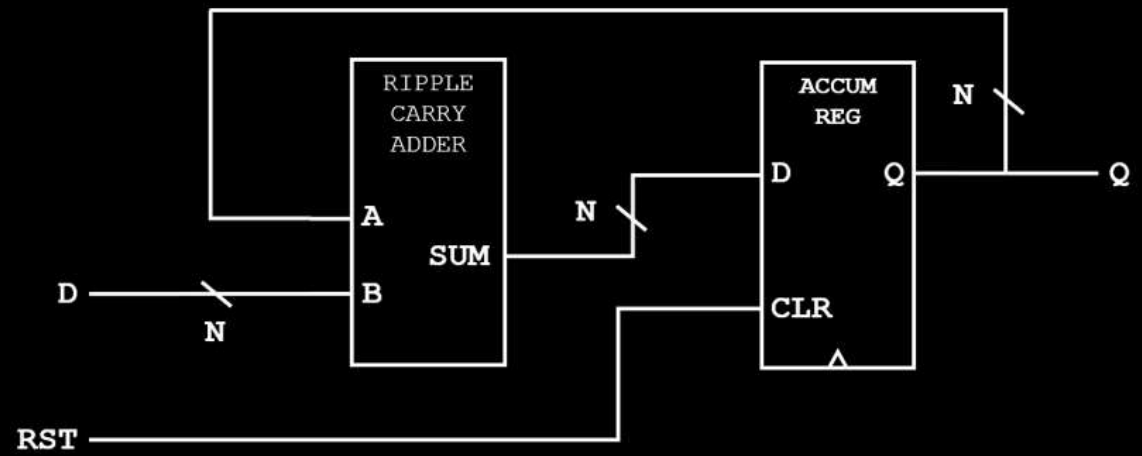
What questions do you have?

EXAM QUESTION | Adder with Accumulator

What will be the output of a Parallel Adder with Accumulator at the end of the following sequence of inputs?

1. 13
2. 7
3. 28
4. 18

D	RST
1	1
2	0
3	1
4	1
5	0
6	0
7	0



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D	RST	Q
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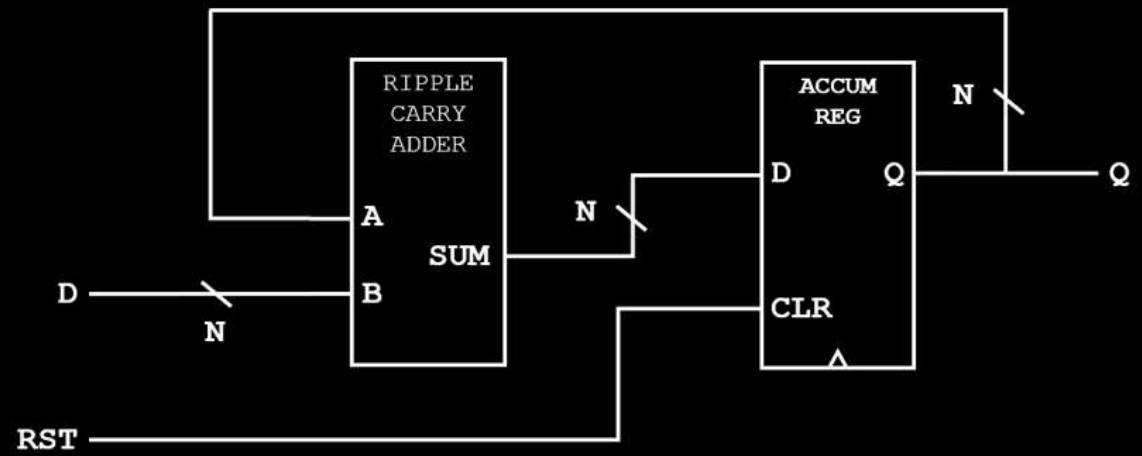
2	0	
3	1	
4	1	
5	0	
6	0	
7	0	



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2	0	
3	1	
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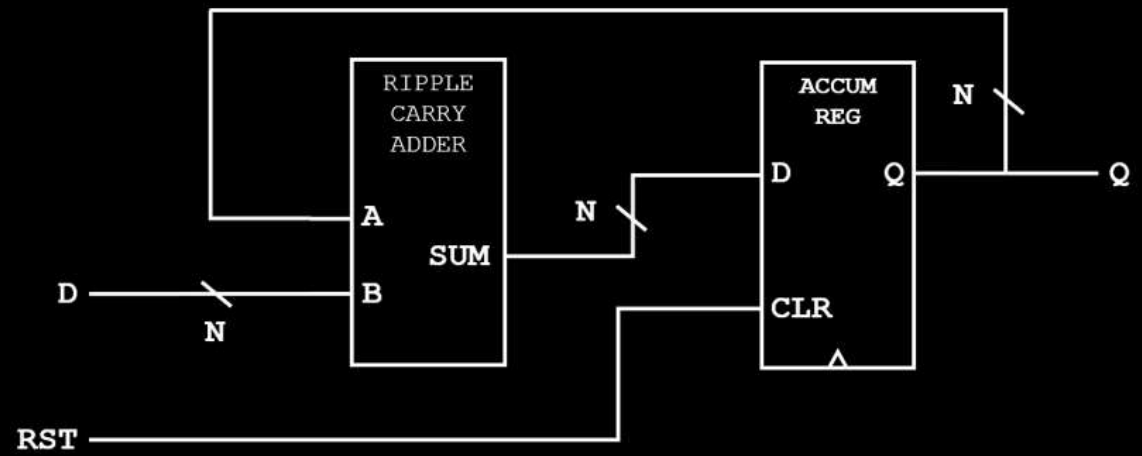
5	0	
6	0	
7	0	



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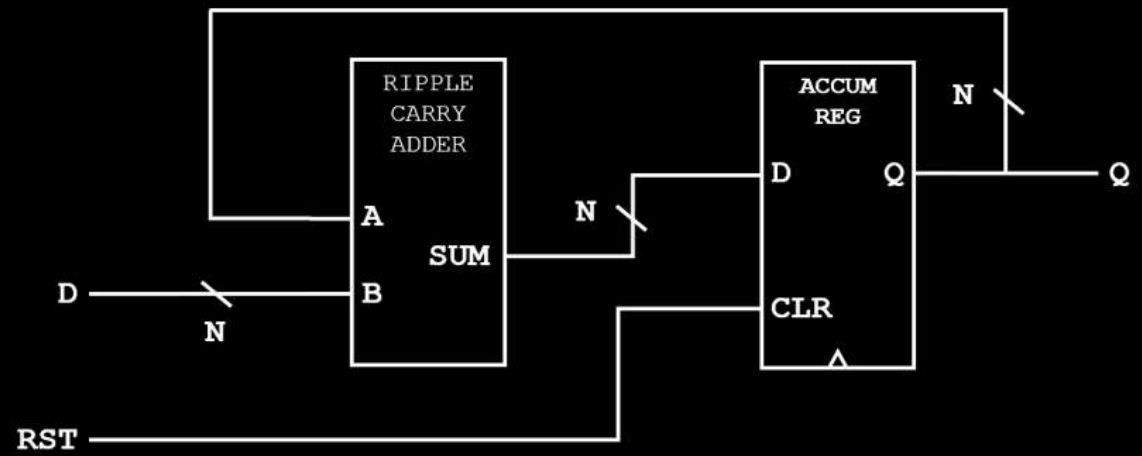
D	RST	Q
1	1	0
2	0	2
3	1	
4	1	
5	0	
6	0	
7	0	



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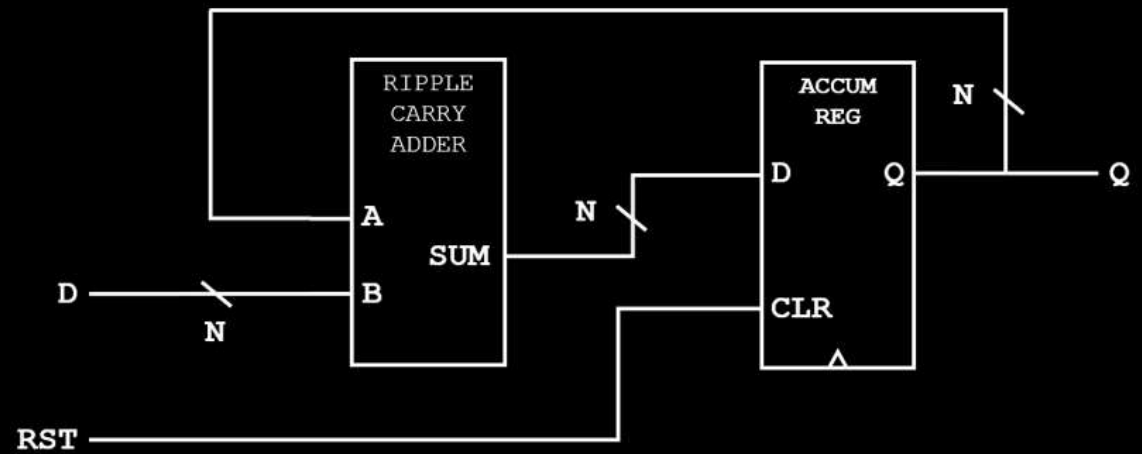
6	0	
7	0	



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6	0	
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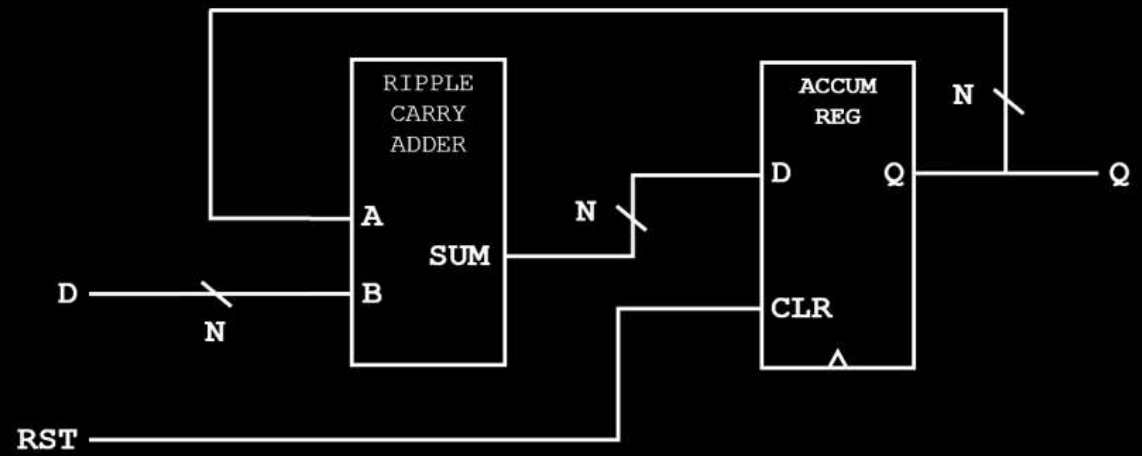

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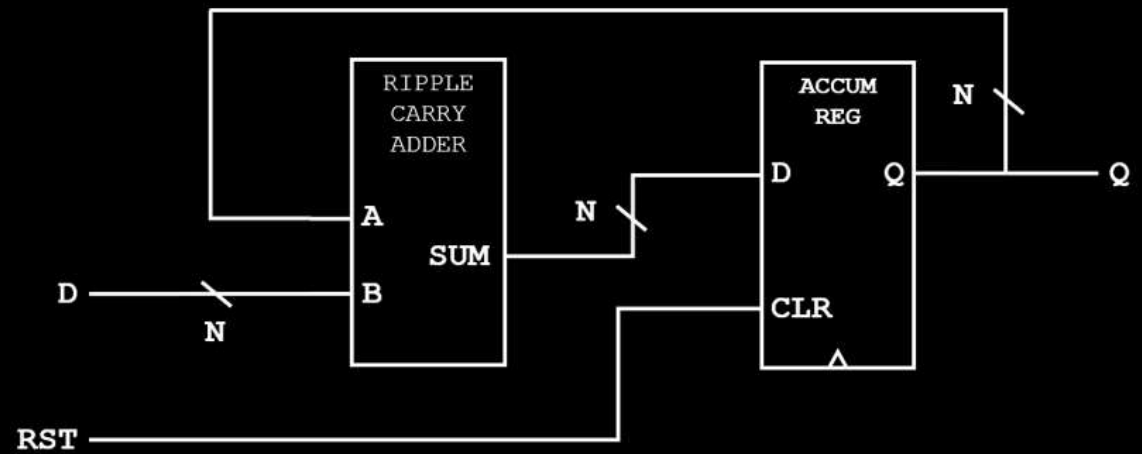
5	0	5
6	0	
7	0	



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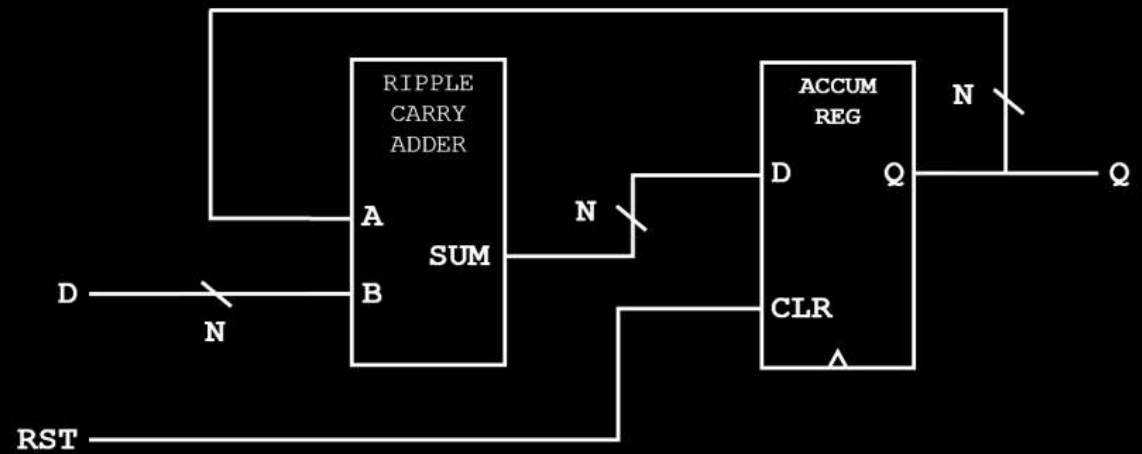
D	RST	Q
1	1	0
2	0	2
3	1	0
4	1	0
5	0	5
6	0	11
7	0	



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1	1	0
2	0	2
3	1	0
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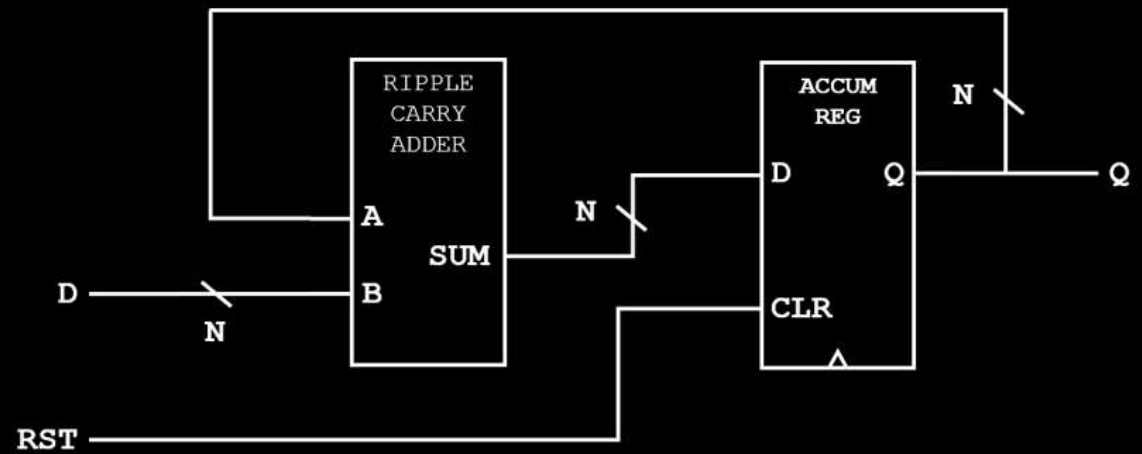
5	0	5
6	0	11
7	0	18



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