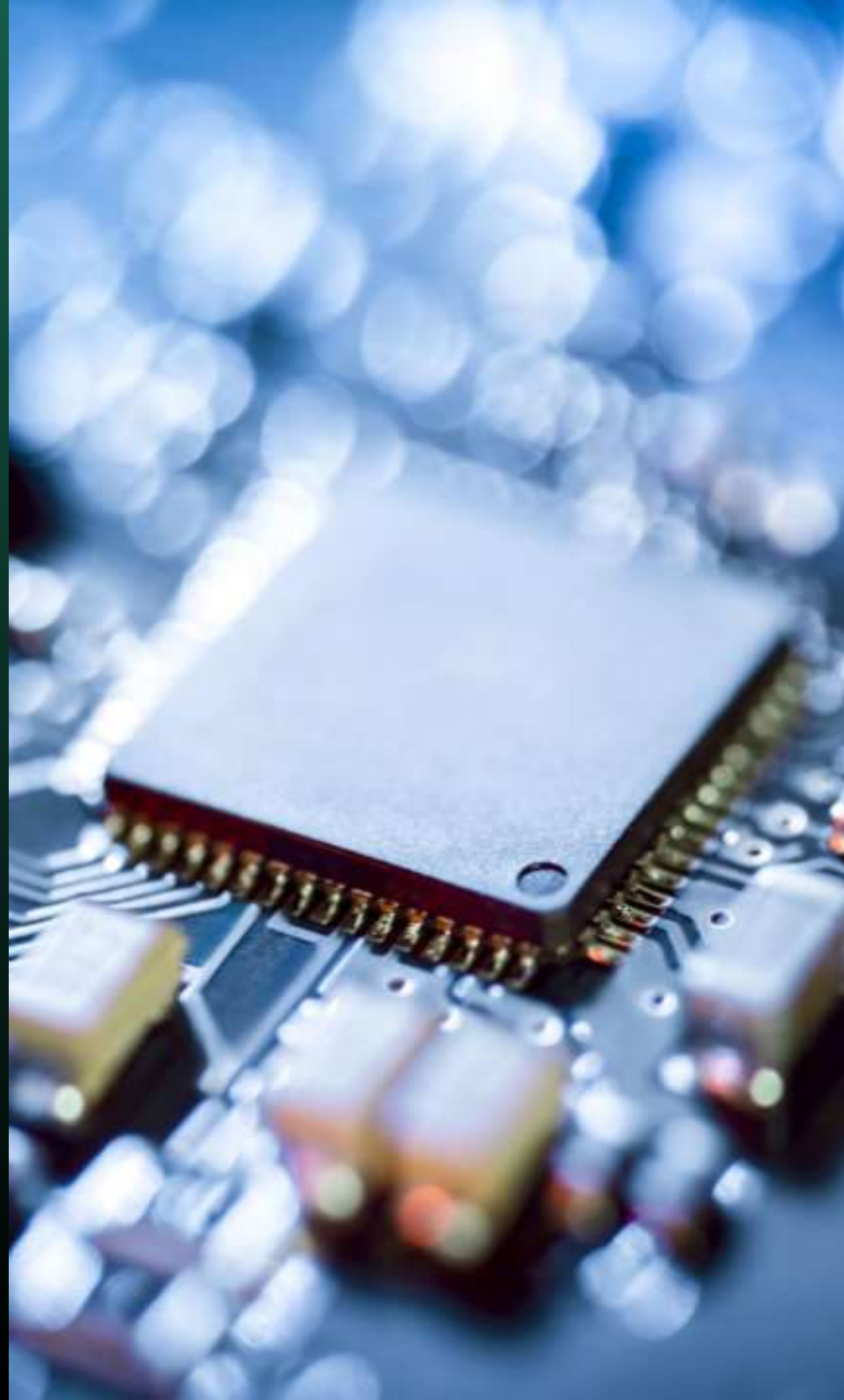
ECE 2372 | Modern Digital System Design | Texas Tech University

Latches



Lecture Overview

1. Combinational vs Sequential Logic
2. Dominant Inputs
3. Set-Reset Latch
4. Set’-Reset’ Latch
5. Gated Set-Reset Latch

Combinational vs Sequential Logic

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Combinational vs Sequential Logic

So far, we've been working with **combinational logic**.

Combinational vs Sequential Logic

Sequential Logic builds on this model by adding State.

Combinational vs Sequential Logic

To make this work, we need a logic circuit that maintain the state.
Even if the input signal changes.

Dominant Input Signals

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Dominant Input Signals

The logic gates AND, NAND, OR, and NOR have truth tables with a similar pattern.

A	B	AND
0	0	0
0	1	0
1	0	0
1	1	1

A	B	OR
0	0	0
0	1	1
1	0	1
1	1	1

Dominant Input Signals

The dominant input signal, either 1 or 0, is the signal which drives the logic gate to a specific state if it appears anywhere in the input.

A	B	AND
0	0	0
0	1	0
1	0	0
1	1	1

For the AND-gate, notice that a 0 anywhere drives the gate to 0.

Dominant Input Signals

The dominant input signal, either 1 or 0, is the signal which drives the logic gate to a specific state if it appears anywhere in the input.

A	B	AND
0	0	0
0	1	0
1	0	0
1	1	1

For the AND-gate, notice that a 0 anywhere drives the gate to 0.

0 is the dominant signal for an AND-gate.

Dominant Input Signals

A	B	OR
0	0	0
0	1	1
1	0	1
1	1	1

For the OR-gate, notice that a 1 anywhere drives the gate to 1.

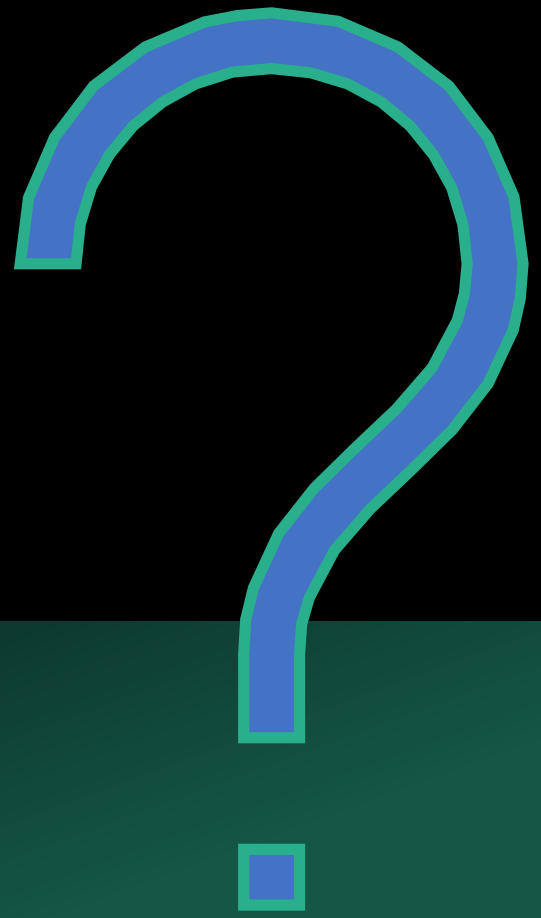
Dominant Input Signals

A	B	OR
0	0	0
0	1	1
1	0	1
1	1	1

For the OR-gate, notice that a 1 anywhere drives the gate to 1.

1 is the dominant input signal for the OR-gate.

What questions do you have?



EXAM PROBLEM | Dominant Input Signals

What is the dominant input signal for the NOR-gate?

A. 1
B. 0
C. The NOR-gate does not have a dominant input signal.

EXAM PROBLEM | Dominant Input Signals

What is the dominant input signal for the NOR-gate?

A. 1

~~B. 0~~

~~C. The NOR-gate does not have a dominant input signal~~.

A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

Set-Reset Latch

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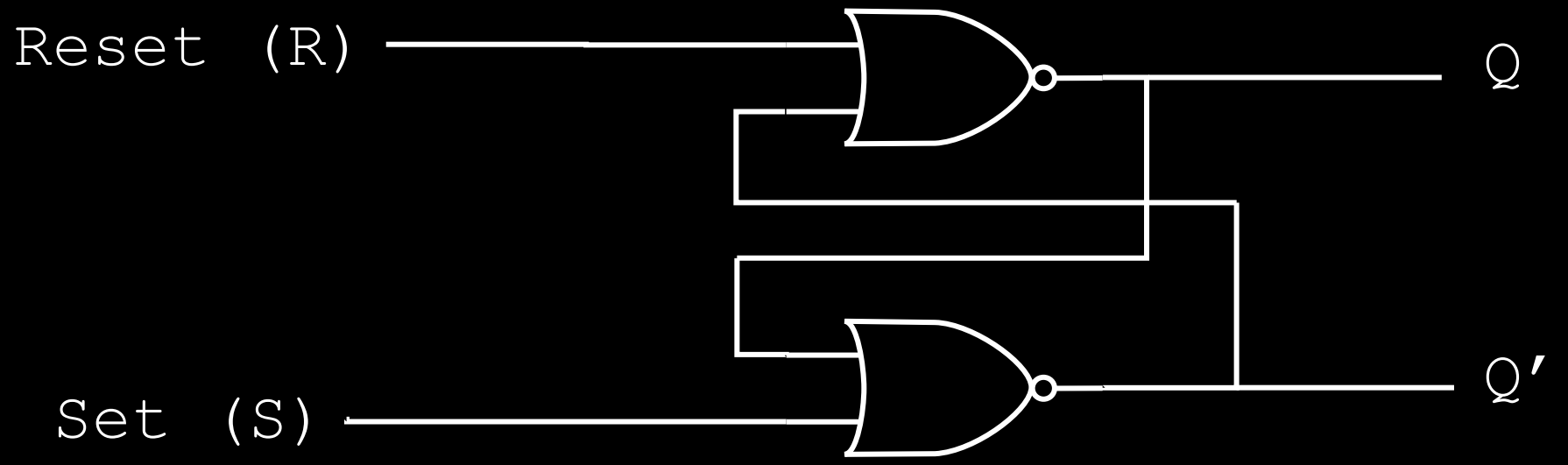
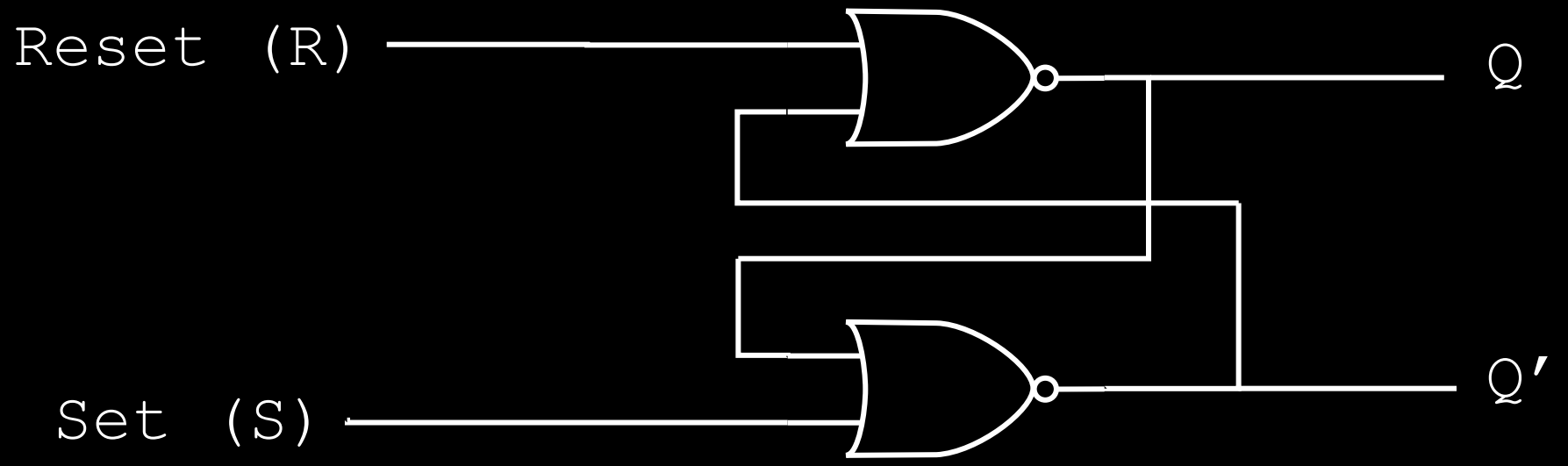
Set-Reset Latch



By convention, we use Q to represent the state of the latch.

Set-Reset Latch



By convention, we use Q to represent the state of the latch.

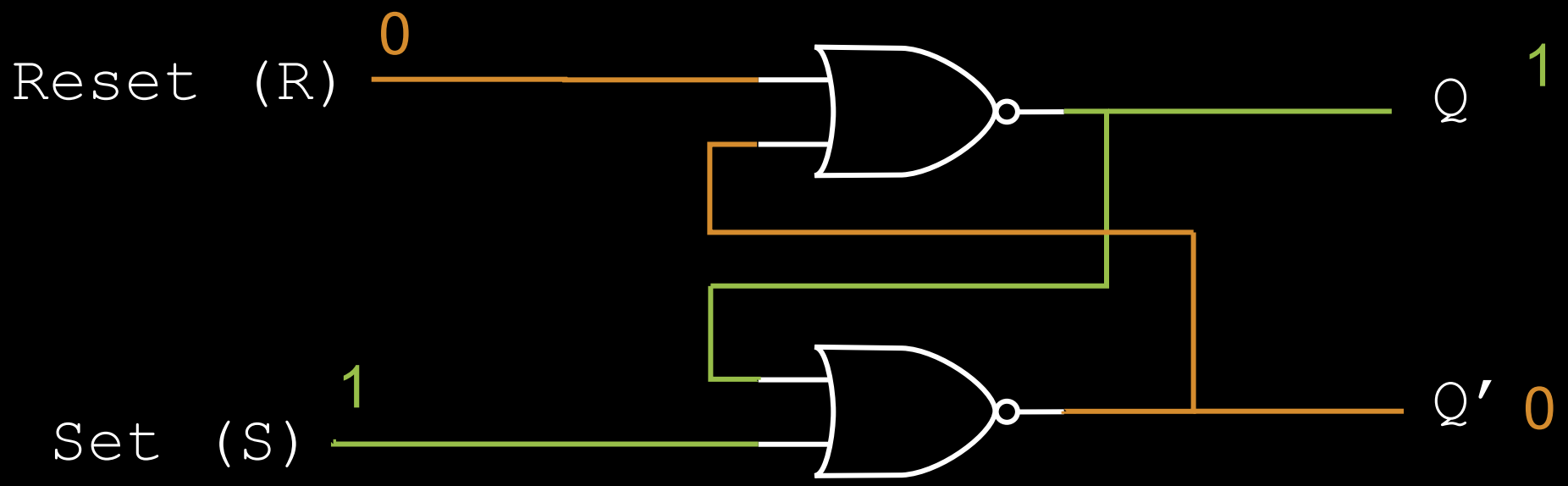
Q = 1 (SET), Q = 0 (RESET)

Set-Reset Latch

1 | 0

Set-Reset Latch

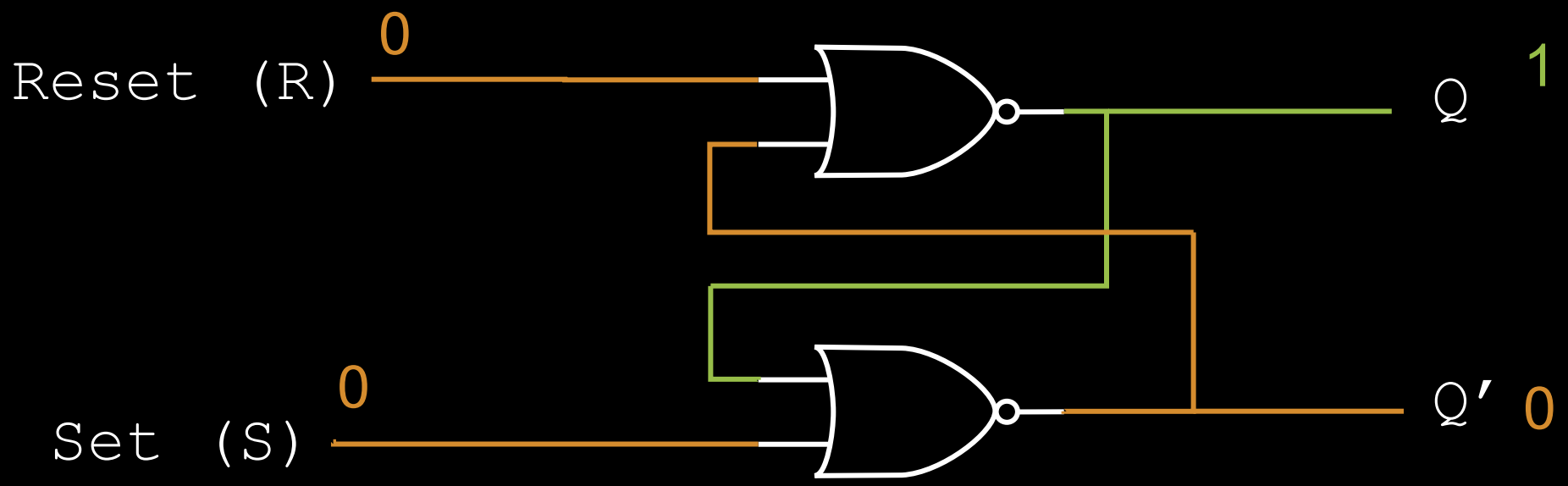
1 | 0



Since NOR is dominated by 1, we must have a 0 on the output of the bottom NOR-gate.

Set-Reset Latch

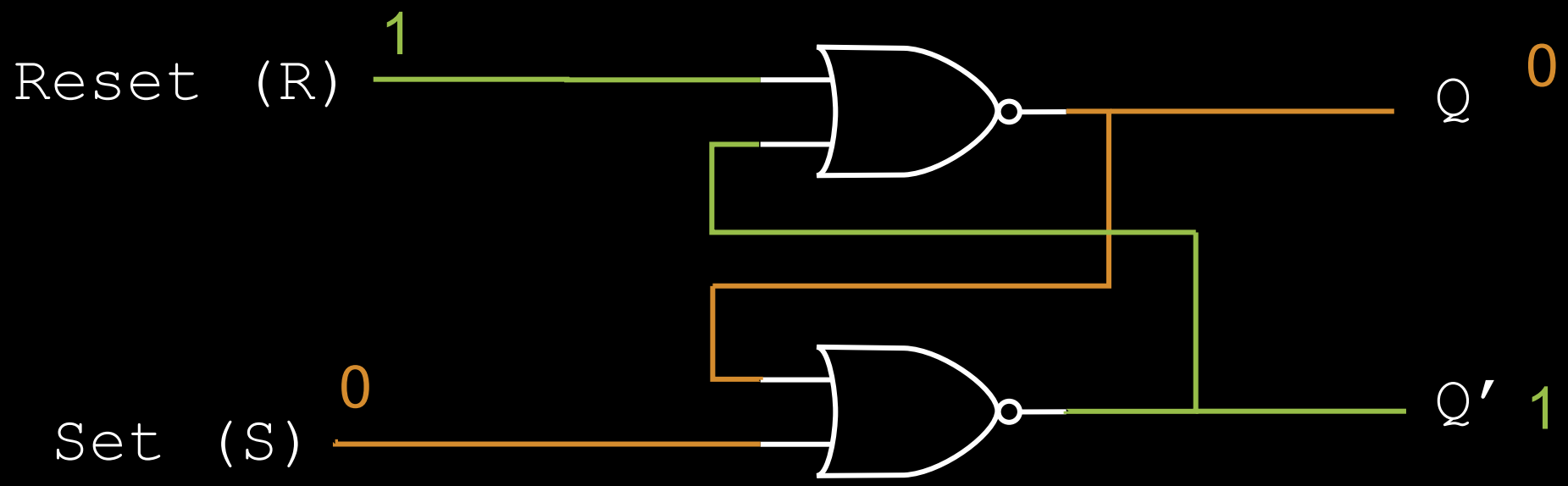
1 | 0



The 1 from Q will continue to dominate the bottom NOR-gate.
Our SET state is maintained, even with all 0’s on the input.

Set-Reset Latch

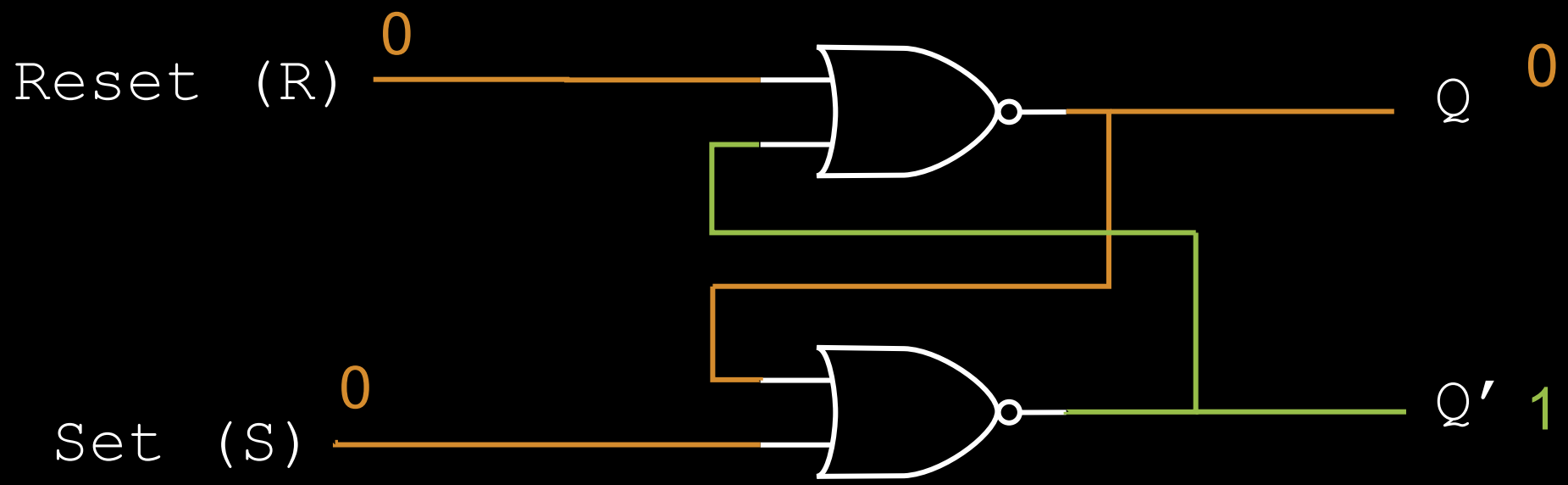
1 | 0



Since NOR is dominated by 1, we must have a 0 on the output of the top NOR-gate.

Set-Reset Latch

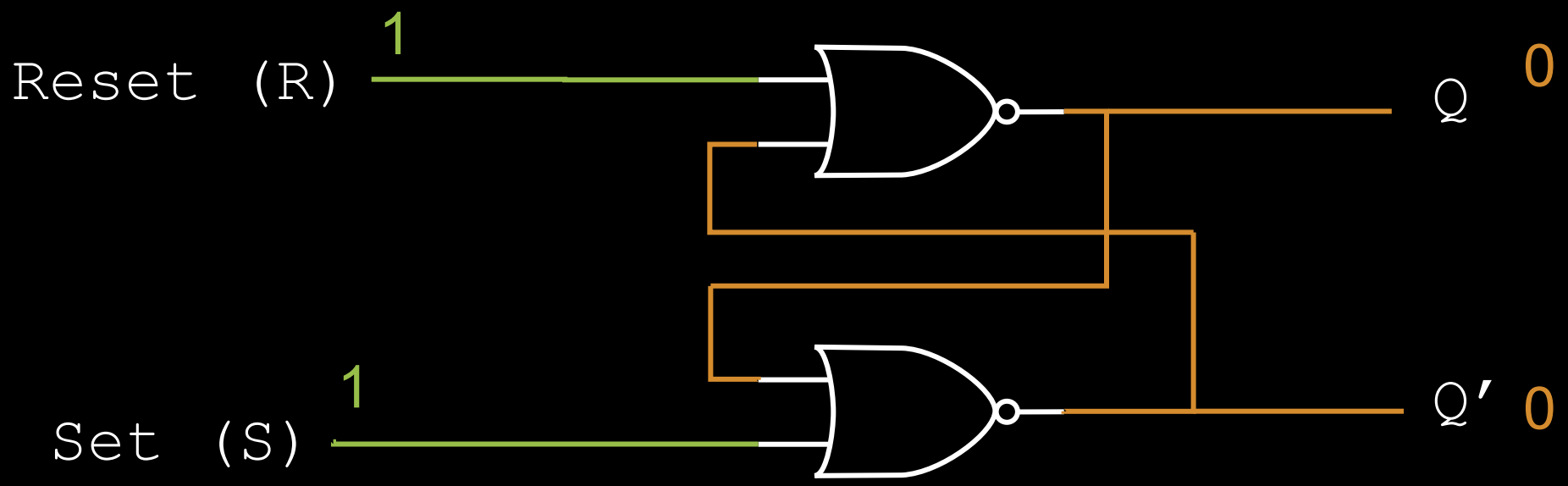
1 | 0



The 1 from Q’ will continue to dominate the top NOR-gate.
Our RESET state is maintained, even with all 0’s on the input.

Set-Reset Latch

1 | 0

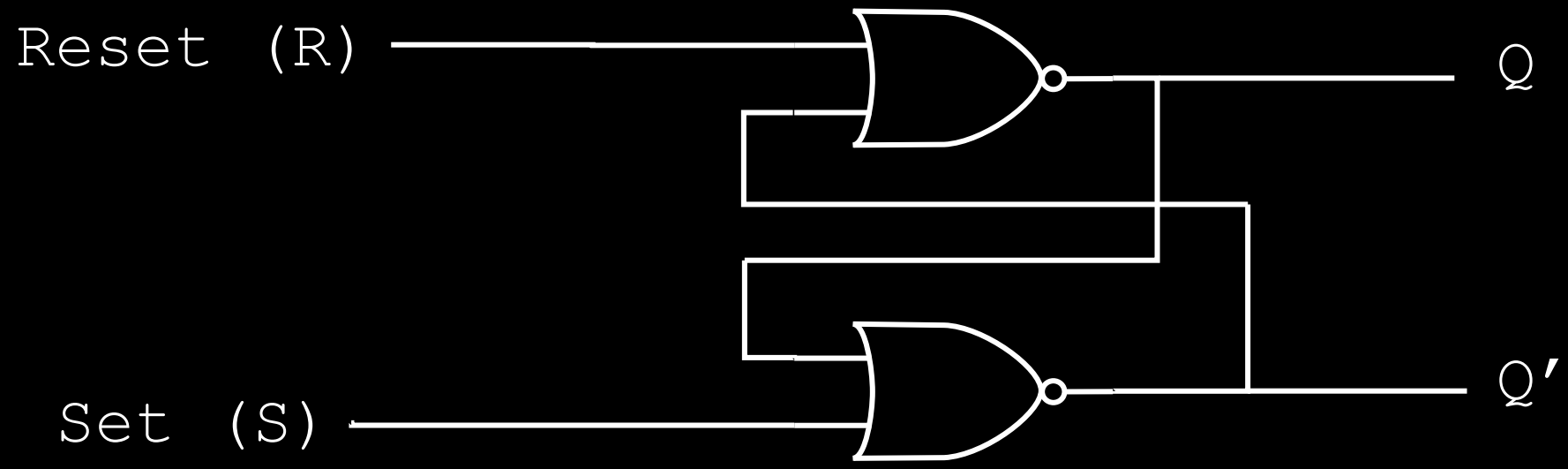


By applying the dominant input to both inputs, both NOR-gates are forced to 0. Since, Q and Q’ cannot both be 0, this is an INVALID state.

Set-Reset Latch

Recap

- When both inputs are non-dominant, the state will not change.
- Apply a dominant input to one input to SET/RESET the state.
- Applying the dominant input on both inputs yields an INVALID STATE



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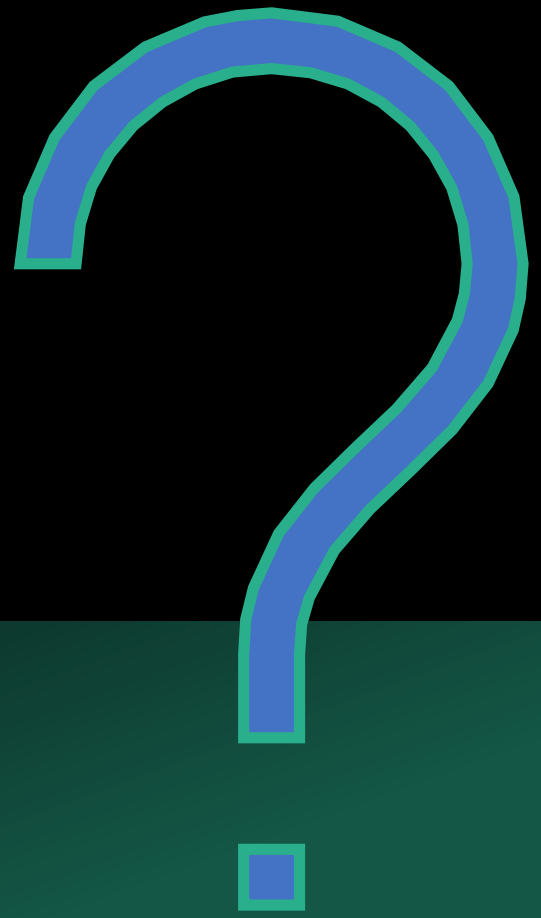

EXAM PROBLEM | Set-Reset Latch

What will be the state of a Set-Reset Latch at the end of the following sequence of inputs?

A. SET
B. RESET
C. INVALID

S	R
1	0
0	0
0	1
1	1
0	0
1	0
0	0

EXAM PROBLEM | Set-Reset Latch

What will be the state of a Set-Reset Latch at the end of the following sequence of inputs?

A. SET

~~B. RESET~~

~~C. INVALID~~

S	R	
1	0	SET
0	0	SET
0	1	RESET
1	1	INVALID
0	0	INVALID
1	0	SET
0	0	SET

Set’-Reset’ Latch

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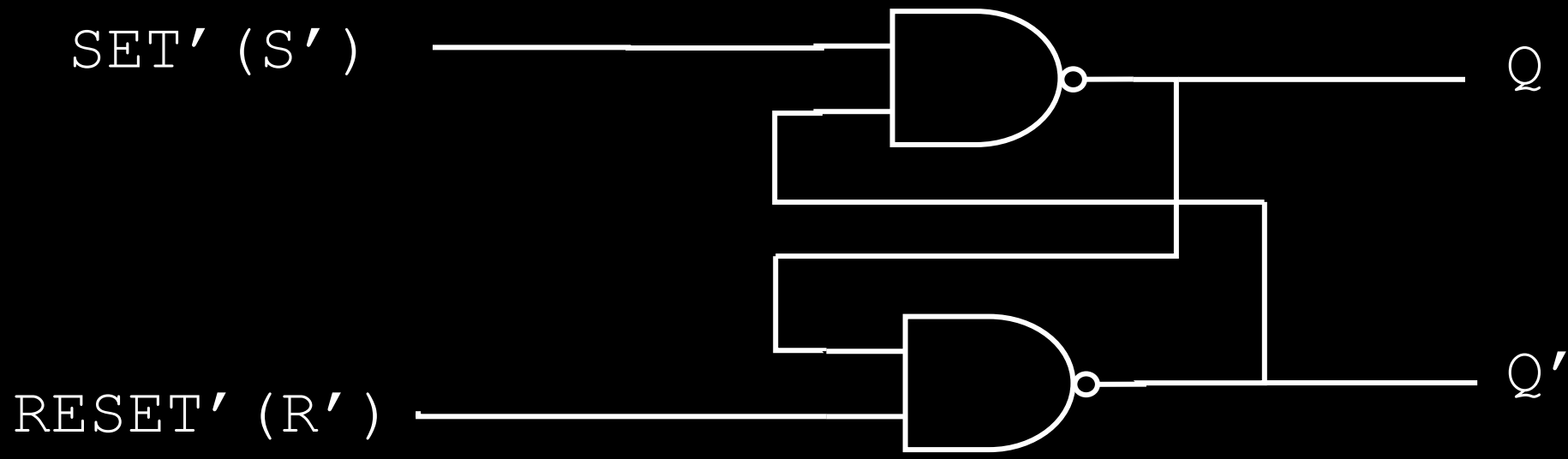
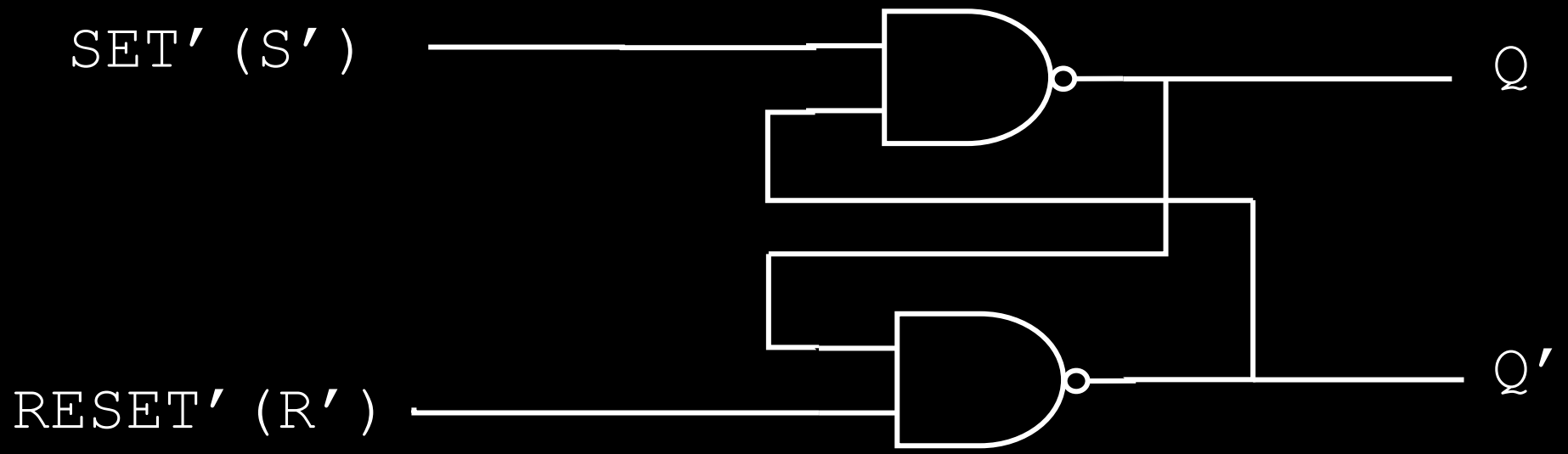
Set'-Reset' Latch

The Set'-Reset' Latch provides an alternate implementation which we'll use for more complex designs.

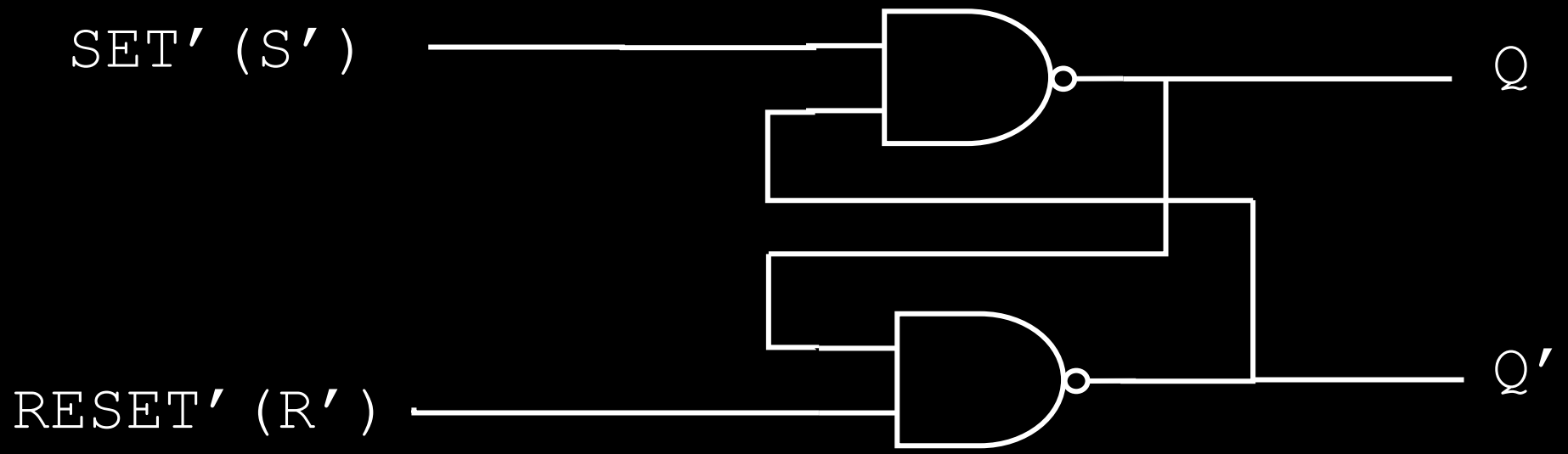


Set'-Reset' Latch



What is the dominant input for the Set'-Reset' Latch?

Set'-Reset' Latch

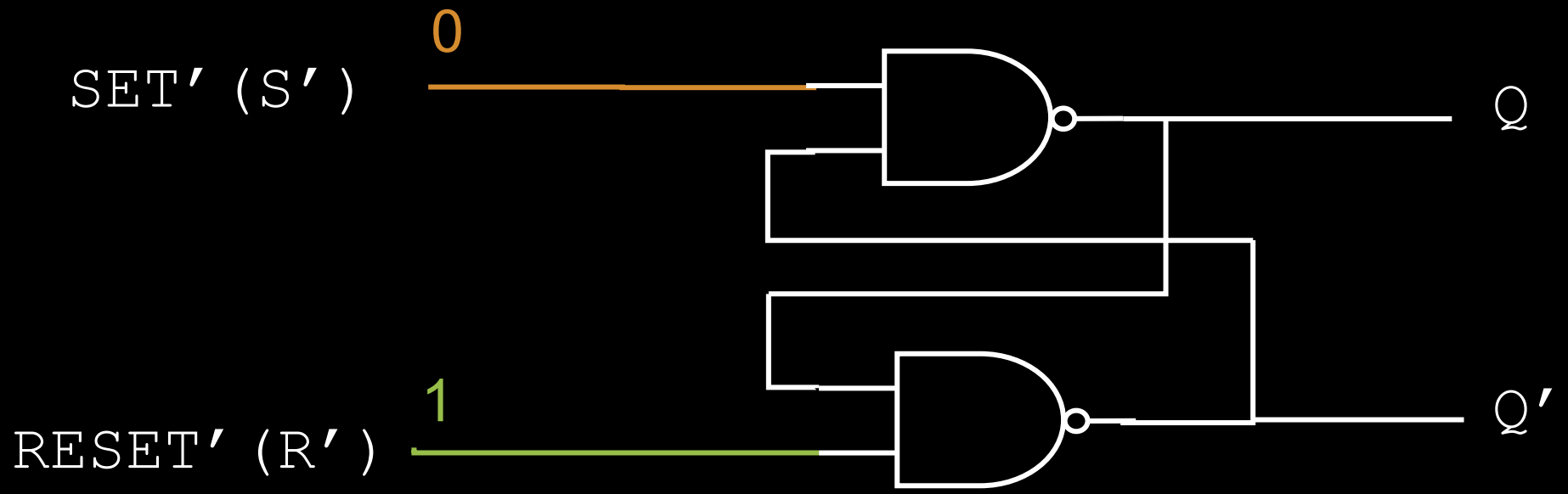


What is the dominant input for the Set'-Reset' Latch?

0 is the dominant input for the NAND-gate

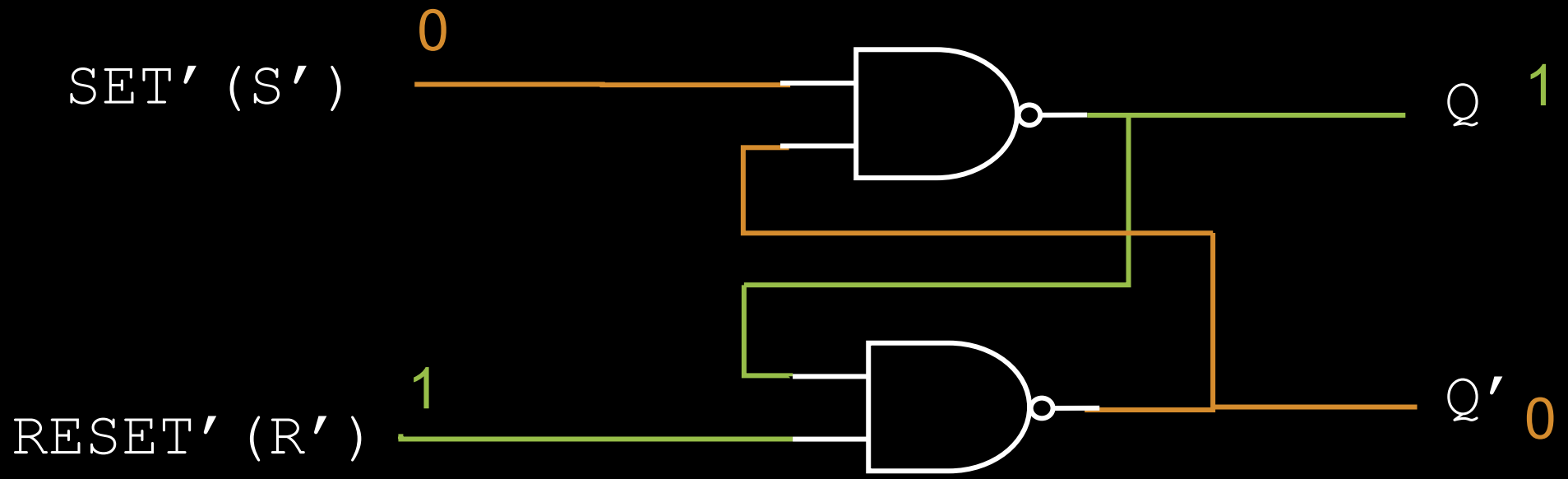
Set'-Reset' Latch

1 | 0



Set'-Reset' Latch

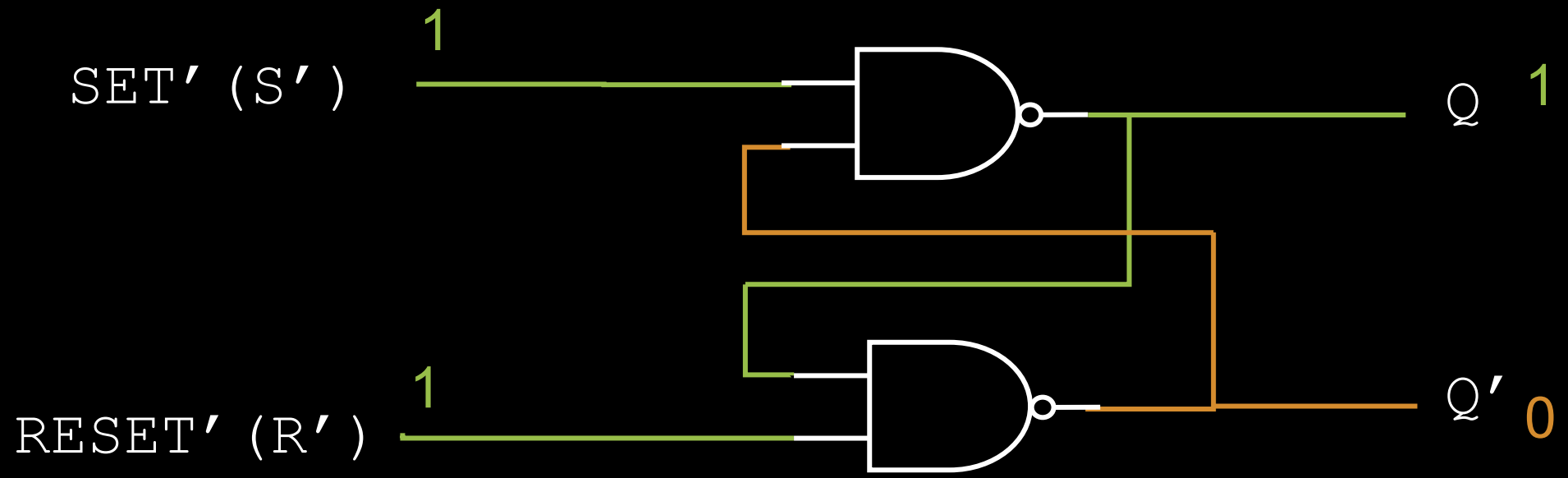
1 | 0



Since 0 is the dominant input, the top NAND-gate will be forced to 1.

Set'-Reset' Latch

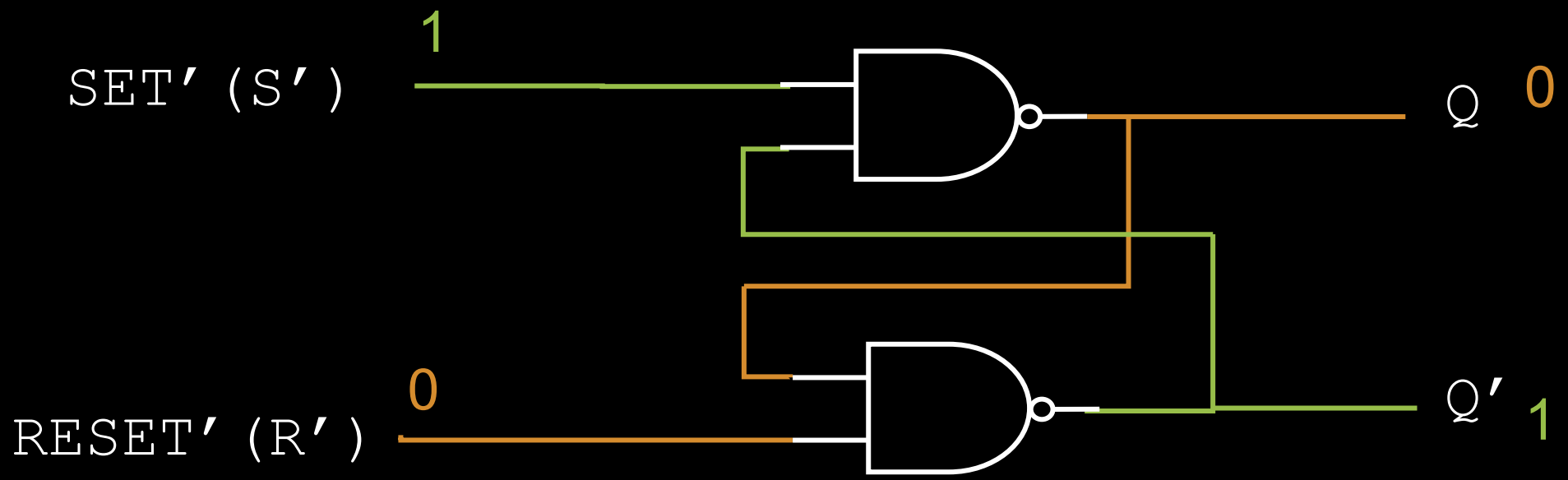
1 | 0



The 0 from Q' will continue to dominate the top NAND-gate.
Our SET state is maintained, even with all 1's on the input.

Set’-Reset’ Latch

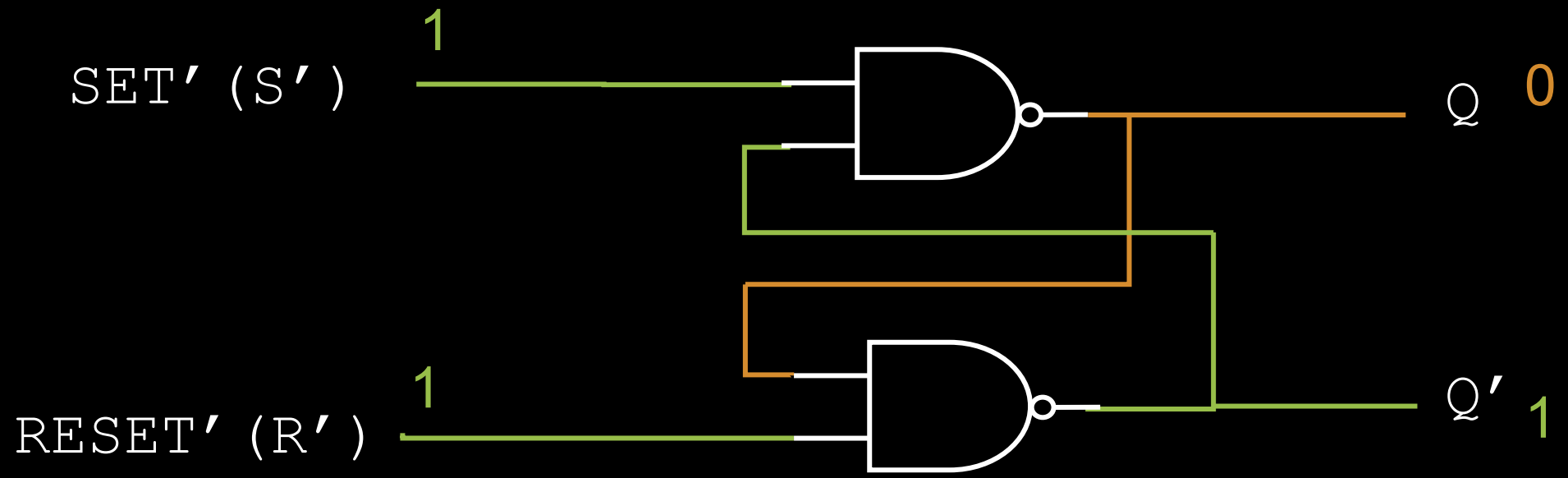
1 | 0



Since 0 is the dominant input, the bottom NAND-gate will be forced to 1.

Set'-Reset' Latch

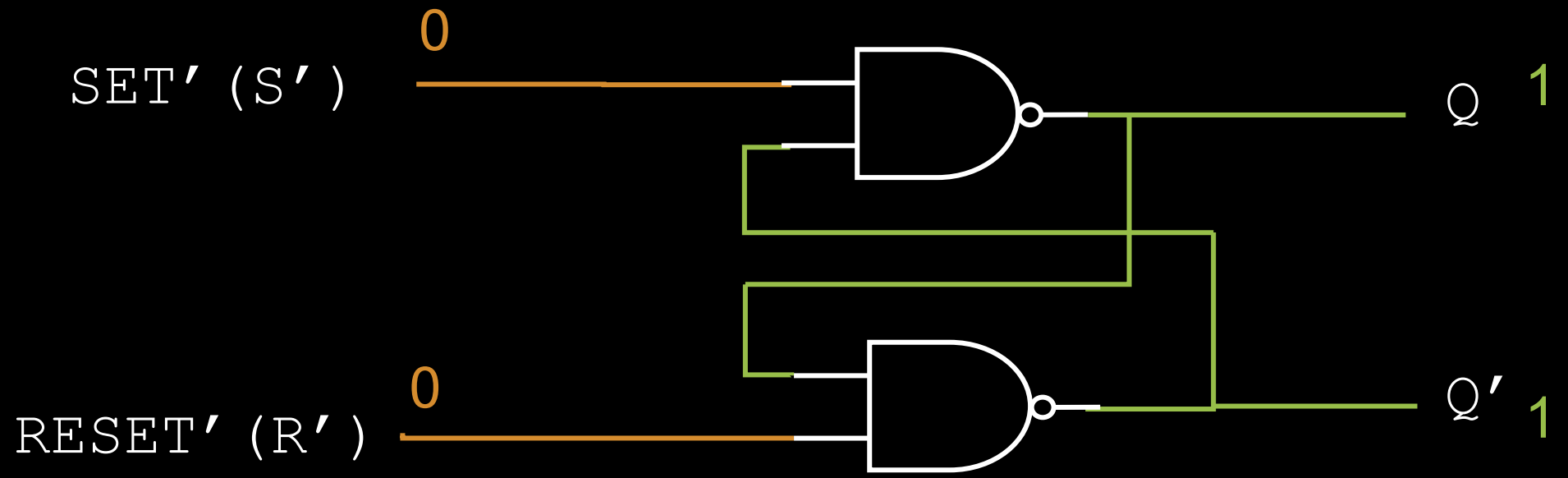
1 | 0



The 0 from Q will continue to dominate the BOTTOM NAND-gate.
Our RESET state is maintained, even with all 1's on the input.

Set'-Reset' Latch

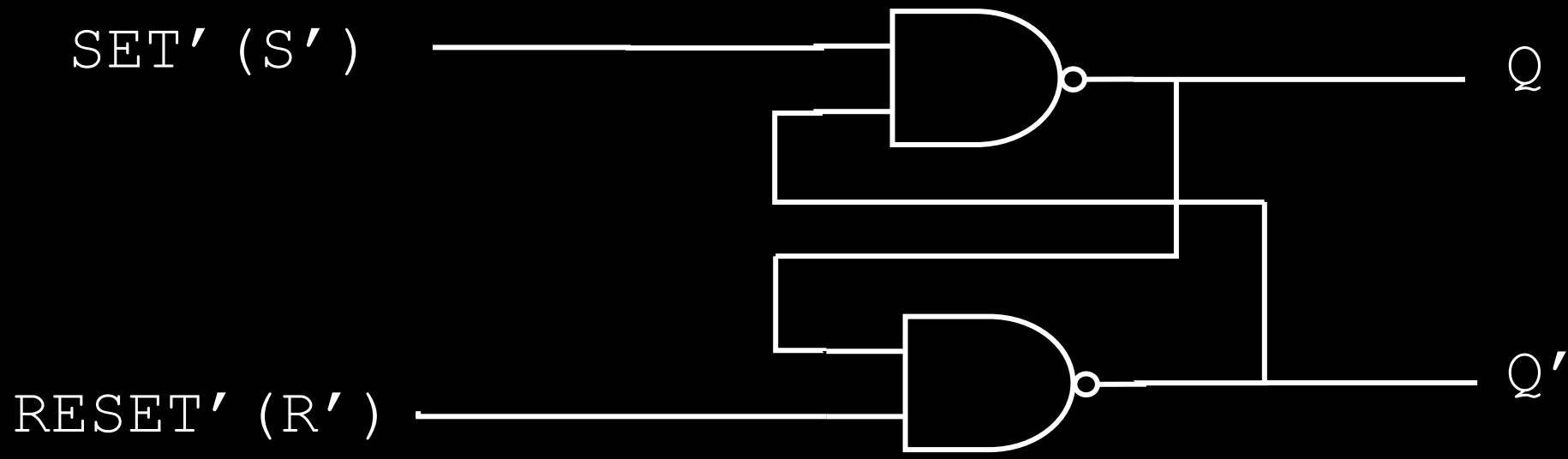
1 | 0



By applying the dominant input to both inputs, both NAND-gates are forced to 1. Since, Q and Q' cannot both be 1, this is an INVALID state.

Set'-Reset' Latch

- Same behavior as the Set-Reset Latch except 0 is the dominant input



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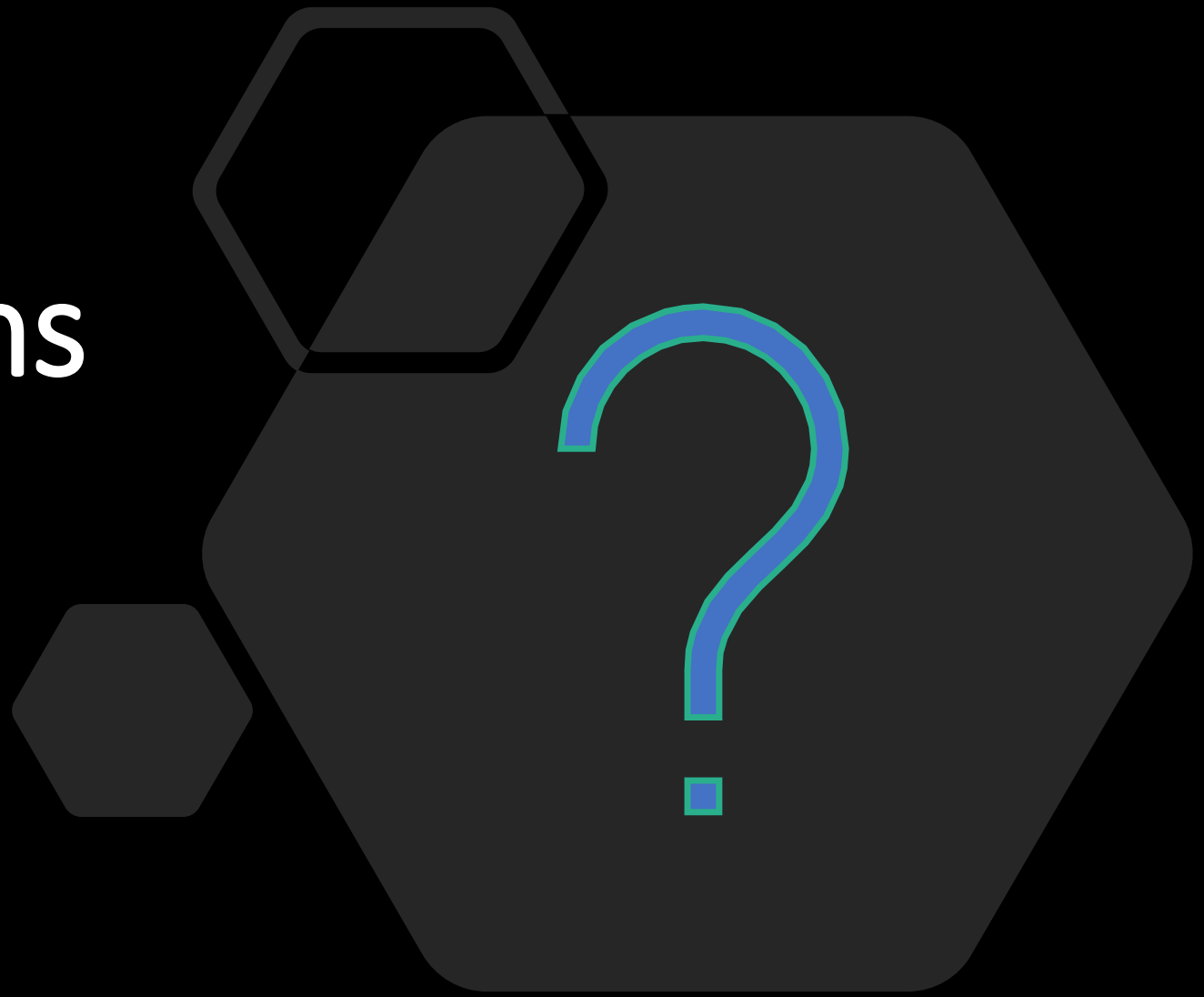

EXAM QUESTION | Set'-Reset' Latch

What will be the state of a Set'-Reset' Latch at the end of the following sequence of inputs?

A. SET
B. RESET
C. INVALID

S	R
1	0
1	1
0	1
1	1
1	1
1	0
1	1

EXAM QUESTION | Set'-Reset' Latch

What will be the state of a Set'-Reset' Latch at the end of the following sequence of inputs?

~~A. SET~~

B. RESET

~~C. INVALID~~

S	R	
1	0	RESET
1	1	RESET
0	1	SET
1	1	SET
1	1	SET
1	0	RESET
1	1	RESET

Gated Set-Reset Latch

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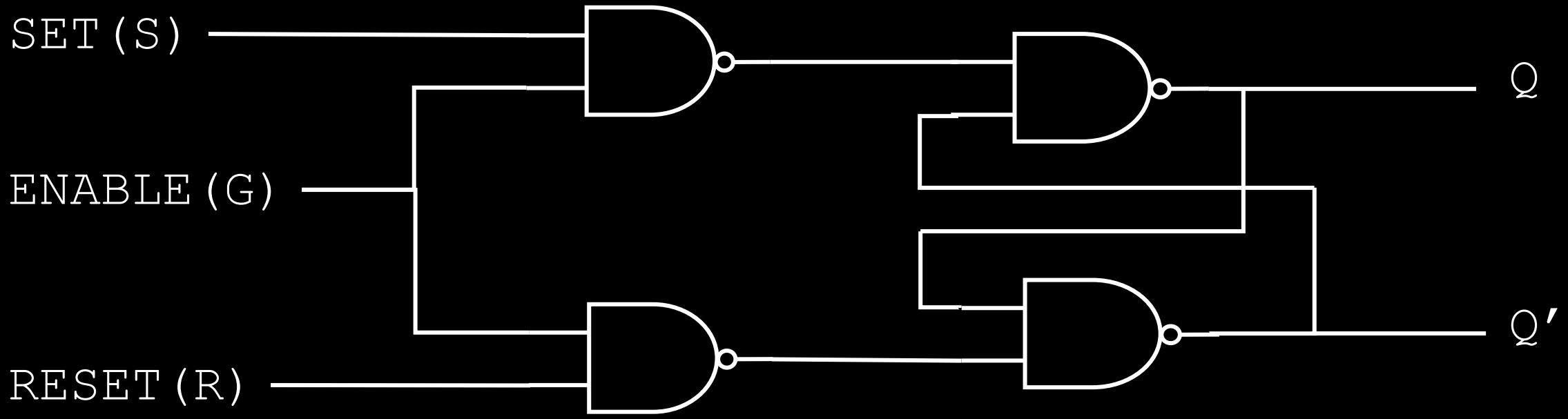
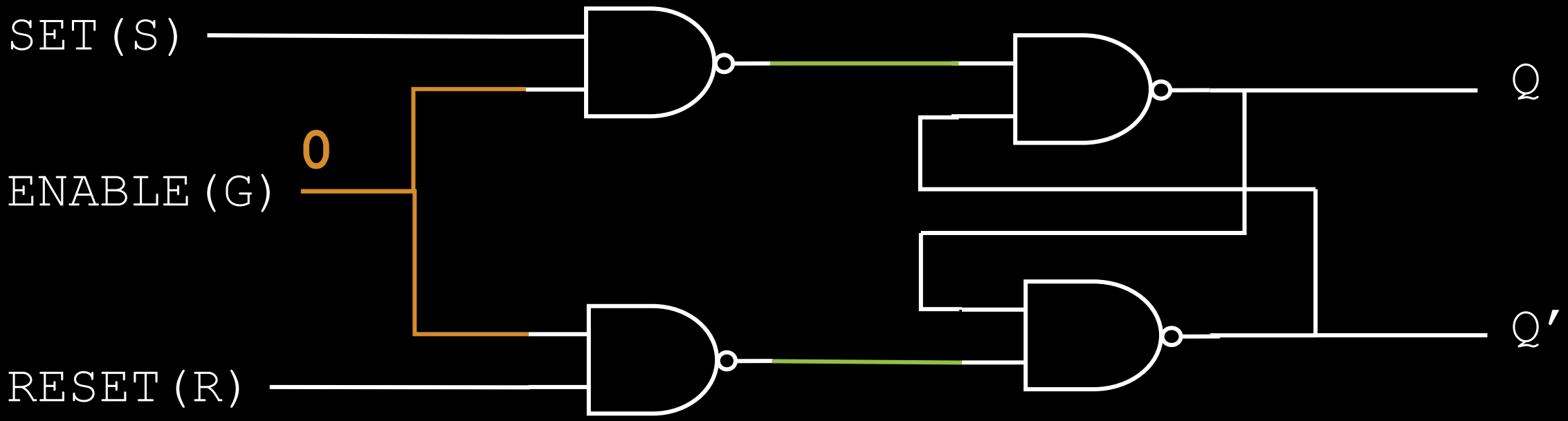
Gated Set-Reset Latch

We can expand out Set-Reset Latch to include a control input to handle when the state can be set or changed.



Gated Set-Reset Latch

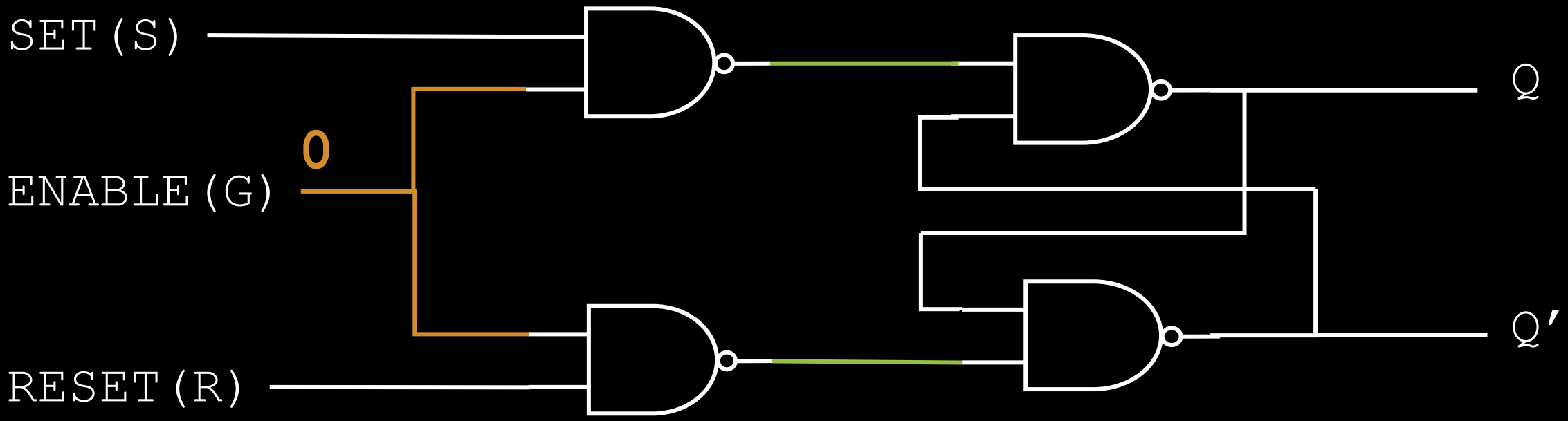
1 | 0



Since 0 is the dominant input, the enable NAND-gates will be forced to 1.

Gated Set-Reset Latch

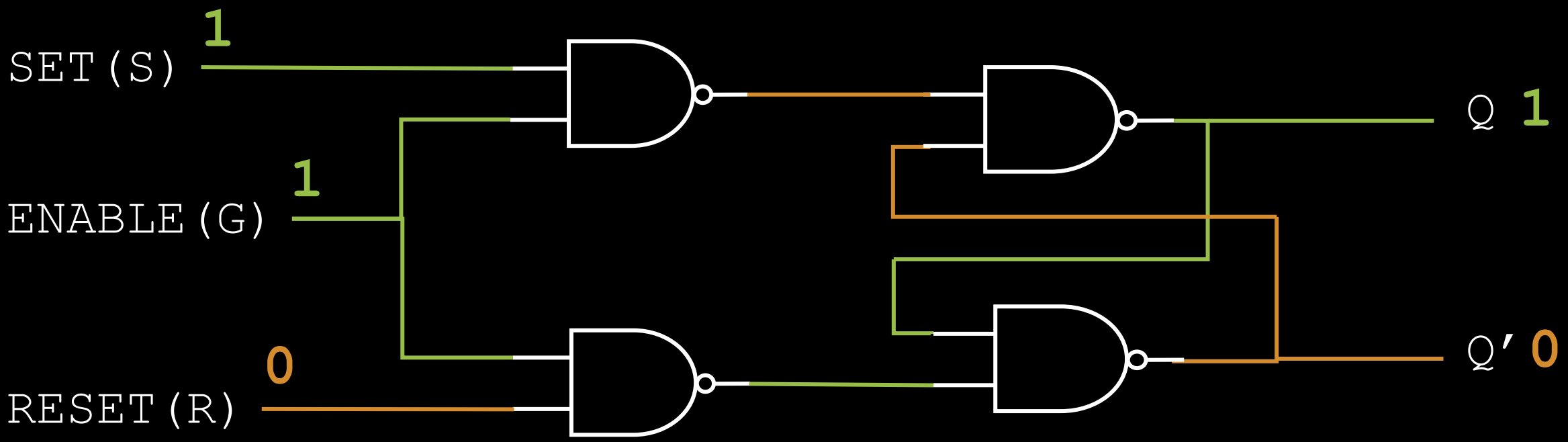
1 | 0



Since 0 is the dominant input, the enable NAND-gates will be forced to 1. This forces the Set'-Reset' Latch to be in the NO-CHANGE state.

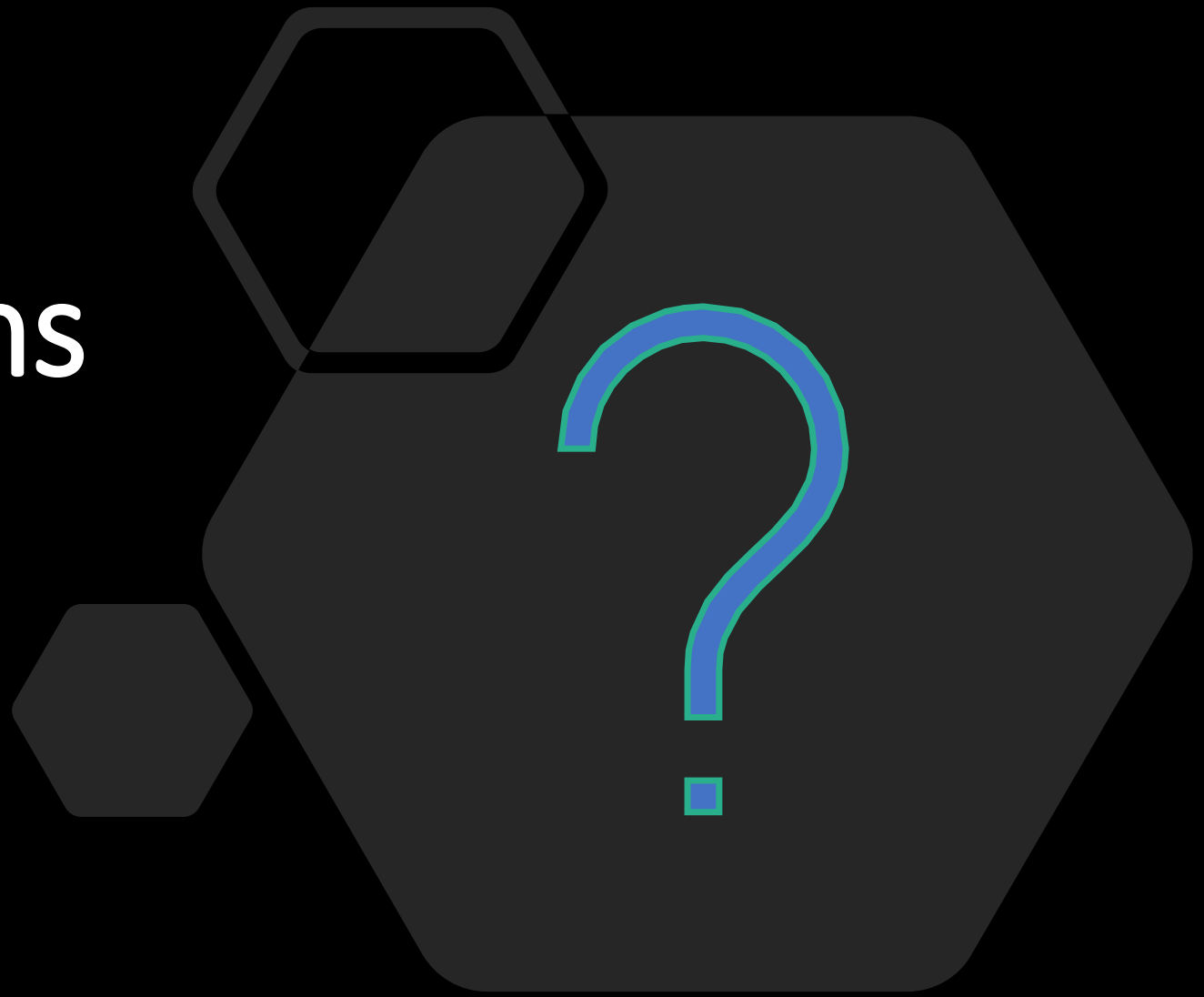
Gated Set-Reset Latch

1 | 0



When the enable signal is 1 (non-dominant), the NAND-gate inverts the SET and RESET signals. Now the latch will behave like a SET-RESET Latch.

What questions do you have?



EXAM QUESTION | Gated Set-Reset Latch

What will the state of a Gated Set-Reset Latch be at the end of the following sequence of inputs?

A. SET
B. RESET
C. INVALID
D. UNDEFINED

G	S	R
0	0	1
1	0	0
1	1	0
1	0	0
0	0	1
1	1	1
0	1	0

EXAM QUESTION | Gated Set-Reset Latch

What will the state of a Gated Set-Reset Latch be at the end of the following sequence of inputs?

~~A. SET~~

~~B. RESET~~

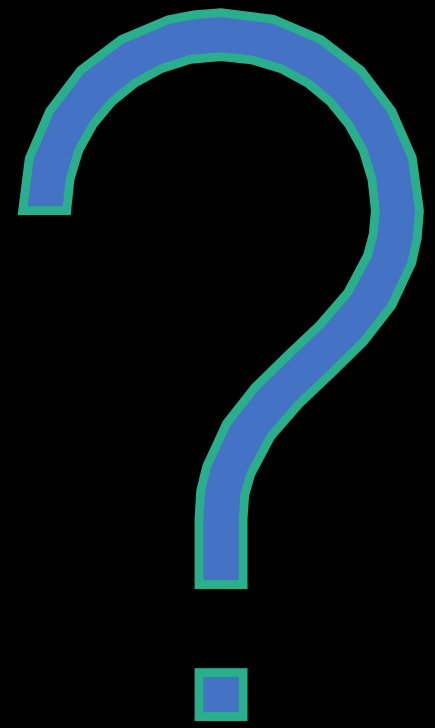
C. INVALID

~~D. UNDEFINED~~

G	S	R	
0	0	1	UNDEFINED
1	0	0	UNDEFINED
1	1	0	SET
1	0	0	SET
0	0	1	SET
1	1	1	INVALID
0	1	0	INVALID

Lecture Recap

1. Combinational vs Sequential Logic
2. Dominant Inputs
3. Set-Reset Latch
4. Set’-Reset’ Latch
5. Gated Set-Reset Latch



What questions do you have?

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