Review Test Submission: Midterm 3

User	Nafiz Imtiaz
Course	Spring 2021 TTU Modern Digital System Design (ECE-2372-D01)
Test	Midterm 3
Started	4/26/21 7:29 PM
Submitted	4/26/21 8:14 PM
Due Date	4/26/21 11:59 PM
Status	Completed
Attempt Score	92 out of 104 points
Time Elapsed	45 minutes out of 50 minutes
Results Displayed	All Answers, Submitted Answers, Correct Answers

Question 1

4 out of 4 points

What will the next state of a register be if C = 0 and L = 1

Selected Answer: C. D

Answers:

A. Undefined

B. Q

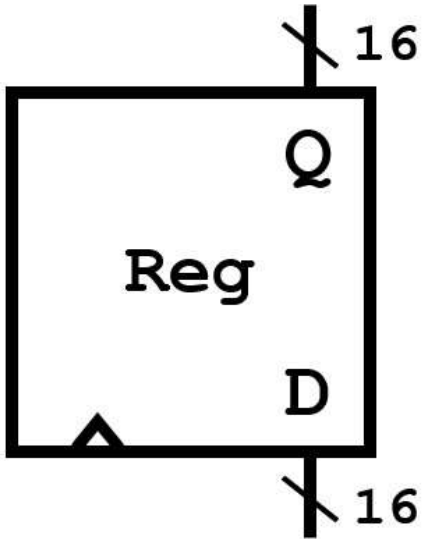
C. D

D. Zeros

Question 2

4 out of 4 points

How many D Flip-Flops are present in the given register?



Selected Answer: A. 16

Answers: A. 16

B. 8

C. 4

D. 32

Question 3

4 out of 4 points

What will the state of a Set'-Reset' Latch be at the end of the following sequence of inputs?

S	R
1	1
1	0
1	1
0	1
0	0
0	0
1	0
0	1
0	0

Selected Answer: B. INVALID

Answers:
A. UNDEFINED
B. INVALID
C. SET
D. RESET

Question 4

4 out of 4 points

For a **Parallel Adder with Accumulator**, what will be the output at the end of the following sequence of inputs?

D	RST
1	1
3	0
2	0
5	0
7	1
4	0
2	0

Selected Answer: C. 6

Answers:
A. 18
B. 24
C. 6
D. 13

Question 5

4 out of 4 points

What will the state of a falling edge-triggered J-K Flip-Flop be at the end of the following sequence of inputs?

CLK	J	K
0	1	0

1	0	0
0	0	1
1	0	0
0	0	0
1	1	1
0	0	0
1	0	1
0	1	1

Selected Answer: A. RESET

Answers: A. RESET

B. SET

C. UNDEFINED

D. INVALID

Question 6

4 out of 4 points

What will the state of a D Latch be at the end of the following sequence of inputs?

G	D
0	0
0	0
1	0
1	1
0	1
0	0
1	0
1	0
0	0

Selected Answer: B. RESET

Answers: A. INVALID

B. RESET

C. UNDEFINED

D. SET

Question 7

4 out of 4 points

A 4-bit PIPO right shift register is initially loaded with the state Q = 4'd13. What will the the output Q be at the end of the following sequence of inputs?

SI	SHIFT	LOAD	D
0	1	0	4'd7
0	1	1	4'd4
1	0	1	4'd10
1	1	0	4'd5
1	0	0	4'd8
1	1	0	4'd9

Selected Answer: D. 4'b1110

Answers:

A. 4'b1010

B. 4'b1101

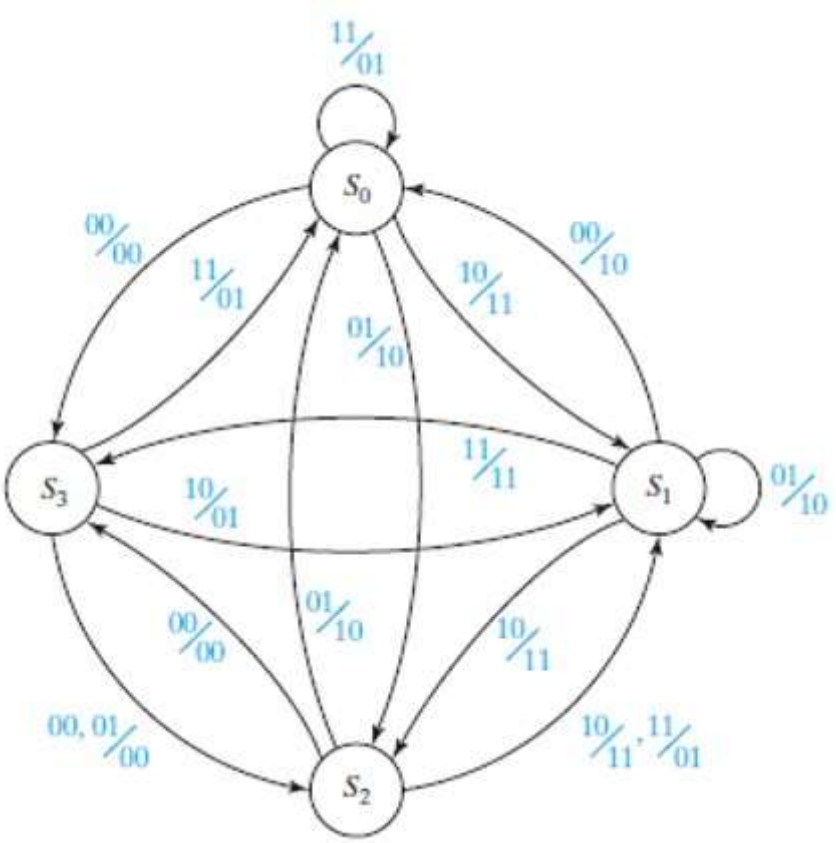
C. 4'b0111

D. 4'b1110

Question 8

4 out of 4 points

For the given state graph, what will the next-state and output be if the present state is S3 and the input is 11?



Selected Answer: B. S0, 01

Answers:
A. S0, 00
B. S0, 01
C. S2, 00
D. S1, 01

Question 9

4 out of 4 points

What is the Next-State equation for flip-flop B in a 2-bit arbitrary sequence binary counter, with enable, with the given sequence?

Q_A^+	Q_B^+
1	0
0	0
1	1
0	1

Selected Answer: B. E'B + AB + EA'B

Answers:
A. EA' + EB + A'B'

B. E'B + AB + EA'B

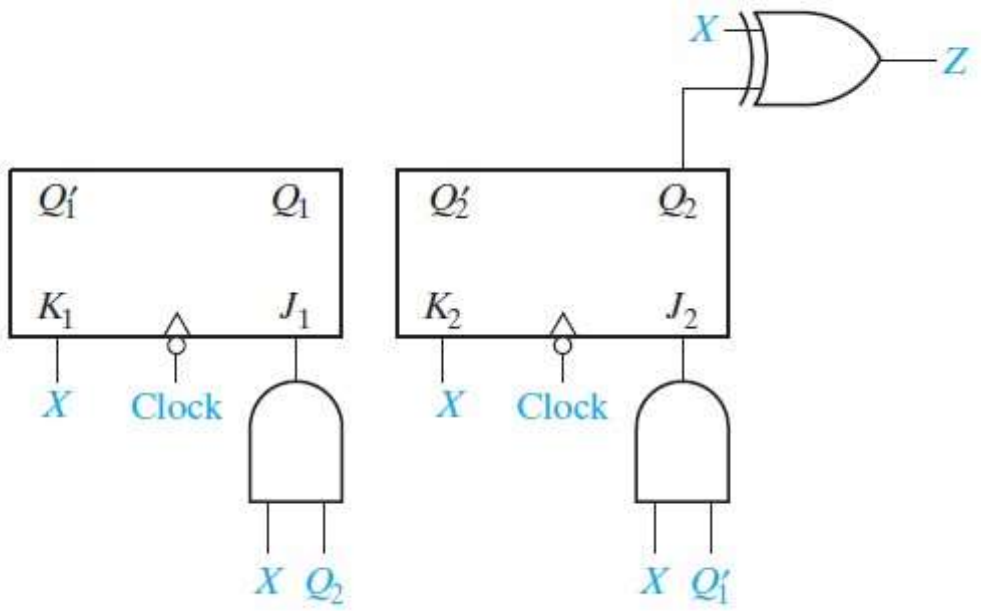
C. E'AB + A'B' + E'B'

D. E'A'B + EAB + EA'

Question 10

0 out of 4 points

What type of sequential circuit is shown?



Selected Answer: A. Moore

Answers:

A. Moore

B. Boolean

C. Mealy

D. Flip-Flop

Question 11

4 out of 4 points

What will the state of a rising edge-triggered S-R Flip-Flop be at the end of the following sequence of inputs?

CLK	S	R
0	1	0
1	0	0
0	0	0

1	0	1
0	0	1
1	1	1
0	0	0
1	1	0
0	1	0

Selected Answer: B. RESET

Answers:
A. INVALID
B. RESET
C. UNDEFINED
D. SET

Question 12

4 out of 4 points

What is the dominant input signal for the AND-gate?

Selected Answer: B. 0

Answers:
A. X
B. 0
C. 1
D. Z

Question 13

4 out of 4 points

What will be the state of a Set-Reset Latch at the end of the following sequence of inputs?

S	**R**
1	0
0	0
1	0
0	1
0	0
1	0
0	0

Selected Answer: D. SET

Answers:

A. RESET

B. INVALID

C. UNDEFINED

D. SET

Question 14

4 out of 4 points

What will the state of a Gated Set-Reset Latch be at the end of the following sequence of inputs?

G	S	R
0	0	0
0	1	0
1	0	1
1	0	0
0	1	0
1	1	1
1	1	0
0	0	0
0	0	1

Selected Answer: D. SET

Answers:

A. UNDEFINED

B. RESET

C. INVALID

D. SET

Question 15

4 out of 4 points

Assuming that the flip-flop is initially in the RESET state, what will be the state of a falling edge-triggered T Flip Flop be at the end of the following sequence of inputs?

CLK	T

0	0
1	0
0	1
1	1
0	1
1	0
0	0
1	1
0	0

Selected Answer: B. RESET

Answers:
A. INVALID
B. RESET
C. SET
D. UNDEFINED

Question 16

4 out of 4 points

For the given state table, what will the next-state and output be if the present-state is S2 and the input X1X2 = 10?

Present State	Next State $X_1X_2 = 00$	01	10	11	Present Output (Z_1Z_2) $X_1X_2 =$ 00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

Selected Answer: D. S1, 11

Answers:
A. S3, 11
B. S0, 10
C. S1, 01
D. S1, 11

Question 17

4 out of 4 points

If a Mealy circuit has a 3-bit input, 10 states, and a 2-bit output, then it will be defined by how many equations of how many variables?

Selected Answer: B. 6 equations of 7 variables

Answers:
A. 4 equations of 7 variables
B. 6 equations of 7 variables
C. 7 equations of 4 variables
D. 2 equations of 3 variables

Question 18

4 out of 4 points

A 3-bit synchronous binary counter is initially loaded with 3'd6. What will the state of the counter be at the end of the following sequence of inputs?

COUNT	RESET
1	1
1	0
0	0
1	0
1	0
1	0

Selected Answer: B. 3'b100

Answers:
A. 3.b011
B. 3'b100
C. 3'b111
D. 3'b101

Question 19

4 out of 4 points

For the given transition table, what is the Next State Equation for Flip-Flop B?

Present State (AB)	Next State (A^+B^+)		Output (F)	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

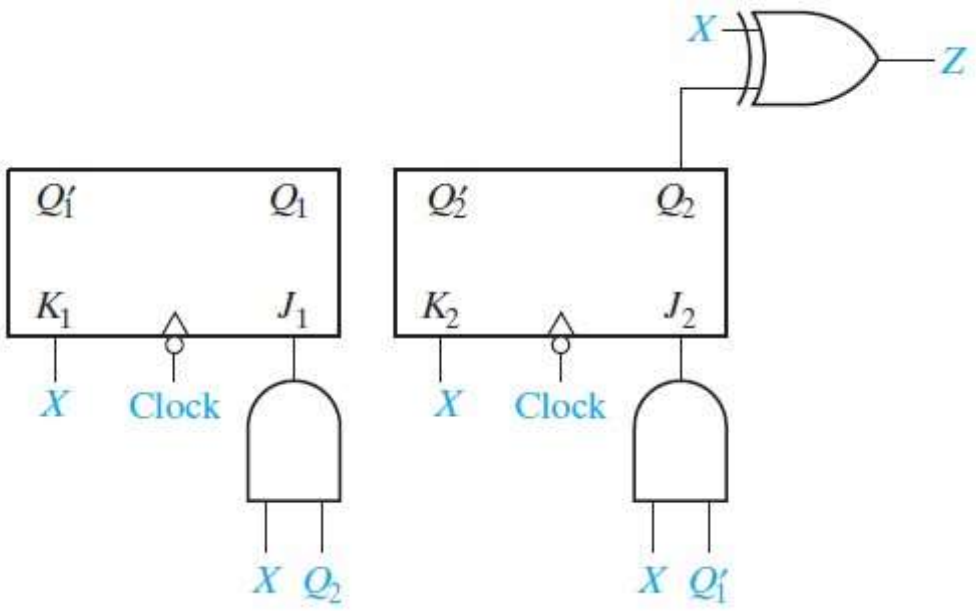
Selected Answer: C. X'B + A'B + XB'

Answers:
A. X'B + XA'B + AB'
B. XA'B' + AB' + XB'
C. X'B + A'B + XB'
D. X'A' + X'B + AB'

Question 20

4 out of 4 points

For the given sequential circuit, What will the output sequence be for the input sequence X = {0, 1, 1, 0, 1}



Selected Answer: B. Z = {0, 1, 0, 0, 1}

Answers:
A. Z = {0, 1, 0, 0, 0}

B. Z = {0, 1, 0, 0, 1}

C. Z = {0, 1, 1, 0, 1}

D. Z = {0, 1, 0, 1, 0}

Question 21

4 out of 4 points

For the given register circuit, how will the command **LOAD Y B**; effect the control inputs **S** and **ADDR**?

Selected Answer: D. S = 1, ADDR = 0

Answers:

A. S = 0, ADDR = 0

B. S = 1, ADDR = 1

C. S = 0, ADDR = 1

D. S = 1, ADDR = 0

Question 22

4 out of 4 points

If a Moore circuit has a 3-bit input, 17 states, and a 2-bit output. How many output equations of how many variables will be needed?

Selected Answer: D. 2 equations of 5 variables

Answers:

A. 2 equations of 4 variables

B. 7 equations of 8 variables

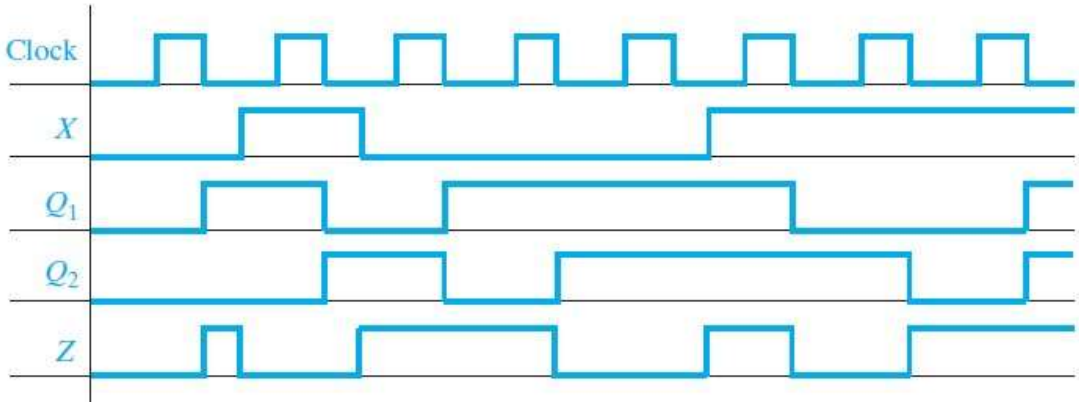
C. 4 equations of 5 variables

D. 2 equations of 5 variables

Question 23

4 out of 4 points

What is the sequence X that is shown in the following timing chart?



Selected Answer: B. X = {0, 1, 0, 0, 0, 1, 1, 1}

Answers:
A. X = {0, 0, 1, 0, 1, 1, 1, 0}
B. X = {0, 1, 0, 0, 0, 1, 1, 1}
C. X = {0, 1, 0, 1, 1, 1, 0, 0}
D. X = {0, 0, 1, 1, 0, 1, 0, 1}

Question 24

0 out of 4 points

Which of the following RTL commands defines a 5-bit internal register?

Selected Answer: A. output reg [4:0] myReg;

Answers:
A. output reg [4:0] myReg;
B. reg [4:0] myReg;
C. output reg [5:0] myReg;
D. output [4:0] myReg;

Question 25

4 out of 4 points

What will the state of a falling edge-triggered D Flip-Flop be after the following sequence of inputs?

CLK	D
0	0
1	1
0	1
0	1
1	0
0	1
1	0
1	0
0	1

Selected Answer: C. RESET

Answers:
A. UNDEFINED
B. SET
C. RESET
D. INVALID

Question 26

0 out of 4 points

Which of the following RTL commands will cause the logic instructions to trigger on both the rising and falling edges of B?

Selected Answer: always@(CLK)

Answers: always@(B)

always@(CLK)

always@(posedge & negedge B)

always@(posedge CLK | negedge CLK)

Thursday, April 29, 2021 4:05:57 PM CDT

← OK