Pipelined Microcontroller Processor

High-Level Architectural Specifications

Properties

The microcontroller has:

- Four 8-bit general purpose registers (GPR)
- One 8-bit immediate value register, source only (IMM)
- Latency of 3 cycles + number of stalls
- 12-bit fixed length instruction set

Instruction Set

I/O instructions:

Op	**Src1**	**Src2**	**Dst**	**Description**
LD	IMM	DC	GPR	Loads the Immediate value into a register.
OUT	GPR	DC	DC	Sends a register value to the output bus.

Arithmetic instructions:

Op	**Src1**	**Src2**	**Dst**	**Description**
ADD	GPR/IMM	GPR/IMM	GPR	Produces an 8-bit modular addition.
SUB	GPR/IMM	GPR/IMM	GPR	Produces an 8-bit modular subtraction.

Logic instructions:

Op	**Src1**	**Src2**	**Dst**	**Description**
NAND	GPR/IMM	GPR/IMM	GPR	Produces an 8-bit vector NAND.
NOR	GPR/IMM	GPR/IMM	GPR	Produces an 8-bit vector NOR.
XOR	GPR/IMM	GPR/IMM	GPR	Produces an 8-bit vector XOR.
SHFL	GPR/IMM	GPR/IMM	GPR	Bit-shifts src1 by the index of the least significant ‘1’ in src2. The index of LSB in src2 is 1.

Instruction format

Instruction	Encoding
LD	000
OUT	001
ADD	010
SUB	011
NAND	100
NOR	101
XOR	110
SHFL	111

Register	Encoding
R0	000
R1	001
R2	010
R3	011
IMM	100

Interface list

Input signals:

Name	Description
clk	System Clock used to synchronize all pipestage activity.
reset	System reset signal clears all necessary state in the processor.
instv	This bit indicates that the instruction is valid.
opcode[2:0]	The encoded instruction to be executed.
src1[2:0]	The encoded source1 register of the instruction
src2[2:0]	This vector is the encoded source2 register of the instruction.
dst[2:0]	The encoded destination register of the instruction.
imm[7:0]	This vector is the immediate data available to the current instruction.

Output signals:

Name	Description
`stalled`	This signal indicates that the processor is stalled and can not receive a new instruction the next cycle.
`dataout[7:0]`	The output data bus on which internal processor data is driven during execution of the OUT instruction.
`dataoutv`	This bit indicates that the output data on `dataout` is valid. The `dataout` vector value is not defined when this valid bit is not set.

Comments:

- Instruction dependency is dealt by stalling for 3 clock cycles after any instruction that writes to the RF.
- An invalid instruction doesn't have an effect upon the processor state.
- The reset signal invalidates the instructions inside the processor. It does not clear the processor GPRs.
- The reset signal is synchronized, meaning it's value should be sampled on clock posedge.
- Design is implemented as flop-based-design.
- There are no internal flops on input signals to the processor. Internal flops are present on the processor's outputs.