## Title: Design and Implementation of Digital Circuits in Microwind
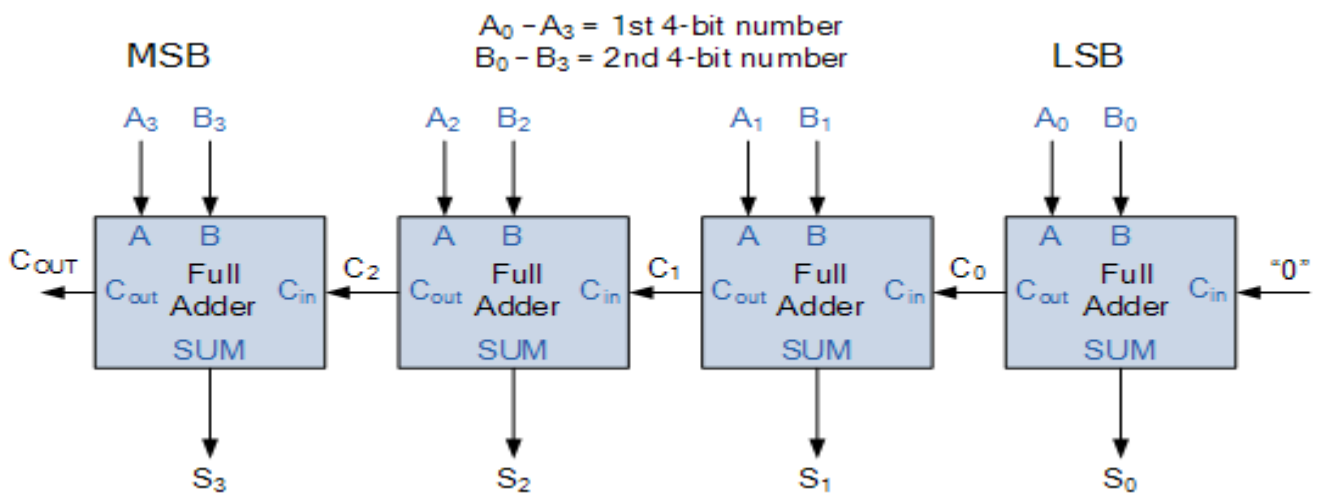
### 1. 4-Bit Full Adder

**Circuit Diagrams:**



Truth Tables: -

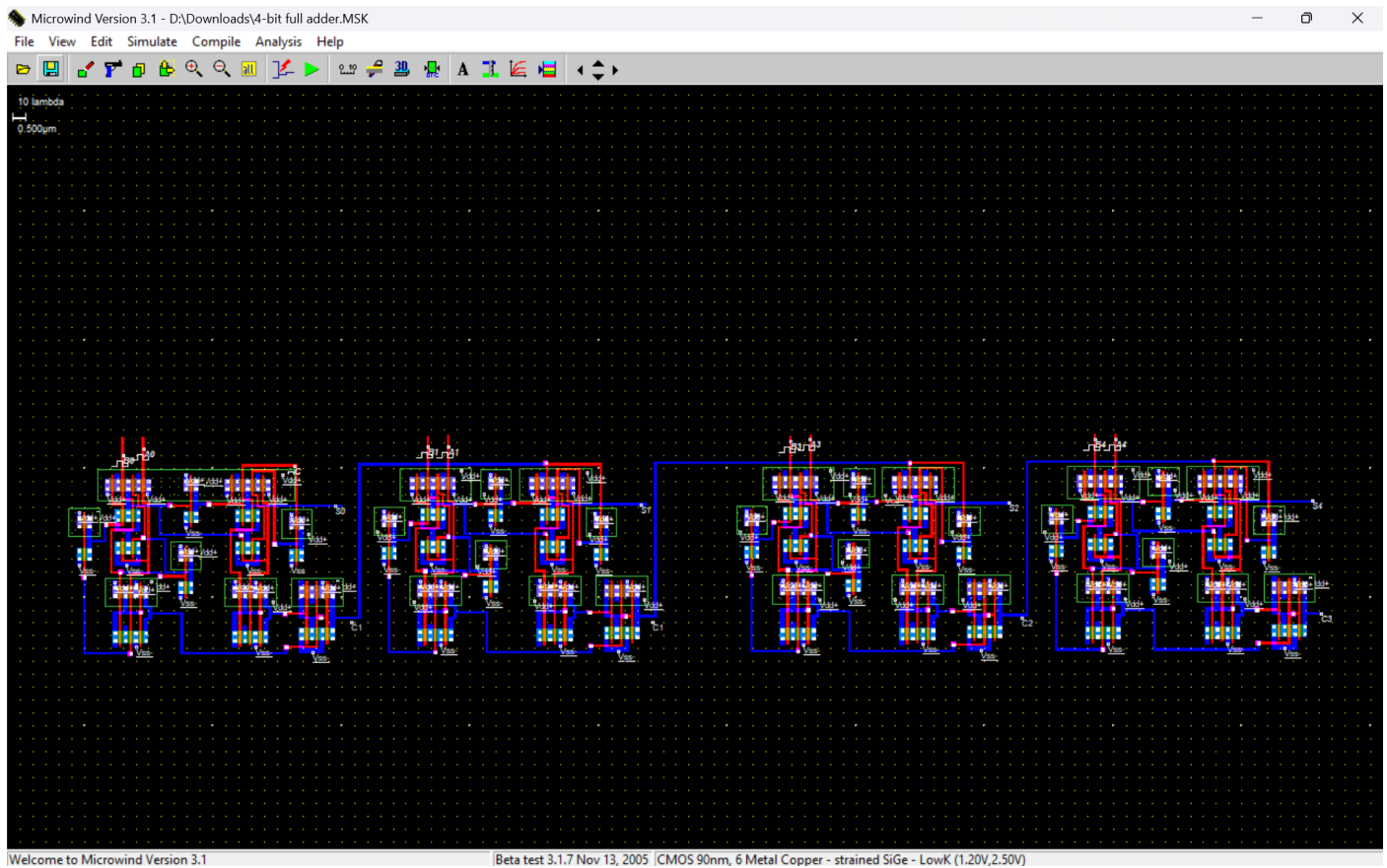| A | B | Cin | Sum | C |
|---|---|-----|-----|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Logic Equations: -

The sum (S) of the full-adder is the XOR of A, B, and Cin. Therefore,

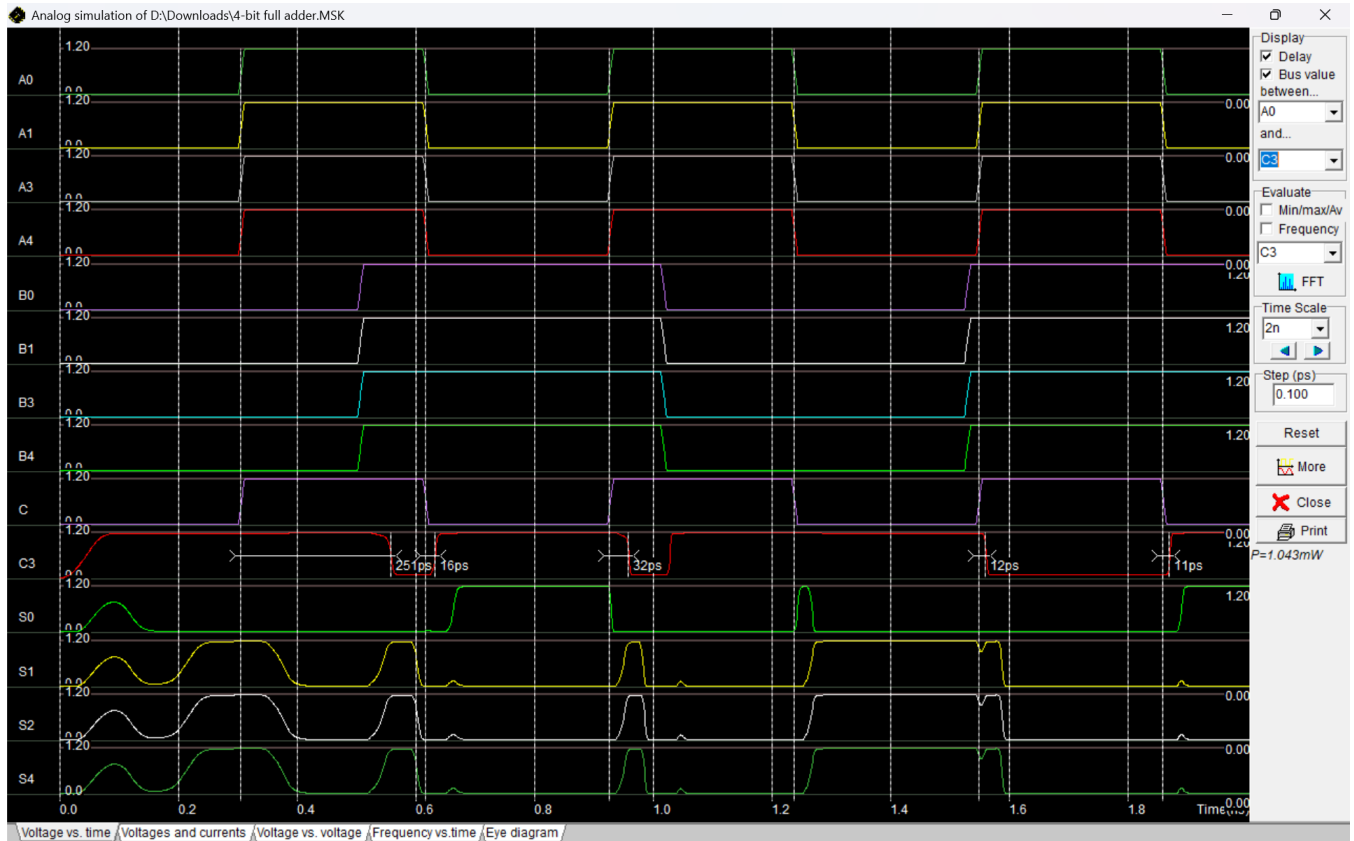$$\text{Sum, S} = A \oplus B \oplus C_{in} = A'B'C_{in} + A'BC'_{in} + AB'C'_{in} + ABC_{in}$$

The carry (C) of the half-adder is the AND of A and B. Therefore,
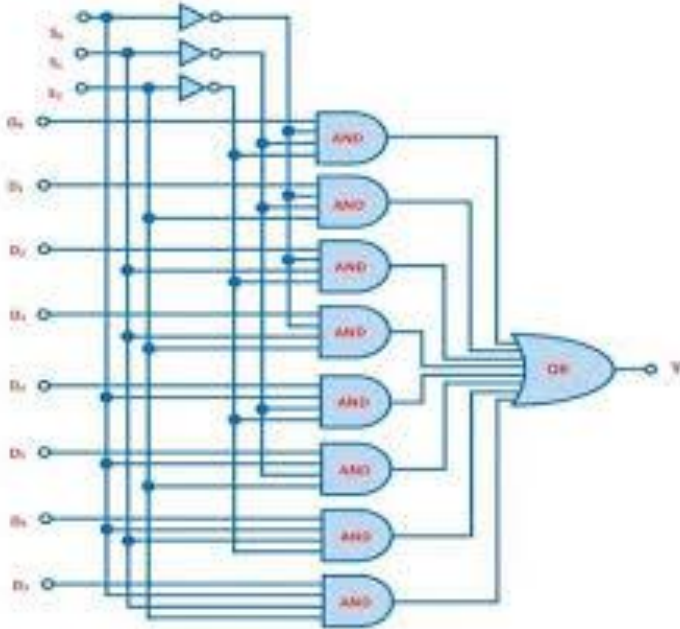
$$\text{Carry, C} = AB + AC_{in} + BC_{in}$$

Microwind Layout: -

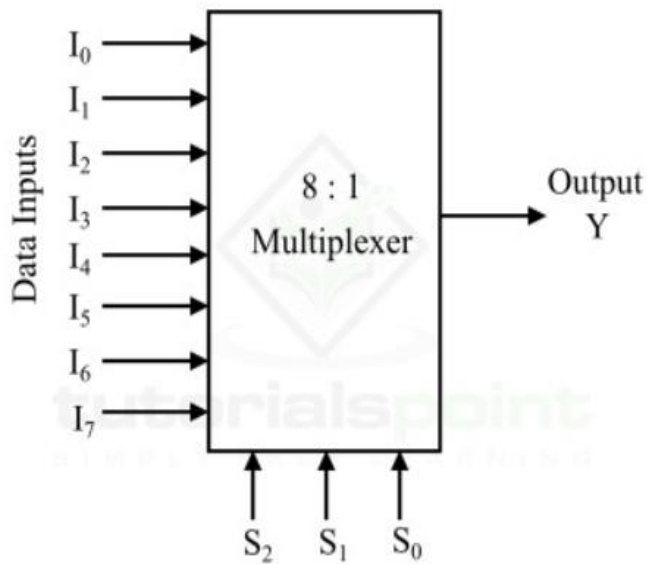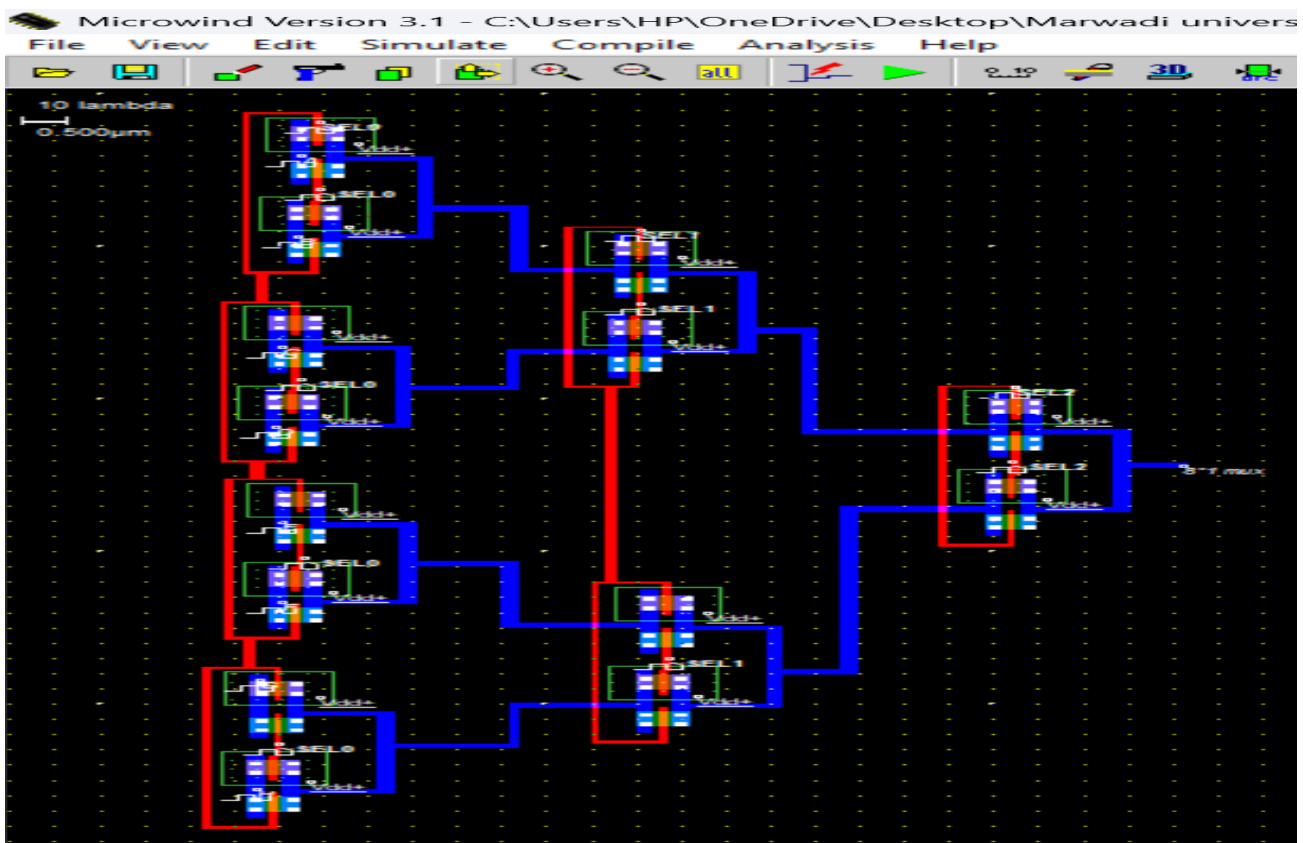## 2. 8×1 MultiplexerCircuit Diagrams: -



Block Diagram: -



Figure 4 - 8:1 Multiplexer

| Selection Inputs | | | Output |
| --- | --- | --- | --- |
| $S_2$ | $S_1$ | $S_0$ | Y |
| 0 | 0 | 0 | $I_0$ |
| 0 | 0 | 1 | $I_1$ |
| 0 | 1 | 0 | $I_2$ |
| 0 | 1 | 1 | $I_3$ |
| 1 | 0 | 0 | $I_4$ |
| 1 | 0 | 1 | $I_5$ |
| 1 | 1 | 0 | $I_6$ |
| 1 | 1 | 1 | $I_7$ |

Logic Equations: -

**Y= S2S1S0I0+S2S1S0I1+S2S1S0I2+S2S1S0I3+S2S1S0I4+S2S1S0I5+S2S1S0I6+S2S1S0I7**

Microwind Layouts: -

Output:



Analog simulation of C:\Users\HP\OneDrive\Desktop\Marwadi university\SEM\5-SEM\VD\long hour codding\81MULTIPLEXER.MSK
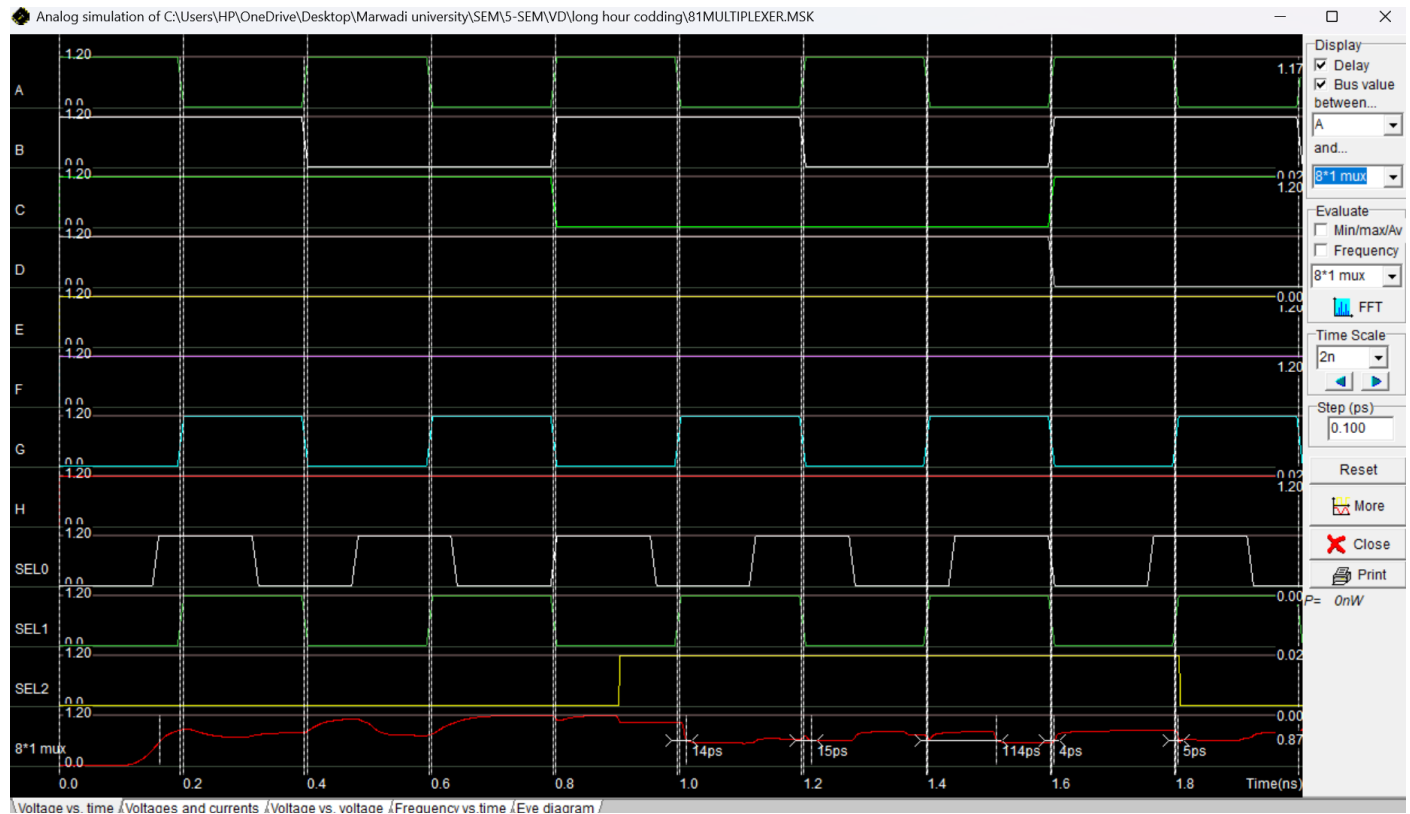
## 3. 1-bit Magnitude Comparator

Circuit Diagrams:



Page no.
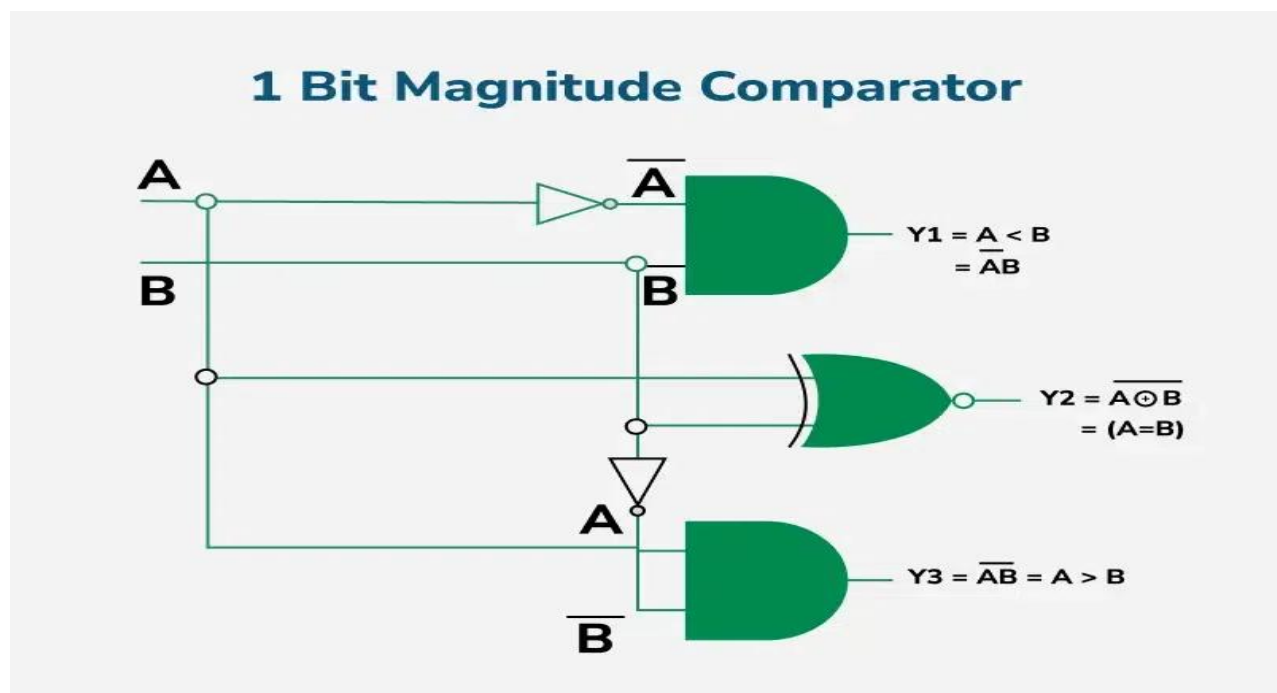
Truth Tables: -

| A | B | A<B | A=B | A>B |
|---|---|-----|-----|-----|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |

Logic Equations: -

( A<B)+(A>B) = A'B+AB'
Taking complement both sides

( (A<B) + (A>B) )' = ( A'B + AB')'

( (A<B) + (A>B) )' = (A'B)' ( AB')'

( (A<B) + (A>B) )' = ( A + B') (A' +B )
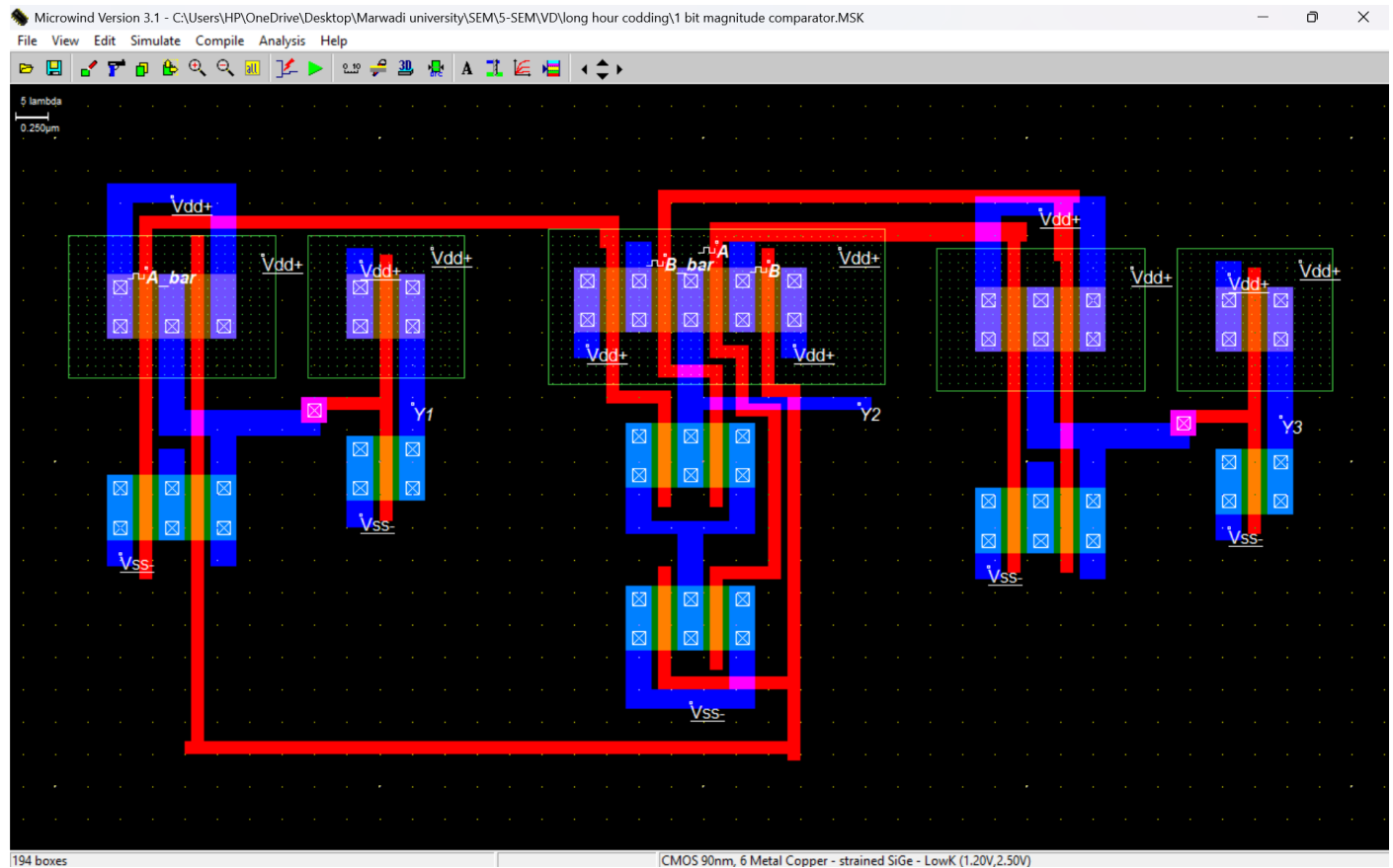
( (A<B) + (A>B) )' =( AA' + AB + A'B' +BB')

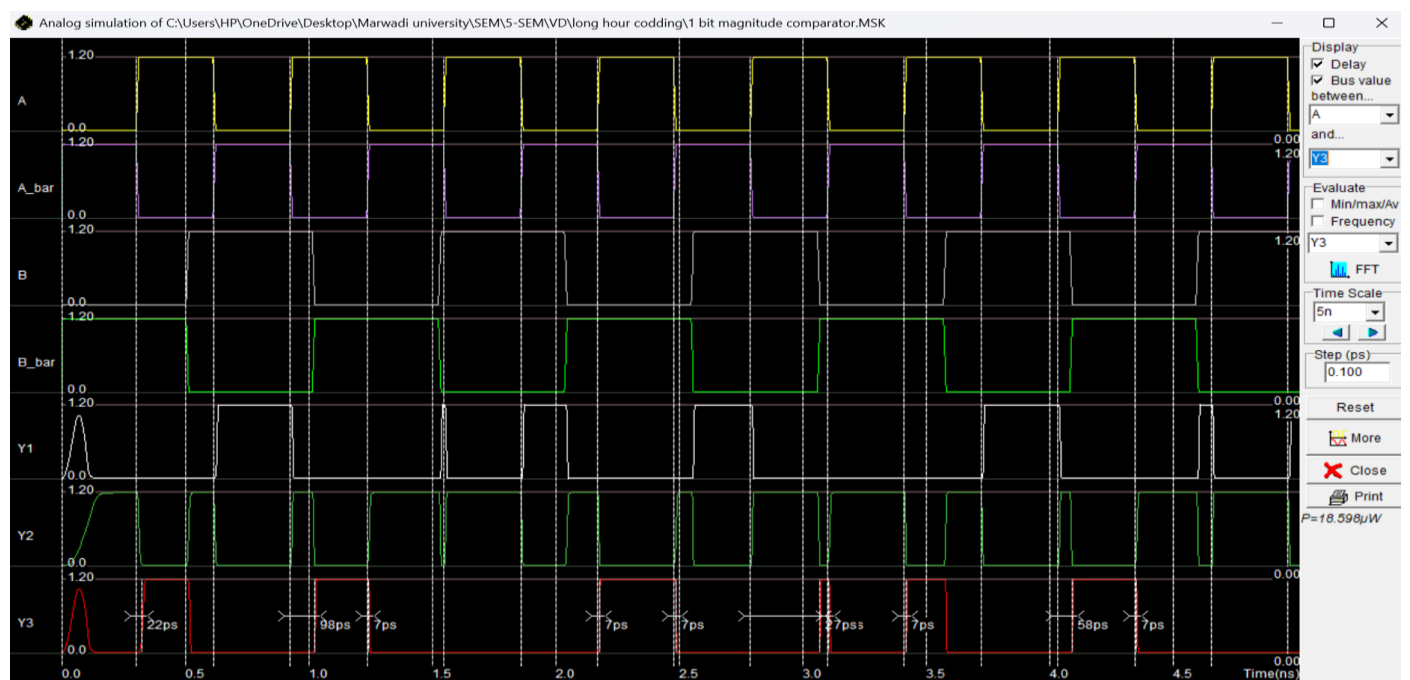     "            "        = ( AB + A'B' )

Thus,
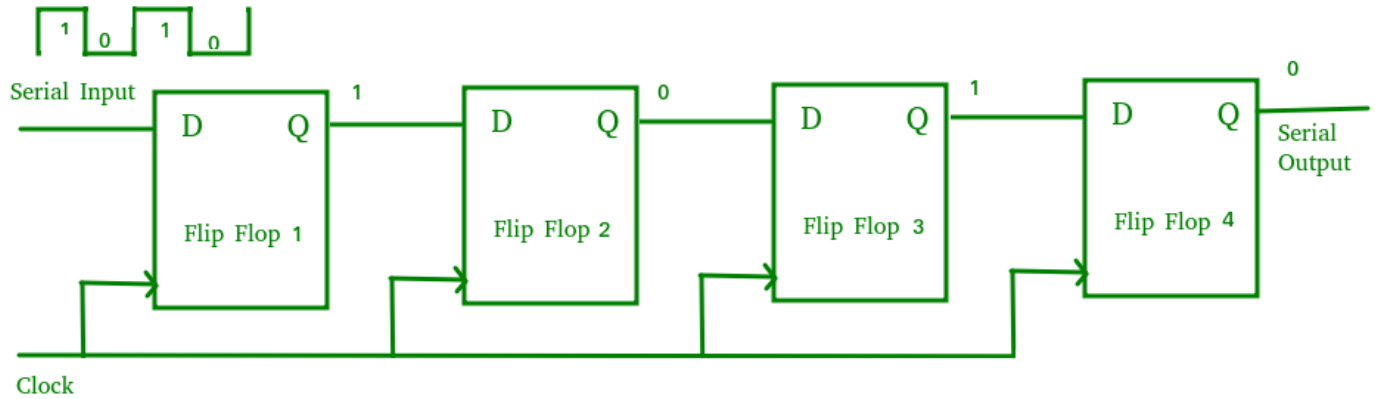
( (A<B) + (A > B) )' = (A = B)

Microwind Layouts: -



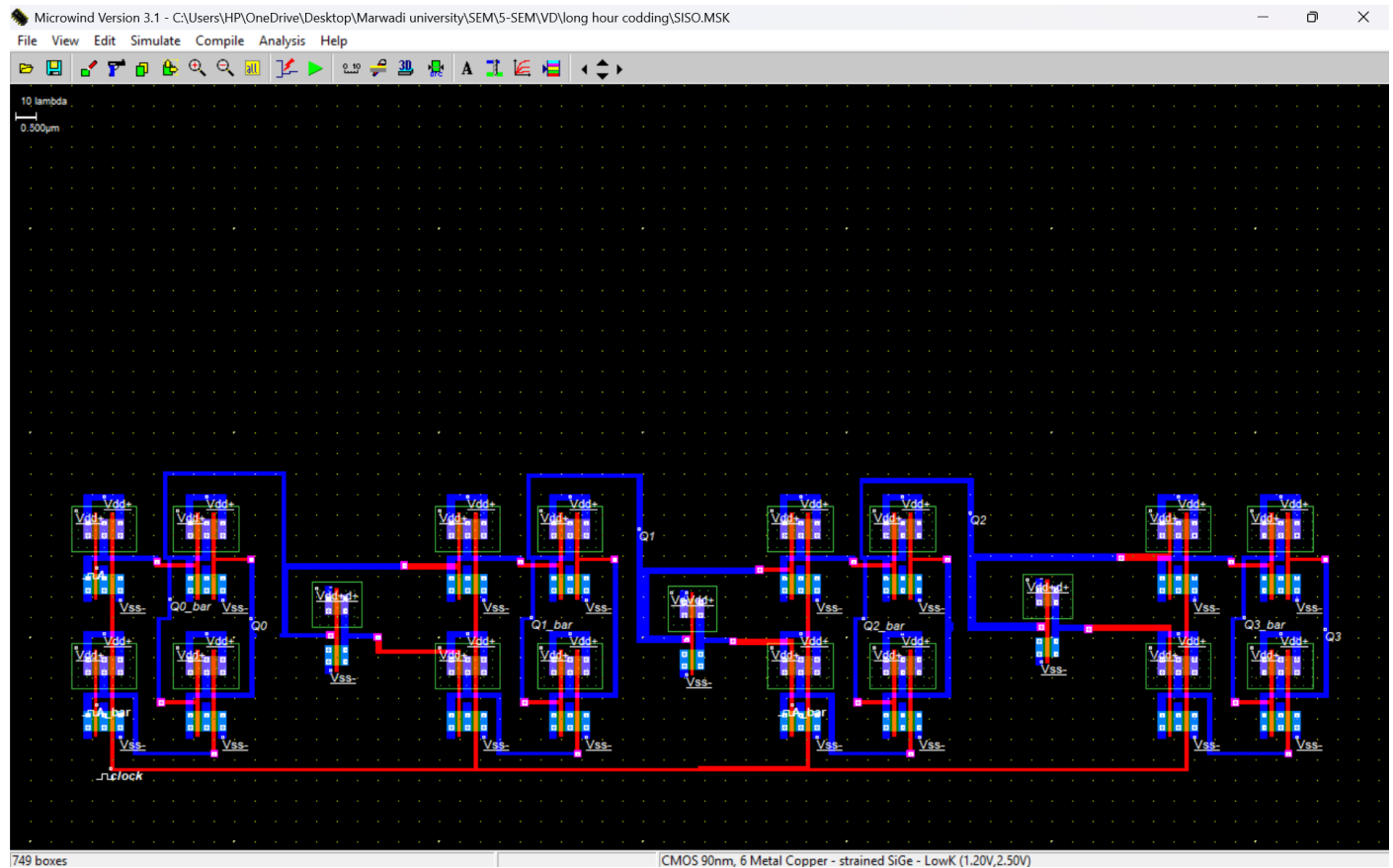Output:

## 4. 4-bit Serial-In Serial-Out (SISO) Register

Circuit Diagrams: -



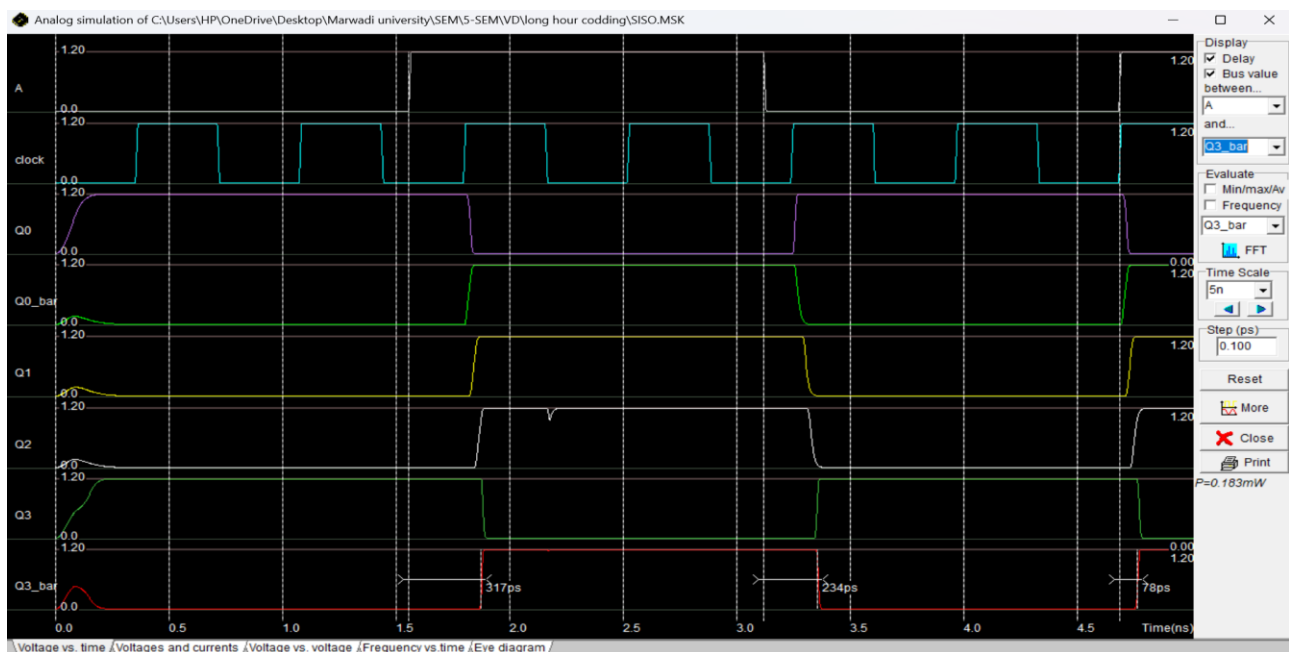Truth table:

| CLK | Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|---|
| Initial (Reset) | 0 | 0 | 0 | 0 |
| After 1st clock pulse | 1 | 0 | 0 | 0 |
| After 2nd clock pulse | 1 | 1 | 0 | 0 |
| After 3rd clock pulse | 1 | 1 | 1 | 0 |
| After 4th clock pulse | 1 | 1 | 1 | 1 |

Screenshots Of Layouts: -



Output:

Conclusion:

Hence Design and implement the transistor level layout 4-bit Full Adder, 8×1 Multiplexer, 1-bit Magnitude Comparator and4-bit Serial-In Serial-Out (SISO) Register using microwind.