Implementation of Nand Gates using Positive Feedback Adiabatic Logic

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Abstract—This paper discuss the impelementation of nand gates using PFAL which gives low power dissipation in adiabatic logic family.In PFAL the circuit uses positive feedback logic to reduce power dissipation by recycling energy. It is to be used for partial energy recovery circuit. It is the best robust ness which is against technological parameter variations

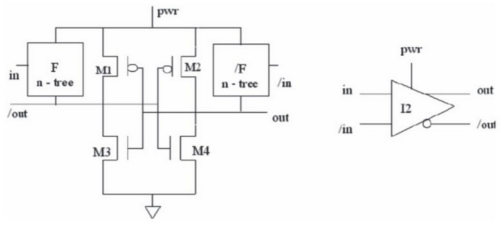
Keywords—Adiabatic logic, PFAL, dissipation

I. Introduction

It comes under the category of partial adiabatic logic It is dual rail circuit. It is used in zigbee communicat ions. It allows a significant reduction of energy dissipation breaking the fundametal limitof static cmos It uses cross coupled transistorswhich shows low energy consumption

Principle of Generation

In PFAL ,a latch is formed by adding two PMOS and two NMOS that avoids a logic level degradation on the output nodes. The two n-tress realize the logic functions. It generates positive and negative outputs. The functional blocks are in parallel with the Pmosfet and form a tramission gate. PMOS transistor will deter- mine the charging path resistance. Decreasing the charging path, resistance of the circuit will improve the performance of the circuit. Due to this logical style of PFAL circuit, the equivalent resistance is smaller when capacitance needs to be charged.

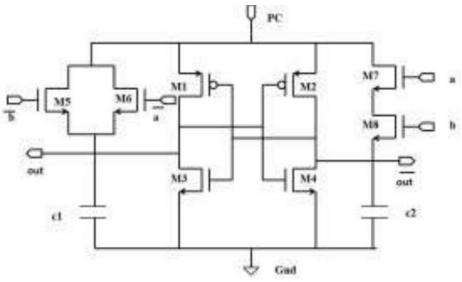


Implementation

The loading and unloading of the load capacitances is performed with voltage ramps which result in a minimized voltage drop over the switching transistors. The voltage ramp is provided by the oscillating power supply PWR. The evaluate (charge) and the recover (discharge) phase should take same time Tcharge as the hold phase in which valid output signals are evaluated by the succeeding stages. An idle phase of the. same duration time is inserted in order to achieve a symmetric trapezoidal waveform, which is advantageous for signal generation

$$E_{adiab} = \frac{R_{\text{charge}} C_L}{T_{\text{charge}}} C_L V_{DD}^2$$

where r is resistance in charging path and the energy is recovered only in charging path



Issues and Improvements

The positive feedback gives some issues it leads to unstability in circuit. Improved version of new logic family called IPFAL Where all npmos and pmos cells are swapped The advantages of using PFAL in designing the logic circuit leads to low energy and power consumption besides it has high maintenance costs.

References

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