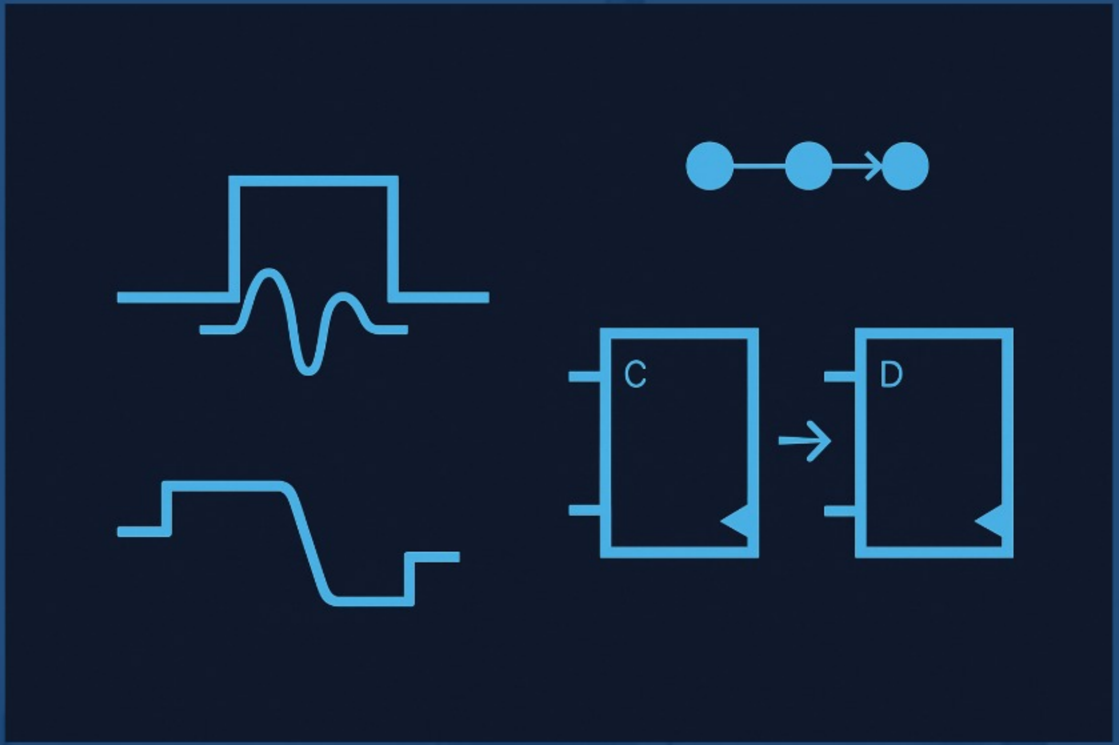


Metastability & Synchronizers

In Digital Systems

What Is Metastability?

- Metastability occurs in a bistable (flip-flop or latch) circuit when, due to a setup/hold timing violation, the circuit is driven to an unstable equilibrium.
- If the input changes right around the clock edge such that setup or hold time is violated, the flip-flop may be forced into that metastable region.
- The metastable output is analog / indeterminate (floating between thresholds) and not valid logic until it resolves.
- Over time (in nanoseconds to picoseconds), it decays (due to internal feedback) toward a valid logic level (0 or 1), influenced by noise or device imbalance.

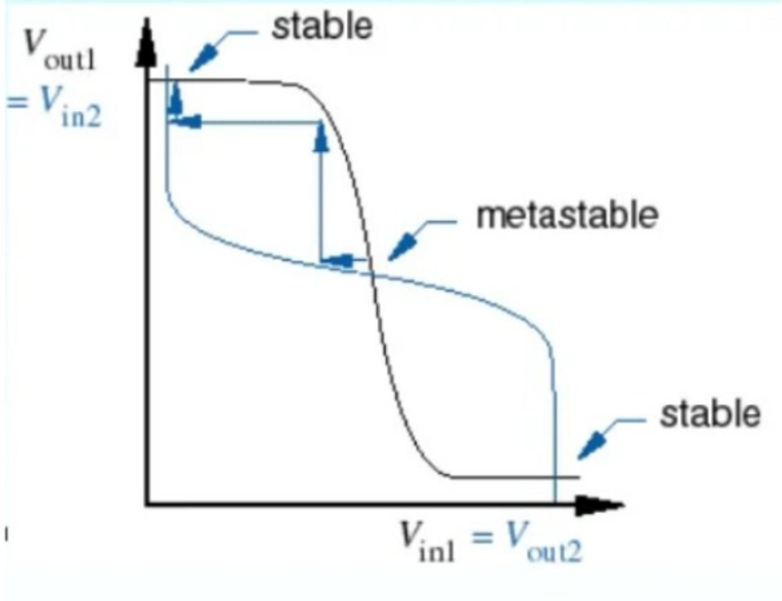
Metastability Probability Model

- Equation :

$$P(T > t) = e^{-\frac{t}{\tau}}$$

Where,

- P(T>t) = Probability that the flip-flop remains in the metastable state beyond time t.
- τ = Time constant of the flip-flop (characteristic decay time)
- If you allow sufficiently large t (e.g. one or more clock cycles), P(T>t) becomes vanishingly small provides practical immunity to metastability.

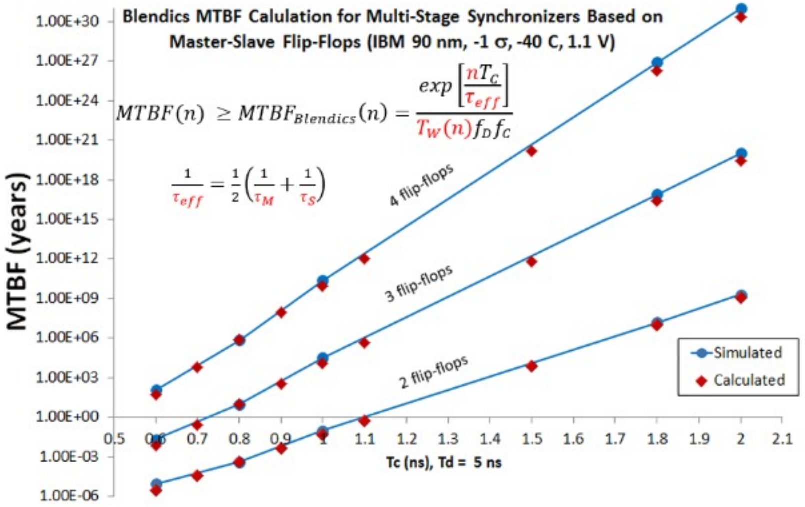


Metastability Probability Model

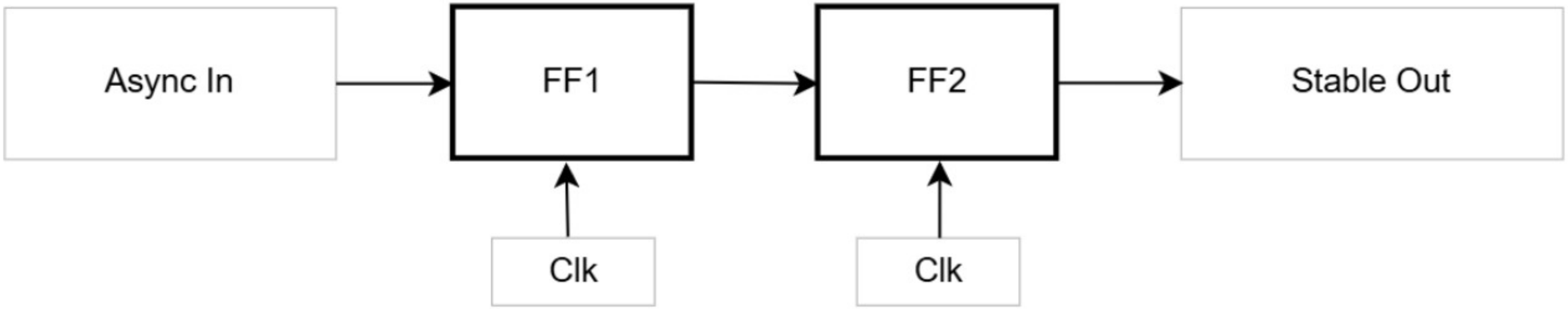
$$\text{MTBF} = \frac{1}{\text{failure rate}} = \frac{e^{S/\tau}}{T_W\, F_C\, F_D}$$

Where,

- T_W = Synchronization window (the vulnerable time window)
- F_C = Clock frequency of the synchronizer (destination clock)
- F_D = Data toggle rate (rate at which input changes)
- S = Available settling time (slack time)
- τ= Time constant of the flip-flop
- ➢ Using 2-FF or 3-FF synchronizer effectively increases S, thus boosting MTBF massively.

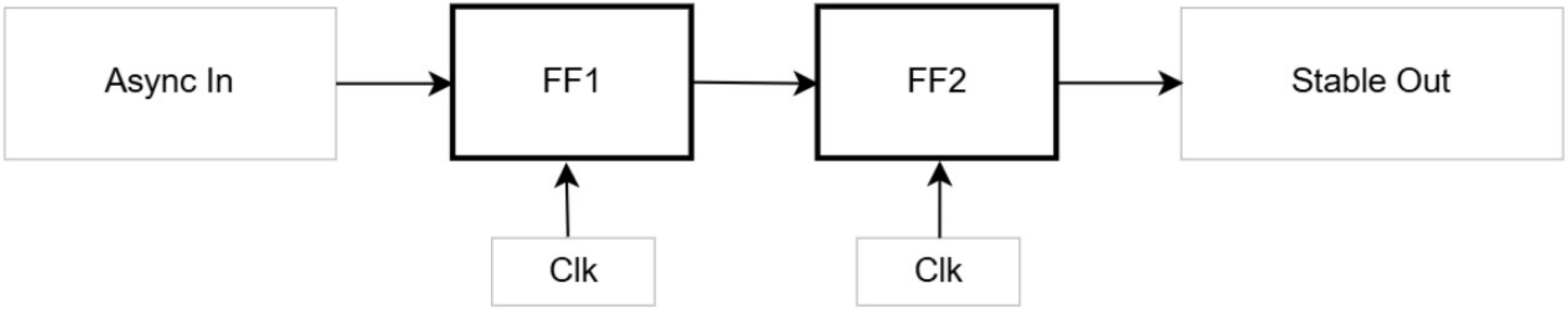

Blendics MTBF Calulation for Multi-Stage Synchronizers Based on Master-Slave Flip-Flops (IBM 90 nm, -1 σ, -40 C, 1.1 V)

Double Flip-Flop Synchronizer



- FF1 may go metastable if async input toggles near clock edge.
- FF2 samples FF1's output one cycle later, after metastability has (with very high probability) resolved.
- Adds 1 cycle latency but produces stable output.
- Widely used in clock domain crossing (CDC) for single-bit signals.

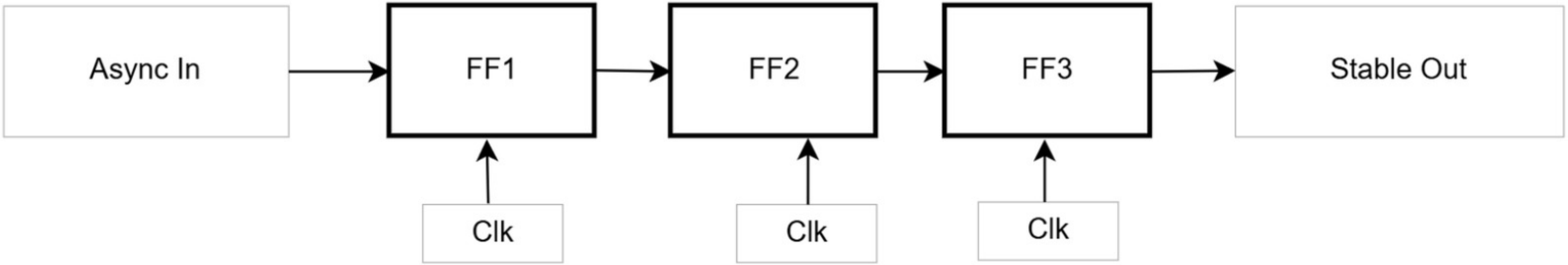
Double Flip-Flop Synchronizer



- Mathematical Impact:

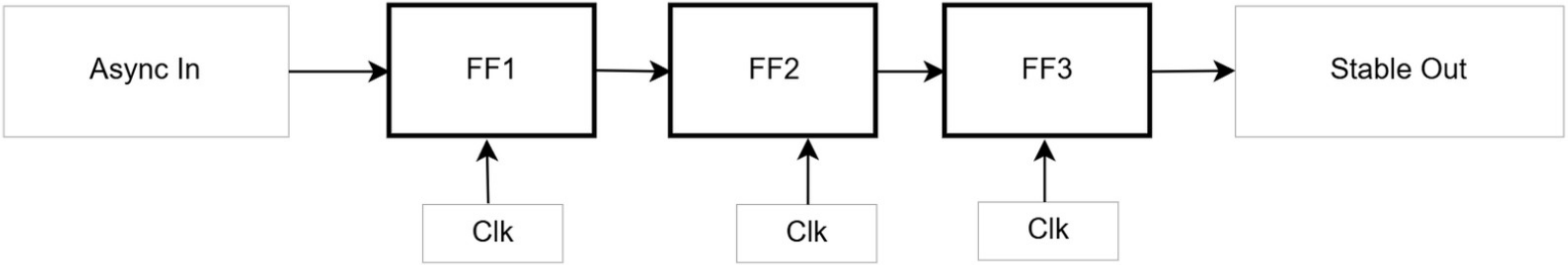
  - Settling Time : S2FF≈S1FF+Tclk
  - MTBF Improvement : $\frac{MTBF_{2FF}}{MTBF_{1FF}} = e^{T_{clk}/\tau}$

Double Flip-Flop Synchronizer



- FF1 may go metastable.
- FF2 provides first resolution cycle, FF3 provides second resolution cycle.
- Logic only uses FF3 output.
- Adds 2 cycle latency, but makes metastability failure probability astronomically low.

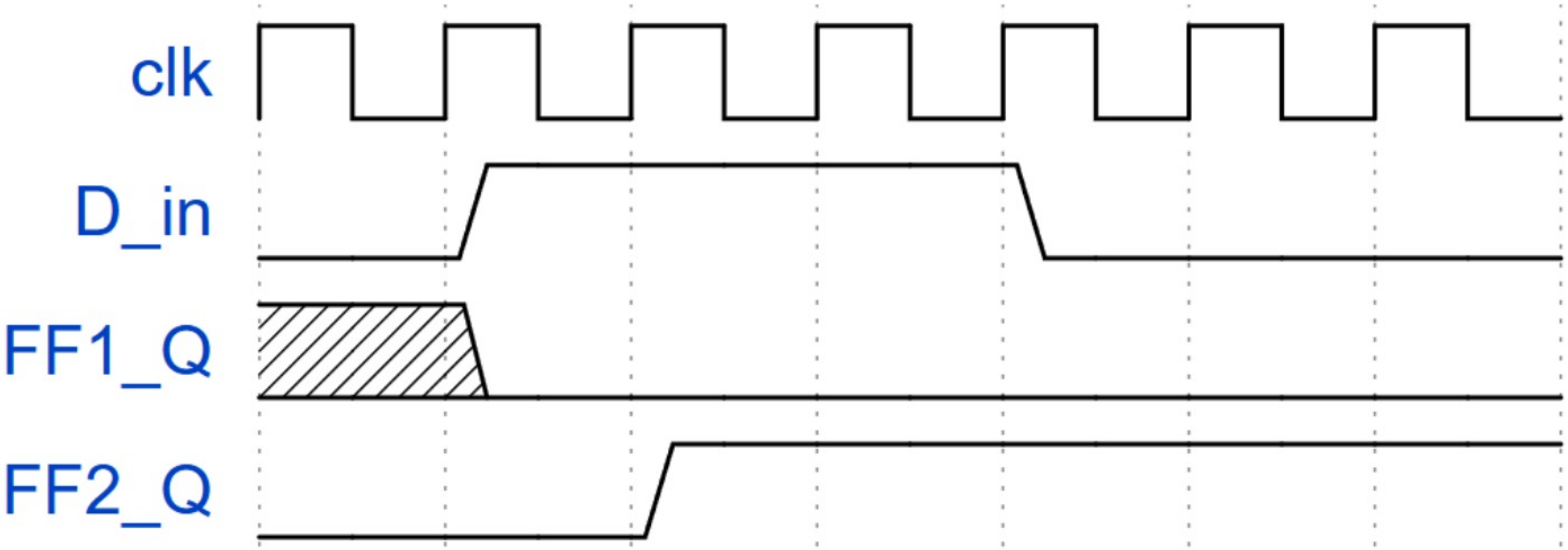
Double Flip-Flop Synchronizer



- Mathematical Impact:
  - Settling Time : S3FF≈S1FF+2Tclk
  - MTBF Improvement : $\frac{MTBF_{3FF}}{MTBF_{2FF}} = e^{T_{clk}/\tau}$

Waveform Illustration

- Metastability cannot be eliminated, but it decays exponentially with time.
- FF1 may output uncertain values for a short time.
- FF2 gives one full clock cycle for metastability to resolve → stable output.



Multi-bit Transfers

Problem with Multi-bit Clock Domain Crossing (CDC):

- Simple synchronizer (2-FF) works for single-bit signals.
- For multi-bit buses, synchronizing each bit independently may cause data corruption:
  - Bits may resolve at different times.
  - Receiver may sample a mixed / invalid word.
- Solutions:
  - Asynchronous FIFO
  - Handshake Protocols
  - Encoder Schemes (Gray Code)

Design Guidelines for Handling Metastability & CDC

For Single-Bit Signals:

- Use 2-FF synchronizer (3-FF if ultra-critical).
- Keep synchronizer FFs physically close (to reduce routing delay).

For Multi-Bit Signals:

- Do not synchronize each bit separately.
- Use asynchronous FIFOs, handshake protocols, or Gray coding.
- Ensure atomic transfer of full data words.