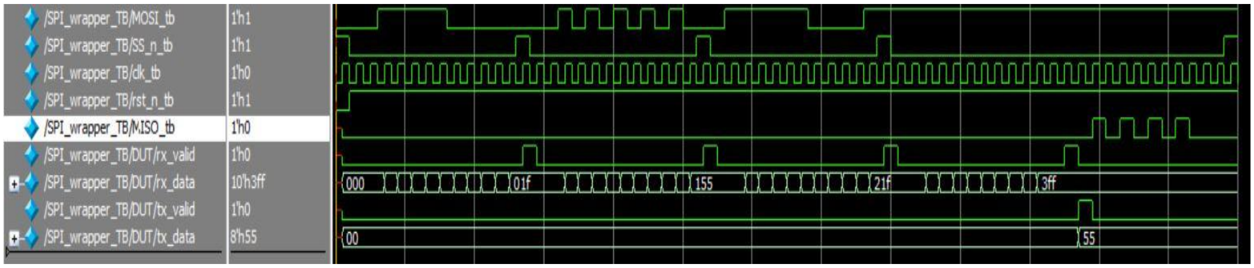
1. Waveforms:




```
# clk = 0 , rst_n = 0 , MOSI = 0 , SS_n = 1 , MISO = x
# clk = 1 , rst_n = 0 , MOSI = 0 , SS_n = 1 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 0 , SS_n = 1 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 0 , SS_n = 1 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 0 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
```

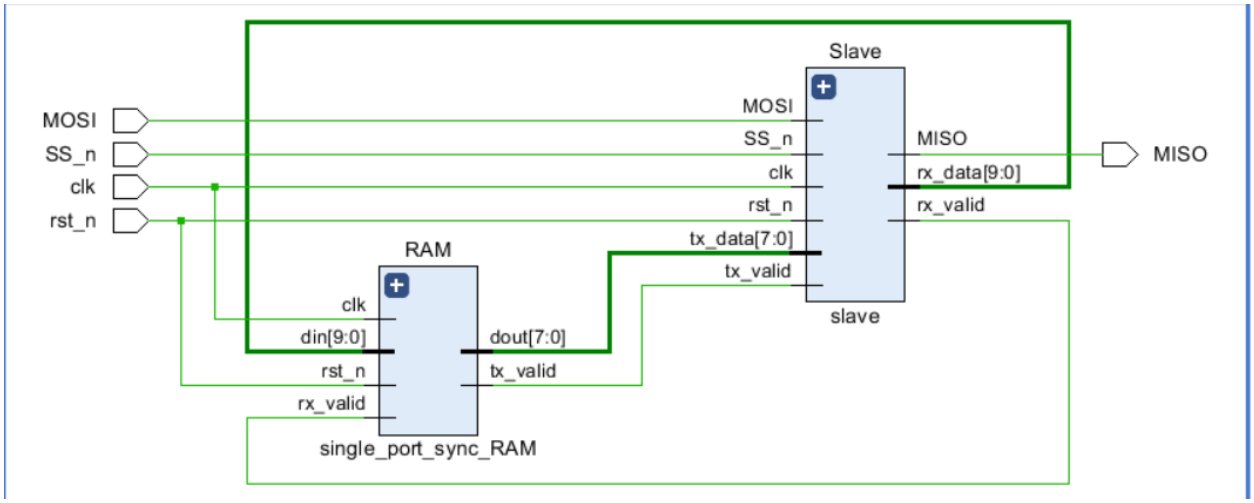
```
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
VSIM 18> run
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 1
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 1
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 1
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 1
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 1
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 1
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 1
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 1
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 0 , MISO = 0
# clk = 0 , rst_n = 1 , MOSI = 1 , SS_n = 1 , MISO = 0
# clk = 1 , rst_n = 1 , MOSI = 1 , SS_n = 1 , MISO = 0
# end
# ** Note: $stop    : E:/SPI/SPI_Wrapper/SPI_wrapper_TB.v(113)
#    Time: 130 ns  Iteration: 1  Instance: /SPI_wrapper_TB
```

2. Questa lint:

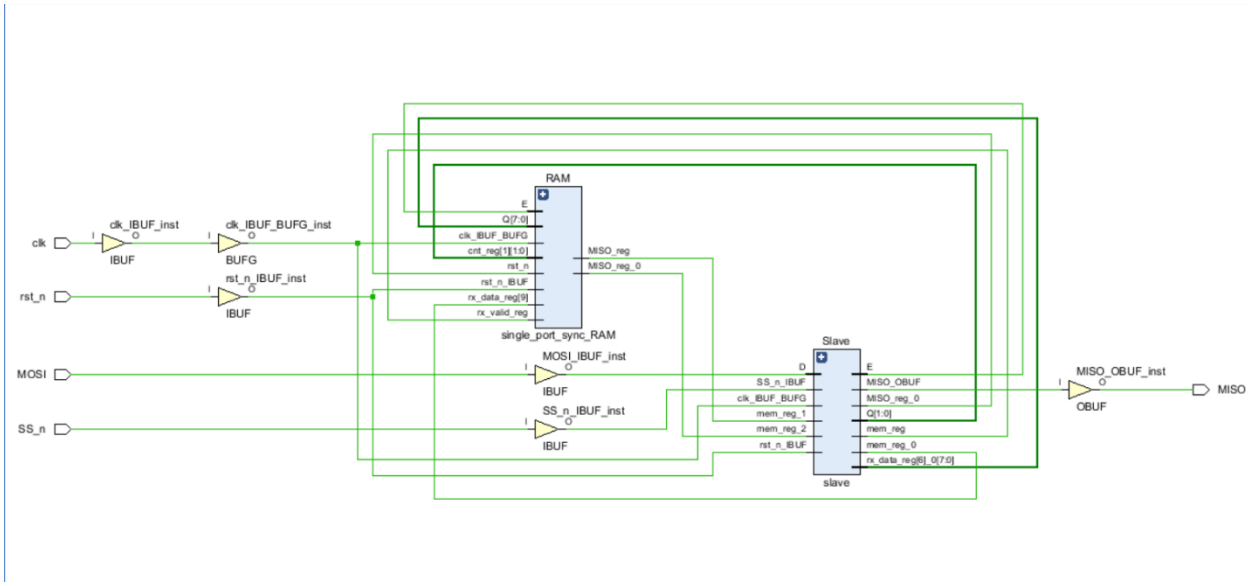
Severity	Status	Check	Alias	Message	Module	Category	S
		if_stmt_shares_arithmetic_operator		If statement has three or more operations sharing the…	slave	Rtl Design Style	ope
		unloaded_input_port		Module input drives no logic. Port tx_valid, Module sla…	slave	Connectivity	ope
		multi_ports_in_single_line		Multiple ports are declared in one line. Module single_…	single_port_sync_RAM	Rtl Design Style	ope
		multi_ports_in_single_line		Multiple ports are declared in one line. Module SPI_w…	SPI_wrapper	Rtl Design Style	ope
		multi_ports_in_single_line		Multiple ports are declared in one line. Module slave, …	slave	Rtl Design Style	ope

- One warning due to line 109 in slave (cnt <= cnt + 1;)
- Info: unloaded input port (tx_valid) but testbench working well as expected.
- Info: multiple ports in single line

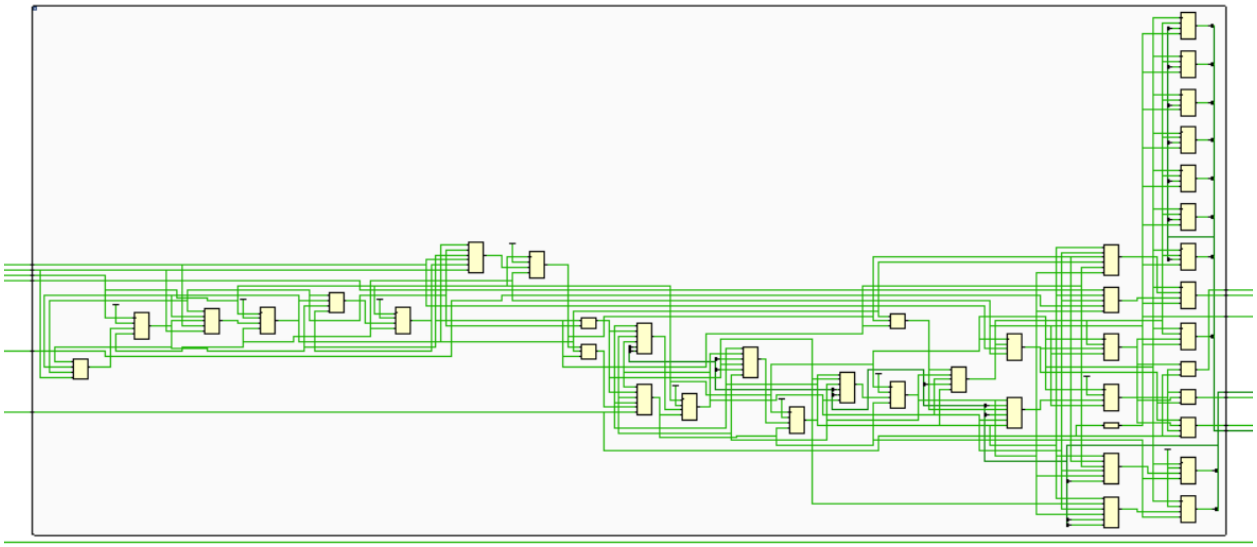
3. Synthesis using Vivado:
    - Gray code:
      Elaborated schematic:



Synthesis schematic:



Slave Synthesis schematic:



FSM encoding:

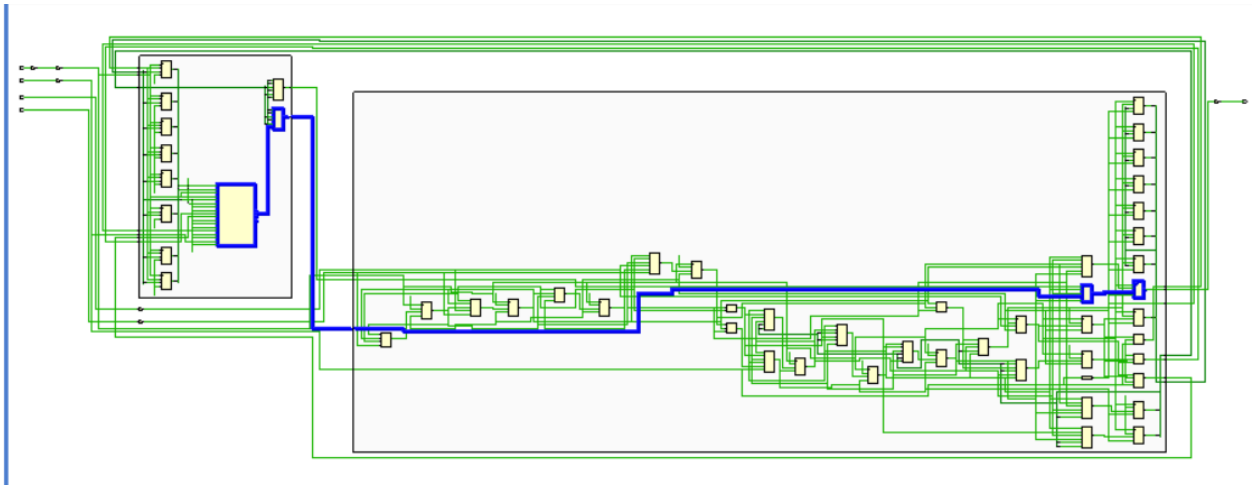
```
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |                Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                             000
                 CHK_CMD |                              111 |                             001
               READ_DATA |                              001 |                             100
                READ_ADD |                              011 |                             011
                   WRITE |                              010 |                             010
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'slave'
```

Timing:

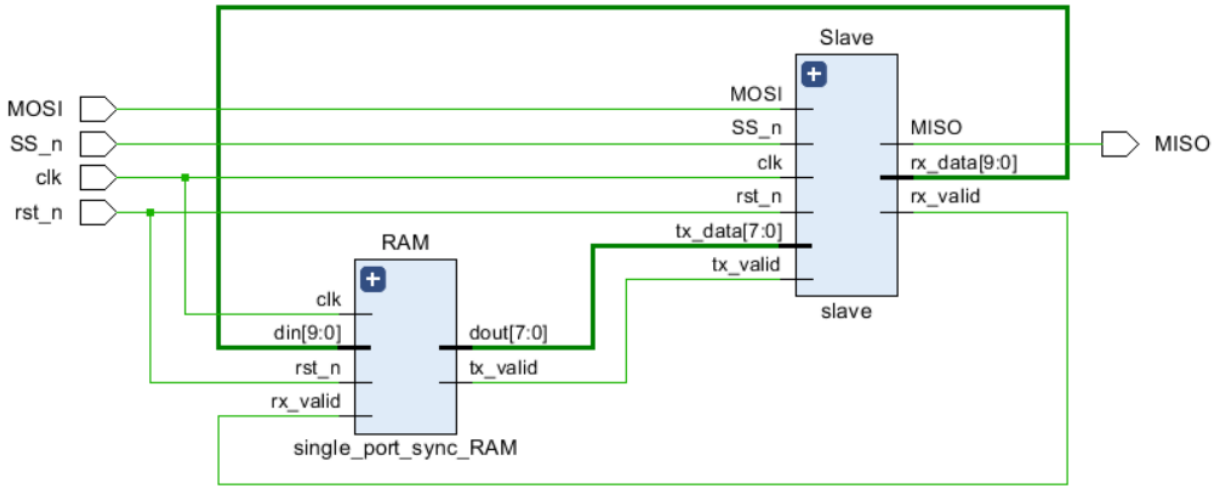
Utilization:

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_wrapper	23	29	0.5	5	1
RAM (single_port_sync...	2	8	0.5	0	0
Slave (slave)	21	21	0	0	0

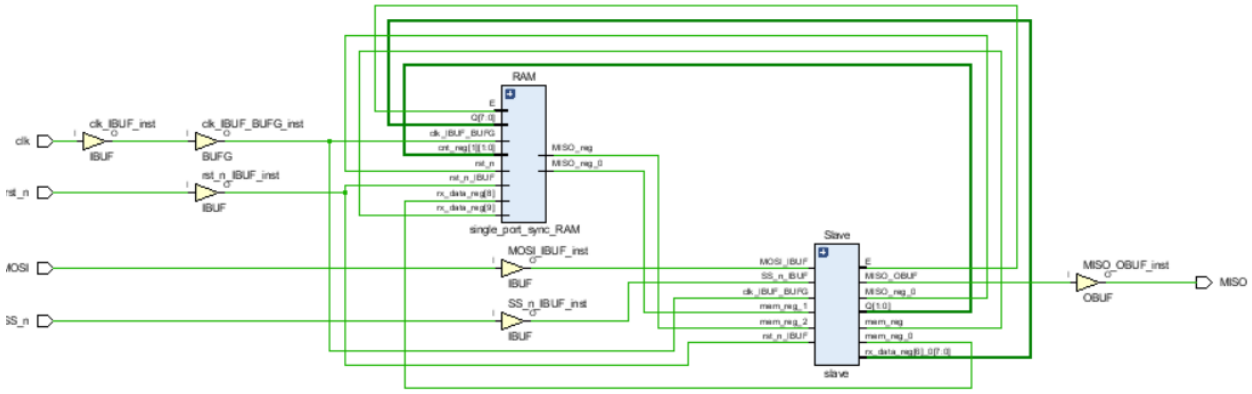
Critical path:



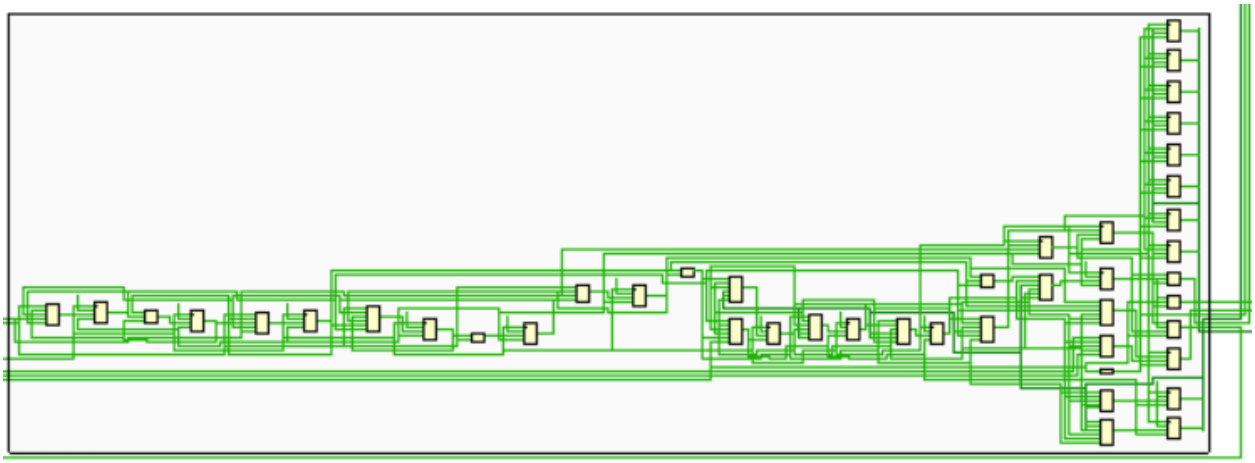
- One-Hot:
  Elaborated schematic:



Synthesis schematic:



Slave synthesis schematic:

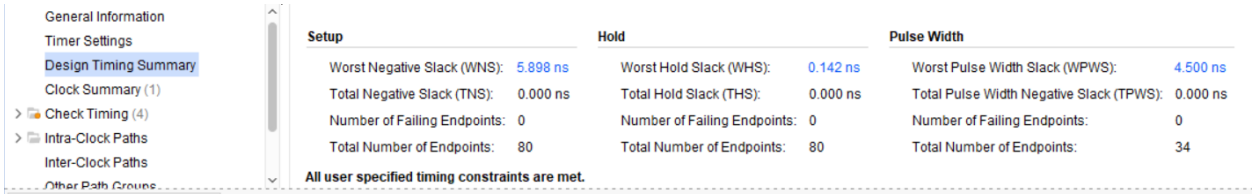


FSM encoding:

State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	10000	001
READ_DATA	00010	100
READ_ADD	00100	011
WRITE	01000	010

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'slave'

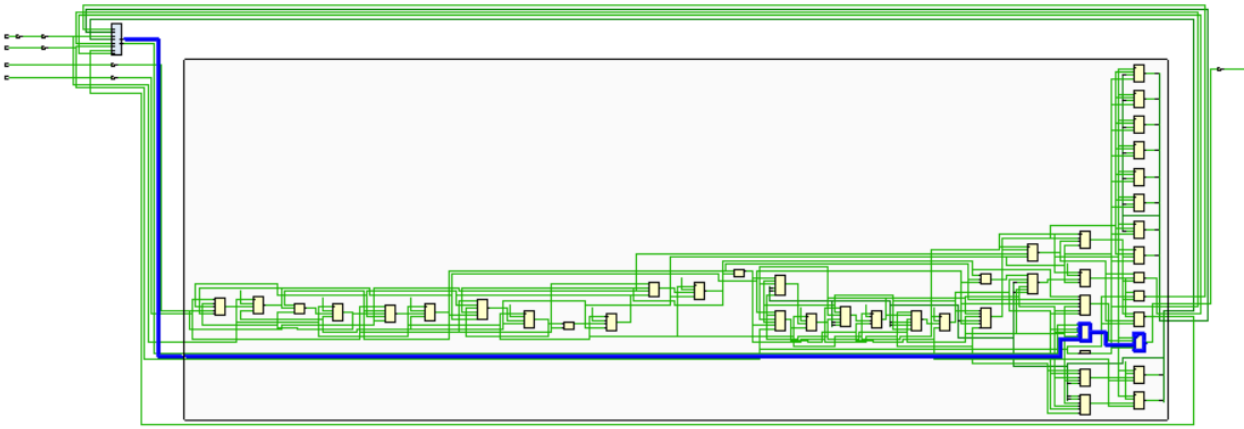
Timing:



Utilization:

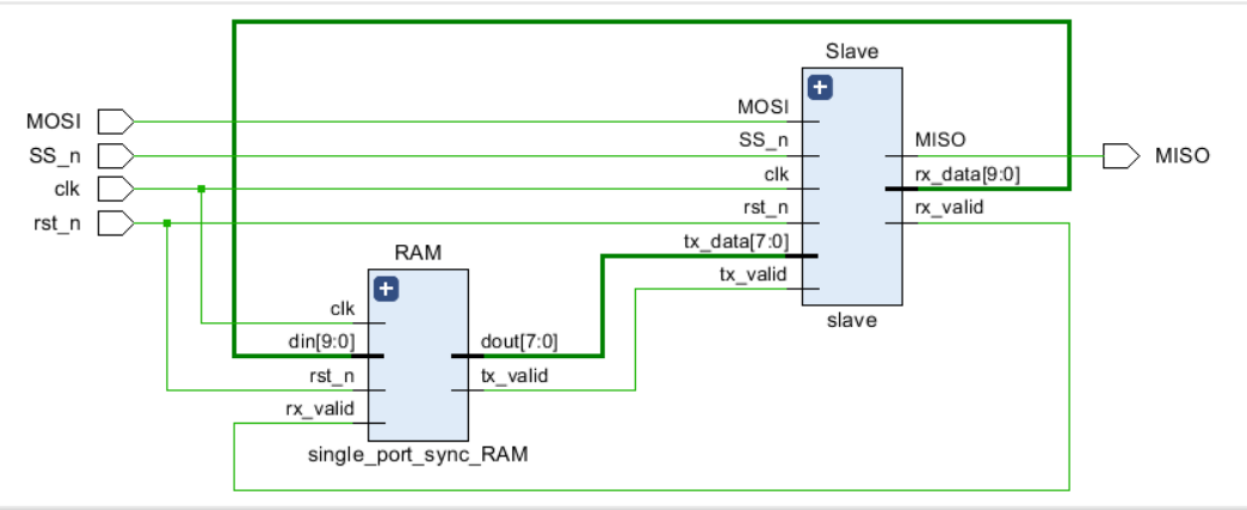
Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_wrapper	24	31	0.5	5	1
RAM (single_port_sync...	2	8	0.5	0	0
Slave (slave)	22	23	0	0	0

Critical path:

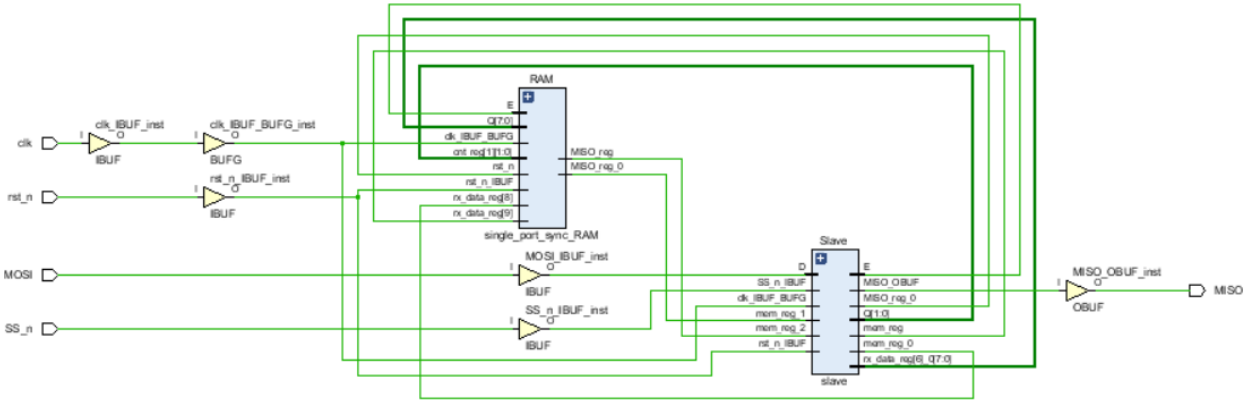


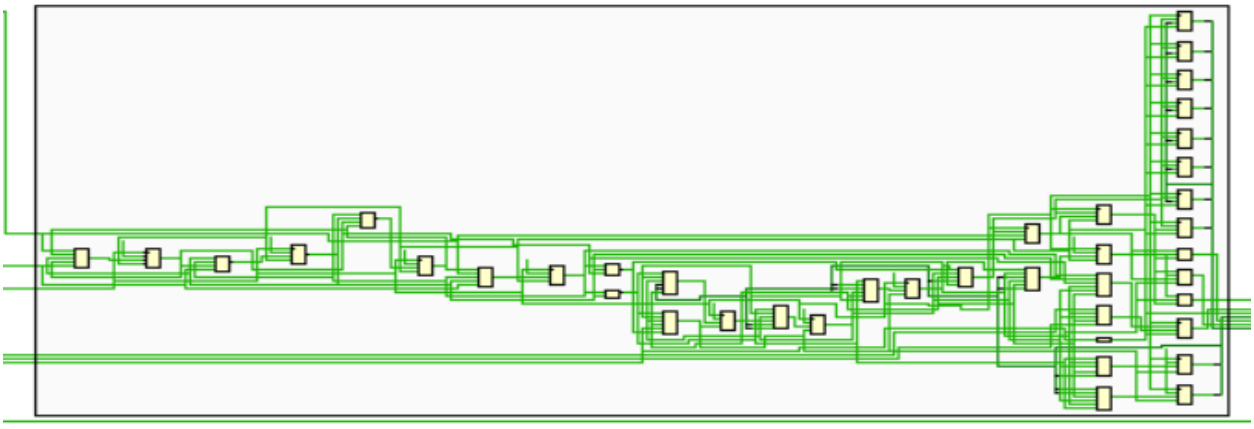
- Sequential:

  Elaborated schematic:



  Synthesis schematic & slave schematic:





FSM encoding:

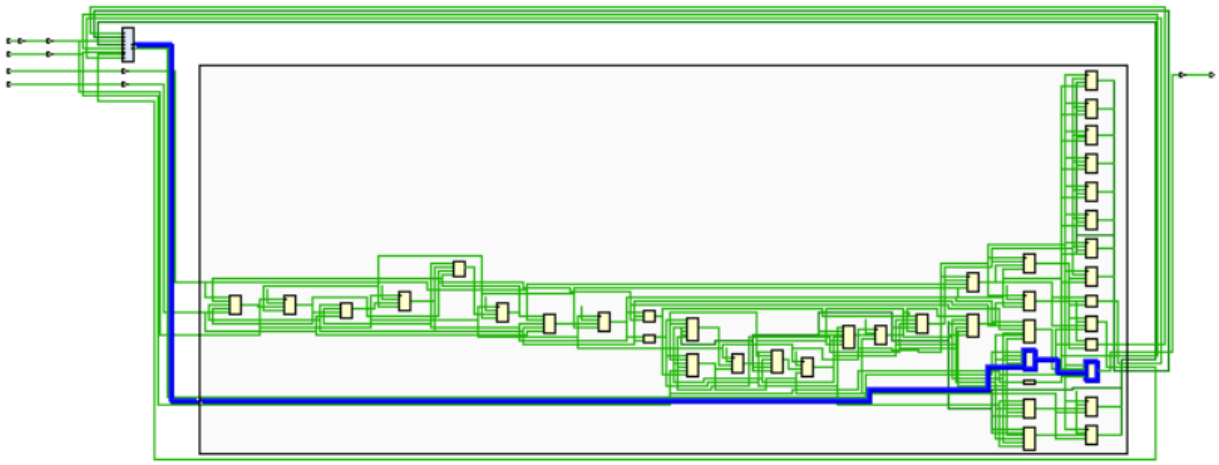
```
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |                Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                             000
                 CHK_CMD |                              100 |                             001
               READ_DATA |                              001 |                             100
                READ_ADD |                              010 |                             011
                   WRITE |                              011 |                             010
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'slave'
---------------------------------------------------------------------------------------------------
```

Timing:

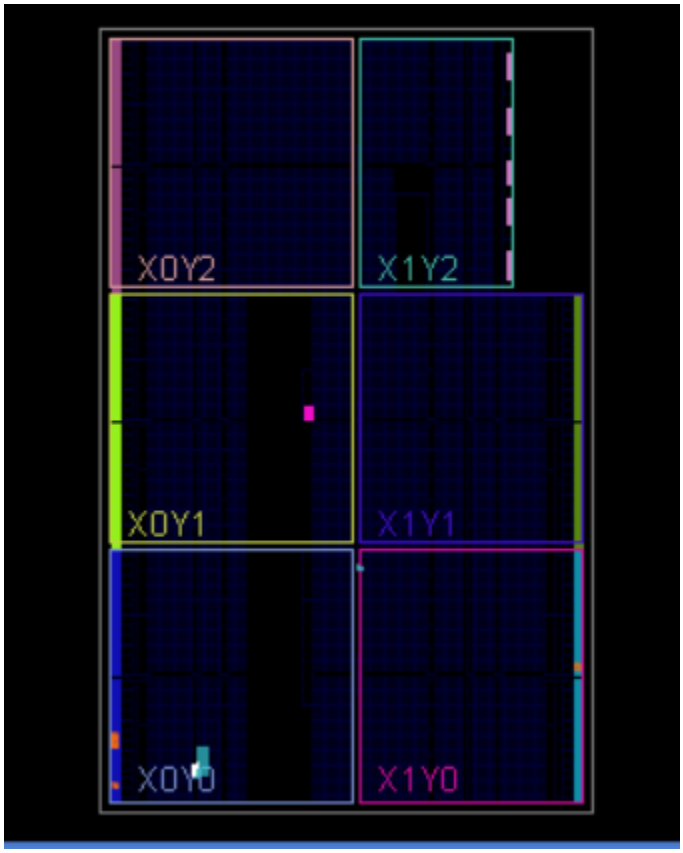
Utilization:

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_wrapper	22	29	0.5	5	1
RAM (single_port_sync...	2	8	0.5	0	0
Slave (slave)	20	21	0	0	0

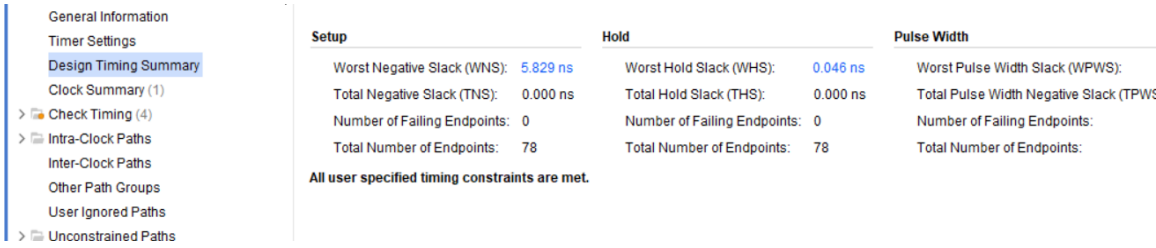
Critical path:



4. Implementation:
    - Grey encoding:



Timing:

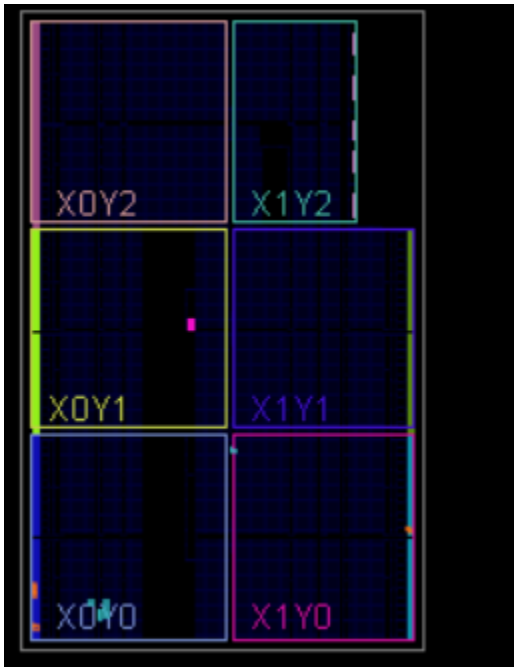


Utilization:

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_wrapper	24	29	11	24	13	0.5	5	1
RAM (single_port_sync...	3	8	3	3	0	0.5	0	0
Slave (slave)	21	21	10	21	12	0	0	0

- One-Hot:

  Device:



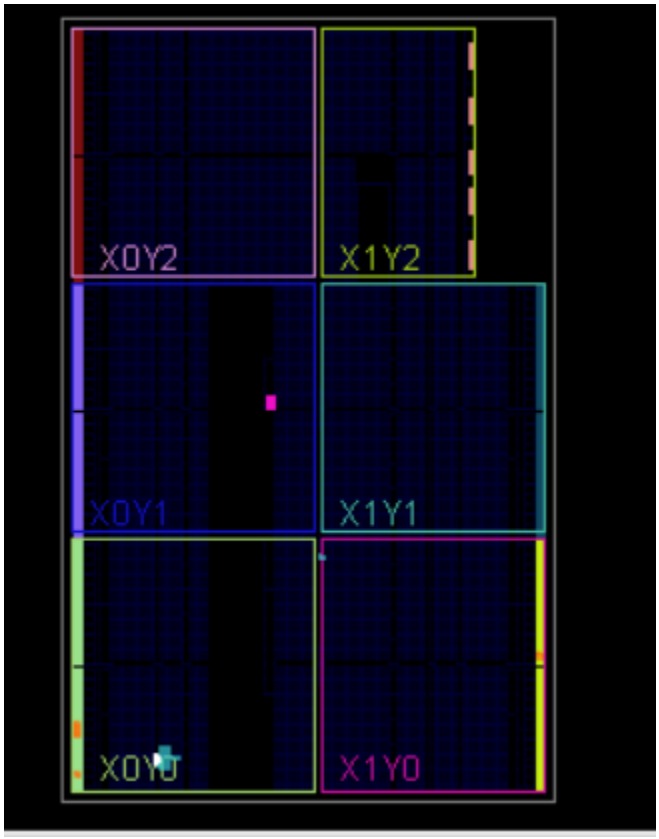
  Timing:

  Utilization:

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_wrapper	25	31	12	25	14	0.5	5	1
RAM (single_port_sync...	3	8	3	3	0	0.5	0	0
Slave (slave)	22	23	10	22	14	0	0	0

- Sequential:

  Device:



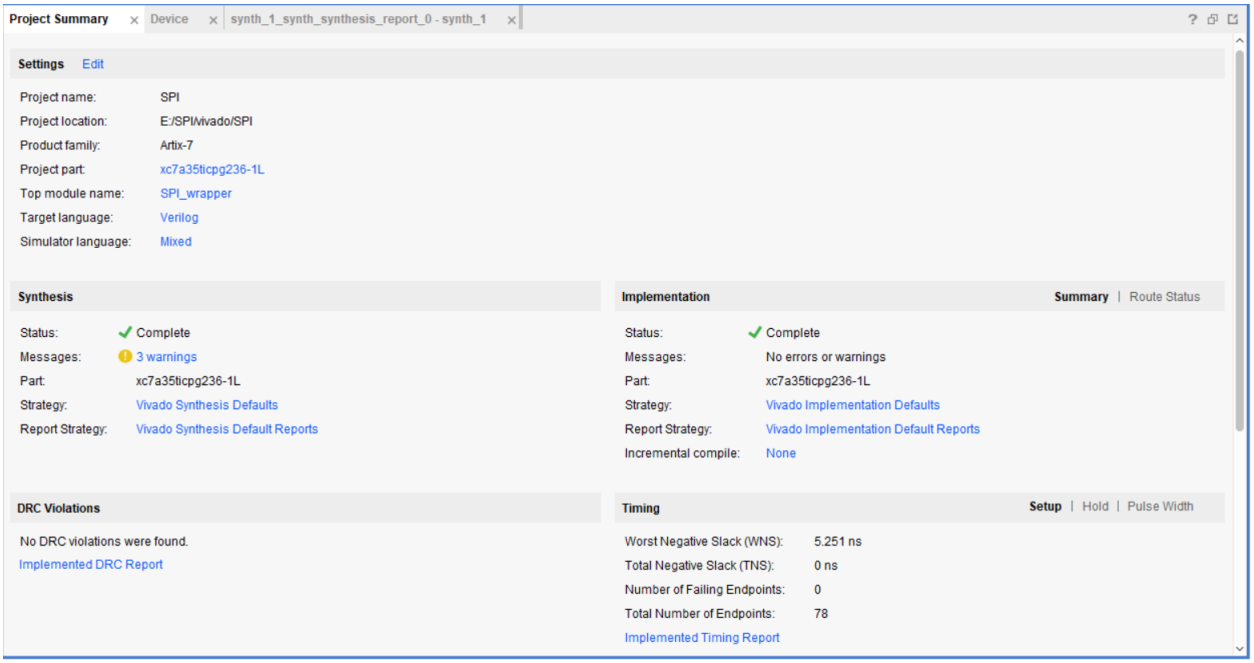
  Timing:

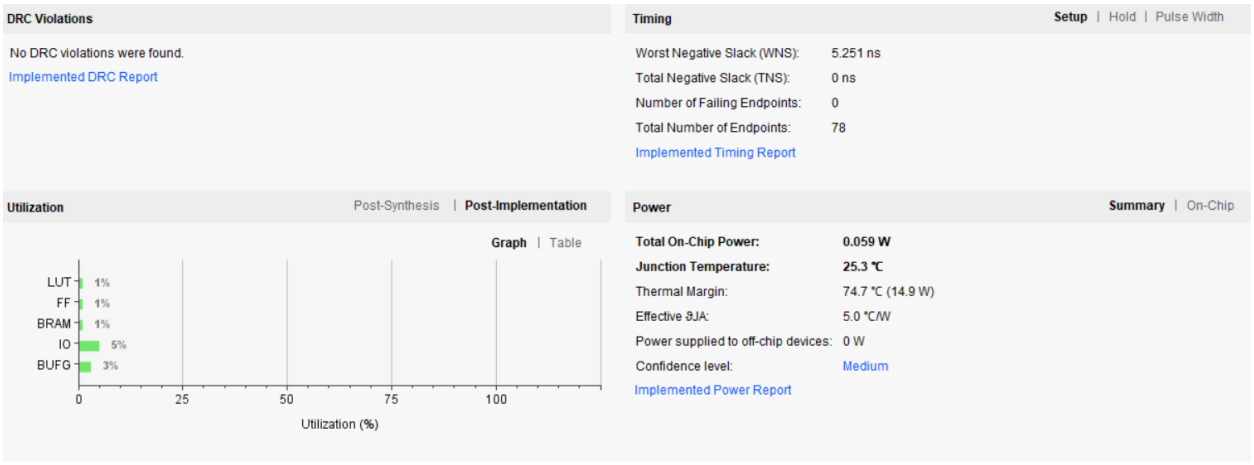
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.251 ns	Worst Hold Slack (WHS):	0.069 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	78	Total Number of Endpoints:	78	Total Number of Endpoints:	32

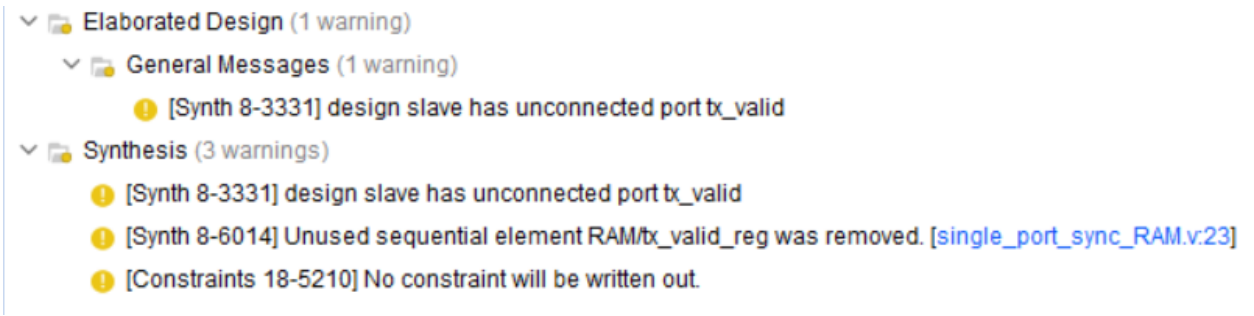
  Utilization:

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_wrapper	23	29	10	23	12	0.5	5	1
RAM (single_port_sync...	3	8	4	3	0	0.5	0	0
Slave (slave)	20	21	8	20	12	0	0	0

5. Massages:


Project Summary
Device
synth_1_synth_synthesis_report_0 - synth_1
Settings Edit
Project name: SPI
Project location: E:/SPI/vivado/SPI
Product family: Artix-7
Project part: xc7a35ticpg236-1L
Top module name: SPI_wrapper
Target language: Verilog
Simulator language: Mixed
Synthesis
Status: Complete
Messages: 3 warnings
Part: xc7a35ticpg236-1L
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Implementation
Summary | Route Status
Status: Complete
Messages: No errors or warnings
Part: xc7a35ticpg236-1L
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental compile: None
DRC Violations
No DRC violations were found.
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): 5.251 ns
Total Negative Slack (TNS): 0 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 78
Implemented Timing Report


DRC Violations
No DRC violations were found.
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): 5.251 ns
Total Negative Slack (TNS): 0 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 78
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
LUT 1%
FF 1%
BRAM 1%
IO 5%
BUFG 3%
0
25
50
75
100
Utilization (%)
Power
Summary | On-Chip
Total On-Chip Power: 0.059 W
Junction Temperature: 25.3 °C
Thermal Margin: 74.7 °C (14.9 W)
Effective ΘJA: 5.0 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Medium
Implemented Power Report


Elaborated Design (1 warning)
General Messages (1 warning)
[Synth 8-3331] design slave has unconnected port tx_valid
Synthesis (3 warnings)
[Synth 8-3331] design slave has unconnected port tx_valid
[Synth 8-6014] Unused sequential element RAM/tx_valid_reg was removed. [single_port_sync_RAM.v:23]
[Constraints 18-5210] No constraint will be written out.