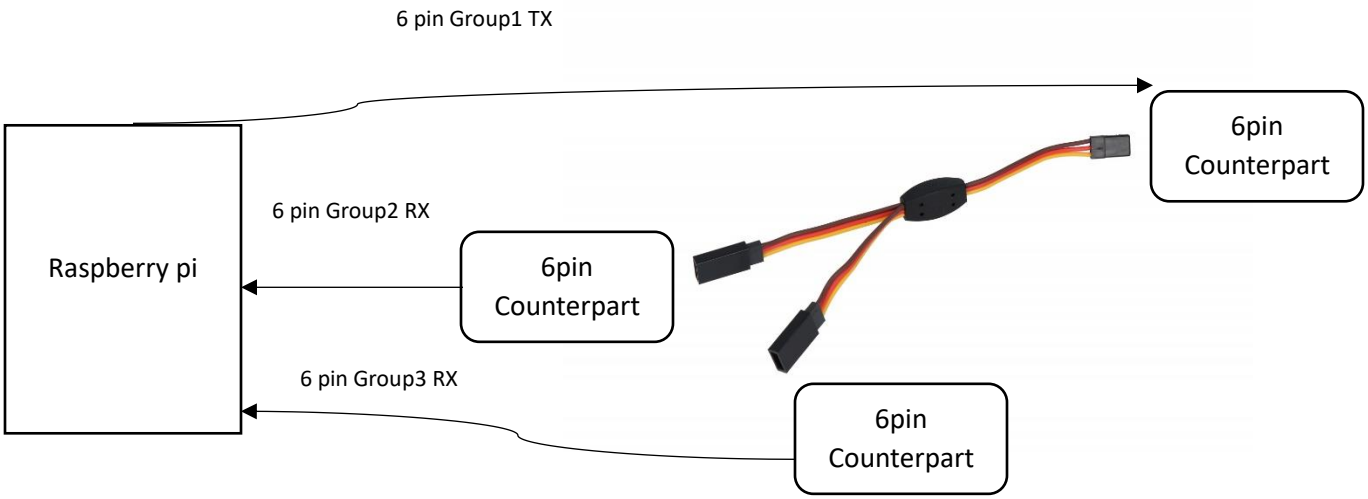
Assumed Architecture

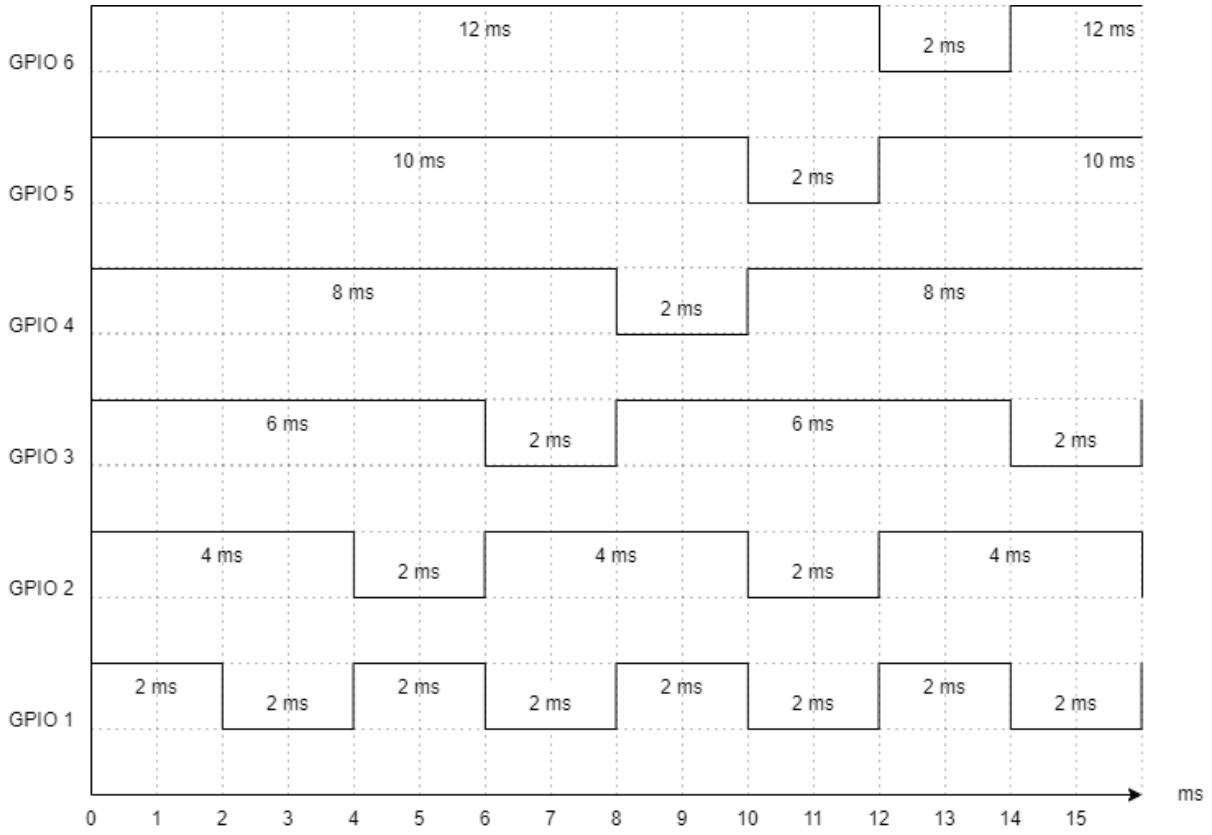
The Raspberry PI provides a large number of GPIO interfaces, with 18 pins being used and categorized into six, each connected to the corresponding parts of Y cable connectors. Please observe below diagram for assumed Architecture



Assumed Algorithm

Our system has 3 groups of GPIOs, each containing 6 pins, with corresponding pins in the other two groups.
so that when a GPIO is set to HIGH on one end, it will be reflected on the other two ends.

we can use one GPIO group in OUTPUT mode and other two in INPUT modes. The task involves sending GPIO pulses with differential width time and observing the pulse width in two other ends. We maintain consistent difference between PULSE WIDTH to avoid close calls.



Each GPIO emits PULSES of variable width with 2ms OFF time (To allow counter reset). This behavior can be read out from their GPIO counterpart