# Computer Components

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April 15, 2023

# The Course Outline

# Course Outline

- **Course Title:** Preparation course for FE examination
- **Intended Participants:** University Students who are going to take ITPEC examinations
- **Course Duration:** 60 hours

# The Lecture Plan

# Lecture Plan: Morning Exam, Sec 2-Computer System, Chapter 1-Computer Components

| Time | Learning Points/Keywo | Explanation Points | Method | Level | Note |
|---|---|---|---|---|---|
| 10 minutes | Processors | General-purpose computer, Server, Process computer, Microcomputer, | Verbal Explanation | **High** | |
| | | PDA (Personal Digital Assistant), Wired logic control, Microprogram control, Accumulator, Complementer | | | |
| | | Instruction address register (instruction counter, program counter, and sequential control counter) | | | |
| | | Instruction register, General register, Index register, Base register, SVC (SuperVisor Call) interrupt | | | |
| | | I/O interrupt, Cycle time, FLOPS, Instruction mix, Pipeline, Super-pipeline, Superscalar | | | |
| | | VLIW, SISD, SIMD, MISD, MIMD, Loosely coupled multiprocessor system, Tightly coupled multiprocessor | | | |
| 10 minutes | Memory | RAM, ROM, DRAM, RAM, Flash memory, Auxiliary memory, Disk cache | Verbal Explanation | **High** | |
| | | Write through, Write back, Memory interleave, Bank, Read-only, Write-once, Rewritable | | | |
| | | Hard disk, CD (CD-ROM, CD-R), DVD (DVD-ROM, DVD-RAM, DVD-R) | | | |
| | | Flash memory (USB memory, SD card), Floppy disk, Streamer, RAM file | | | |
| 10 minutes | Buses | Address bus, Data bus, Control bus, System bus, Memory bus, I/O bus, | Verbal Explanation | Low | |
| | | PCI, Serial bus, Parallel bus, Bus access mode | | | |
| 10 minutes | I/O interfaces and drivers | USB, RS-232C, IEEE 1394, SCSI, Serial ATA, Bluetooth, IrDA, Star connection, Cascade connection | Verbal Explanation | Medium | |
| | | Hub, Daisy chain, Terminator, Tree connection, Program control, Device driver | | | |

# Objectives

## 1.1 Understand Processors***

- Understand the types and characteristics of memory, and apply them to associated matters.
- Understand the mechanisms of storage devices, including the configuration of the main memory, configuration of the memory system, and storage hierarchy, and apply them to associated matters.
- Understand the types and characteristics of storage media, and apply them to associated matters.

# Keywords

## 1.1 Understand Processors***

- General-purpose computer, Server, Process computer, Microcomputer , PDA (Personal Digital Assistant), Operation, Control , Storage, Input, Output , Wired logic control, Microprogram control , Accumulator, Complementer , Instruction address register (instruction counter, program counter, and sequential control counter), Instruction register, General register, Index register, Base register, SVC (SuperVisor Call) interrupt, I/O interrupt, Cycle time, FLOPS, Instruction mix, Pipeline, Super-pipeline, Superscalar , VLIW, SISD, SIMD, MISD, MIMD, Loosely coupled multiprocessor system, Tightly coupled multiprocessor system

# Objectives

## 1.2 Understand Memory***

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- Understand the types and characteristics of storage media, and apply them to associated matters.

# Keywords

## 1.2 Understand Memory***

- RAM, ROM, DRAM, RAM, Flash memory, Auxiliary memory, Disk cache, Write through, Write back, Memory interleave, Bank, Read-only, Write-once, Rewritable, Hard disk, CD (CD-ROM, CD-R), DVD (DVD-ROM, DVD-RAM, DVD-R), Flash memory (USB memory, SD card), Floppy disk, Streamer, RAM file

# Objectives

## 1.3 Understand Buses

- Understand an outline of the types, characteristics, and configurations of buses.

# Keywords

## 1.3 Understand Buses

- Address bus, Data bus, Control bus, System bus, Memory bus, I/O bus, PCI, Serial bus, Parallel bus, Bus access mode

# Objectives

**1.4 Understand I/O interfaces and drivers****

- Understand the types and characteristics of a typical I/O interface, and apply them to associated matters.
- Understand the basic role and functions of a device driver.

# Keywords

## 1.4 Understand I/O interfaces and drivers**

- USB, RS-232C, IEEE 1394, SCSI , Serial ATA, Bluetooth, IrDA, Star connection, Cascade connection, Hub, Daisy chain, Terminator, Tree connection, Program control, Device driver

# Objectives

**1.5 Understand I/O devices****

- Understand the types and characteristics of typical I/O devices, and apply them to associated matters.
- Understand the types and characteristics of a typical auxiliary storage device, and apply them to associated matters.

# Keywords

## 1.5 Understand I/O devices**

- OLED (Organic Light Emitting Diode) display , Plasma display,Interlaced mode, Non-interlaced mode, Blu-ray drive, DVD-R/RW drive, agnetic tape unit, Track, Cylinder, locking factor, BG (Interblock Gap), Sector, Defragmentation

# Analyzation

# Analyzation

- Analyzed 31 questions
- Covered the most recent years
  - 2021 Q1 Exam
  - 2021 Q2 Exam
  - 2020 Q2 Exam

# Questions

# Question 1

Q1. (q2-1) When an instruction that involves access to the main memory is executed, which of the following is an operation that is performed between "instruction decode" and "operand fetch"?

a. Calculation of an effective address
b. Start of an I/O device
c. Calculation of a branch address
d. Occurrence of an interrupt

Q1. (q2-1) When an instruction that involves access to the main memory is executed, which of the following is an operation that is performed between "instruction decode" and "operand fetch"?
Theme: Computer Components, Category: FE

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b. Start of an I/O device
c. Calculation of a branch address
d. Occurrence of an interrupt

# Question 1: Answer Explanation: Slide I

An instruction is executed in the order of **"instruction fetch →instruction decode → effective address calculation →operand fetch → execution."** Therefore, the "operation that is performed between "instruction decode" and "operand fetch" is a) Calculation of an effective address. Here, an operand refers to the data on which the instruction is to be processed. This operand uses various types of addressing modes, which are classified as follows:

- **Direct addressing:** specification of an address in the main memory
- **Index addressing:** specification of an address in the main memory by using the result of adding the value of an index register to the value of the address part
- **Relative addressing:** specification of a position relative to the position where the its own instruction is stored

# Question 1: Answer Explanation: Slide II

- **Indirect addressing:** specification of the address of the target data in the main memory by using a value stored in an address in the main memory that is indicated in the address part
- **Register addressing:** specification of an address stored in a register
- **Immediate addressing:** specification of the value of the address part as the target data

# Question 2

Q2. (q2-2) Which of the following causes an external interrupt?

a. A page fault that occurs when a non-existent page is accessed under virtual memory management
b. A privileged instruction violation that occurs when a system management instruction is executed under the general user mode
c. Machine check due to a hardware failure
d. Operation exception, such as an overflow caused by a floating-point operation instruction

Q2. (q2-2) Which of the following causes an external interrupt?
Theme: Computer Components, Category: FE

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b. A privileged instruction violation that occurs when a system management instruction is executed under the general user mode
c. Machine check due to a hardware failure
d. Operation exception, such as an overflow caused by a floating-point operation instruction

# Question 2: Answer Explanation: Slide I

- **Interrupts** include internal interrupts that occur as a result of the execution of an instruction within a program, and external interrupts that occur regardless of an executing instruction.
  Among the options, an interrupt that occurs when a hardware failure is detected as described in c) is classified as an external interrupt.
  Each of the interrupts mentioned above includes the following:
- **External interrupts:** An I/O interrupt (e.g., completion of an I/O operation or malfunction of the I/O device), a timer interrupt (e.g., timeout of a timer), and a machine check interrupt (e.g., hardware malfunction or power failure)
- **Internal interrupts:** A supervisor call interrupt (e.g., usage of an OS function by a SVC instruction or system call instruction of the running program), and a program interrupt (e.g., divide-by-zero, overflow, execution of an invalid instruction, or page fault)

# Question 2: Answer Explanation: Slide II

- a) A page fault that occurs when a page that does not exist in the main memory is accessed by a program instruction is classified as an internal interrupt.
- b) Generally, a system management instruction, which is an OS function, is executed in kernel mode (also called the privileged mode and supervisor mode), and if a privileged instruction such as a system management instruction is executed under the user mode in which general application programs are executed, a privileged instruction violation occurs. Since this privileged instruction violation is a program interrupt, it is classified as an internal interrupt.
- d) A floating-point operation is performed by a program instruction, and as a result, an overflow generates a program interrupt classified as an internal interrupt.

# Question 3

Q3. (q2-3) Which of the following is an appropriate description concerning the clock frequency of the CPU in a PC?

a. The timing of instruction execution in the CPU changes depending on the clock frequency. The speed of instruction execution increases with the clock frequency.

b. The communication speed of the LAN changes depending on the clock frequency. The communication speed of the LAN increases with the clock frequency.

c. The rotation speed of the hard disk changes depending on the clock frequency. The rotation speed increases with the clock frequency, and the transfer rate of the hard disk increases.

d. The interrupt interval of the real-time processing changes depending on the clock frequency. The interrupt frequency increases with the clock frequency, and the processing speed of the real-time processing increases.

Q3. (q2-3) Which of the following is an appropriate description concerning the clock frequency of the CPU in a PC?
Theme: Computer Components, Category: FE

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c. The rotation speed of the hard disk changes depending on the clock frequency. The rotation speed increases with the clock frequency, and the transfer rate of the hard disk increases.
d. The interrupt interval of the real-time processing changes depending on the clock frequency. The interrupt frequency increases with the clock frequency, and the processing speed of the real-time processing increases.

# Question 3: Answer Explanation: Slide I

- **Clock frequency** is the frequency of a signal (clock) generated to determine the timing of an internal operation of a computer, and is expressed in MHz (megahertz) and GHz (gigahertz).
  One MHz indicates that the signal is generated one million times in one second, and one GHz means that the signal is generated one billion times in one second. Since the CPU operates synchronously with the clock, generally, the speed of execution of an instruction increases with the frequency.
  Therefore, the description of a) is appropriate.
- b) The clock frequency is related to the CPU operation, and does not control the communication speed.
- c) The clock frequency is related to the CPU operation, and the rotation speed of a disk is a value specific to a device.

# Question 3: Answer Explanation: Slide II

- d) The clock frequency is related to the CPU operation, and the interrupt interval of real-time processing is not directly related to the clock frequency.

# Question 4

Q4. (q2-4) A CPU runs at 1 GHz and is capable of executing one machine-language instruction in an average time of 0.8 clocks. Approximately how many million instructions can this CPU execute in one second?

a. 1.25
b. 2.5
c. 800
d. 1,250

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Theme: Computer Components, Category: FE

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c. 800
d. 1,250

# Question 4: Answer Explanation: Slide I

A clock is a signal for determining the timing of an internal operation of a CPU. The clock frequency represents the number of signals generated in one second in MHz (megahertz) or GHz (gigahertz). Normally, a single instruction consists of several basic operations, which are performed in one clock cycle, and therefore, one instruction is executed in several clock cycles. However, when multiple instructions of machine language are executed simultaneously by using a technique called superscalar, the average number of clock cycles for the execution of an instruction can be reduced to below one. Since the CPU runs at one GHz, this CPU generates one giga clock signals in one second. One clock period is
$1$ ( second) $\div$ $1$ G
$= 10^9$ (seconds).
Next, since this CPU "is capable of executing one machine instruction in 0.8 clock cycles on average," the average execution time of one instruction

# Question 4: Answer Explanation: Slide II

is $0.8 \times 10^{-9}$ seconds. Therefore, the number of instructions that can be executed in one second is as follows:
1 (second) $\div$ $0.8 \times 10^{-9}$ (seconds/instruction)
$= 10^9 \div 0.8$
$=$ 1,000,000,000 $\div$ 0.8
$=$ 1,250 million instructions
Therefore, d) is the correct answer.

# Question 5

Q5. (q2-5) A CPU has a clock frequency of 1 GHz. When the instruction type of the CPU consists of two types as shown in the table below, what is the approximate performance in MIPS of the CPU?

| Instruction type | Execution time(clock) | Frequency of appearance (%) |
|---|---|---|
| Instruction 1 | 10 | 60 |
| Instruction 2 | 5 | 40 |

a. 34
b. 100
c. 125
d. 133

Q5. (q2-5) A CPU has a clock frequency of 1 GHz. When the instruction type of the CPU consists of two types as shown in the table below, what is the approximate performance in MIPS of the CPU?

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| Instruction 2 | 5 | 40 |

Theme: Computer Components, Category: FE

a. 34
b. 100
c. 125
d. 133

# Question 5: Answer Explanation

A clock frequency of 1 GHz indicates that clock signals are generated $1 \times 10^9$ times in one second. The average instruction execution time (average number of clock cycles necessary for executing one instruction) of the CPU is calculated from the table of assigned instruction types, and the performance is calculated by dividing the clock frequency by the average instruction execution time.

Average instruction execution time

$= 10 \times 0.6 + 5 \times 0.4 = 8$ (clocks)

Performance $= (1 \times 10^9) \div 8 = 125{,}000{,}000$ (instructions/second)

This becomes 125 MIPS when it is converted to MIPS (Million Instructions Per Second).

Therefore, c) is the correct answer.

# Question 6

Q6. (q2-6) Which of the following is an explanation of pipeline processing in a processor?

a. It is a method in which multiple processors are synchronized with each other to process multiple data in parallel, based on a single instruction.

b. It is a method in which the execution time required for a single instruction in a single processor is made as short as possible.

c. It is a method in which a single processor executes multiple instructions simultaneously by slightly shifting them in stages.

d. It is a method in which multiple processors process multiple data, based on their own instructions.

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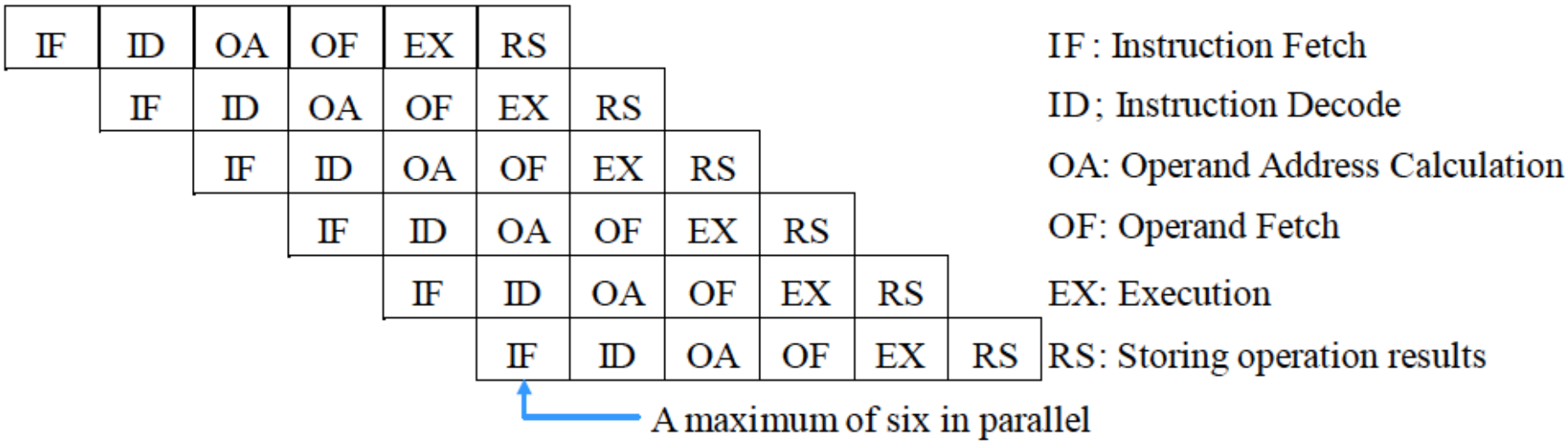
# Question 6: Answer Explanation: Slide I

As shown in the figure below, pipeline processing is a method in which a single processor executes multiple instructions simultaneously by slightly shifting them in stages.
Therefore, c) is the correct answer.




**Example of pipeline processing**

# Question 6: Answer Explanation: Slide II

- a) This is an explanation of the SIMD (Single Instruction stream Multiple Data streams) method. This method is suitable for matrix operations.
- b) This is an explanation concerning a processor in which pipeline processing is not adopted.
- d) This is an explanation of the MIMD (Multiple Instruction streams Multiple Data streams) method. This method is applicable to a multiprocessor system.

# Question 7

Q7. (q2-7) Which of the following is an explanation of superscalar?

a. It is a method for splitting a vector to be processed into a set of vectors with the same length as the vector register when the length of the vector is longer than that of the vector register, and then repeating the process.

b. It is a method for increasing speed with more deeply staged pipelines.

c. It is a method for increasing speed by enabling the simultaneous execution of multiple instructions with multiple pipelines.

d. It is a method for increasing speed by using a long instruction word and simultaneously controlling multiple functional units with a single instruction.

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b. It is a method for increasing speed with more deeply staged pipelines.

c. It is a method for increasing speed by enabling the simultaneous execution of multiple instructions with multiple pipelines.

d. It is a method for increasing speed by using a long instruction word and simultaneously controlling multiple functional units with a single instruction.

# Question 7: Answer Explanation

- **Superscalar** is the technique of simultaneously executing multiple instructions by further dividing the pipeline mechanism into multiple stages with increased processing performance during the execution of multiple instructions.
  Therefore, c) is the correct answer.
  In the CPU, when multiple instructions are to be processed in parallel, the simultaneous execution of interrelated multiple instructions must be avoided. In superscalar, the CPU performs this control in the hardware. VLIW (Very Long Instruction Word), on the other hand, omits the time-consuming operation of determining the possibility of parallel processing by the CPU through the compilation of an extremely large group of instructions that must be processed in sequence into a single instruction.
- a) This is an explanation concerning a vector processor.
- b) This is an explanation concerning a super-pipeline.
- d) This is an explanation concerning VLIW.

# Question 8

Q8. (q2-8) Which of the following is the architecture that allows one instruction to perform multiple instances of the same operation simultaneously for different data, and is implemented on CPUs that are designed for multimedia data processing?

a. MIMD
b. MISD
c. SIMD
d. SISD

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c. SIMD
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# Question 8: Answer Explanation: Slide I

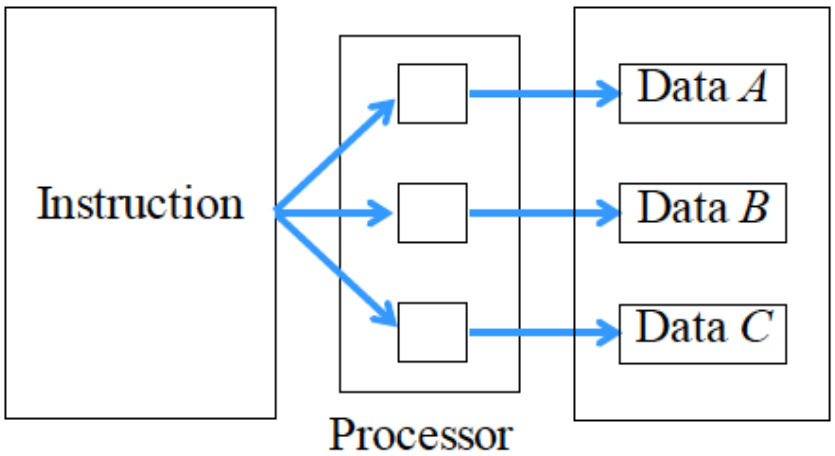
- The method that allows one instruction to perform multiple instances of the same operation simultaneously for different data is c) SIMD (Single Instruction stream Multiple Data streams).
  SIMD is suitable for multimedia data processing in which the same operation is often repeated for continuous data, and typical examples include processors called GPU (Graphics Processing Unit) that are used exclusively for image processing and vector computers. All options are a classification of CPU called the Flynn's taxonomy, where S indicates Single, M indicates Multiple, I indicates Instruction, and D indicates Data, and if it is understood that the options are a combination of these, all options need not be memorized.
  The details other than the correct answer are as follows:

# Question 8: Answer Explanation: Slide II

- a) MIMD (Multiple Instruction streams Multiple Data streams) Multiple processors process multiple data in parallel based on individual instructions for each data. This method is applicable to a general multiprocessor.
- b) MISD (Multiple Instruction streams Single Data stream) A single piece of data is processed by multiple instructions, but a processor based on this method is not yet implemented in a practical way.
- d) SISD (Single Instruction stream Single Data stream) A single piece of data is processed by a single instruction. This method is applicable in a general computer that is controlled sequentially by a single processor.

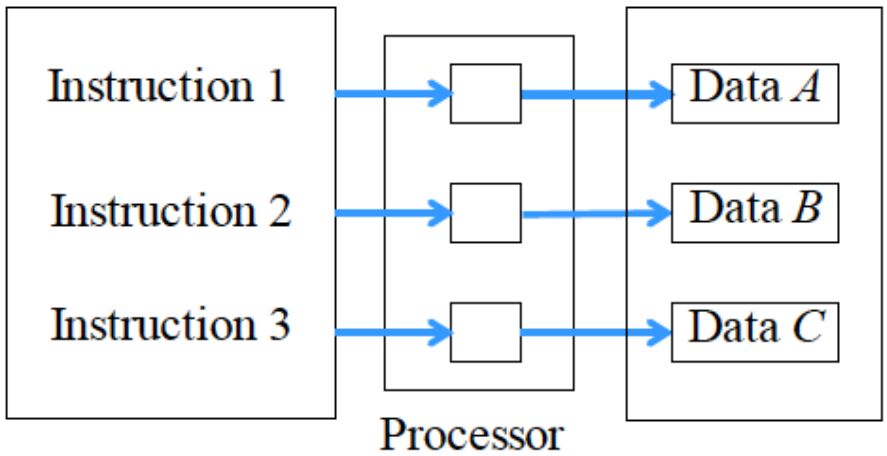
# Question 8: Answer Explanation: Slide III

SIMD method




Different processors execute the same instruction for different data.

MIMD method




Different processors execute different instructions for different data.

# Question 9

Q9. (q2-9) Which of the following is an appropriate explanation of DRAM?

a. It represents one bit depending on whether or not the capacitor is electrically charged. It is often used as the main memory.

b. Data is written during the manufacturing process. It is used as a memory for storing microprograms.

c. Data can be written by a dedicated device, and can be erased by ultraviolet irradiation.

d. It is composed of flip-flops. Although the access speed is fast, the manufacturing cost is high. It is used for cache memory.

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# Question 9: Answer Explanation

- As described in a), DRAM ( Dynamic Random Access Memory) is memory that stores one (1) bit depending on whether or not each capacitor is electrically charged. Since DRAM is composed of tiny capacitors, the stored charge is discharged over time, and an operation called "refresh" by which the content is rewritten every few milliseconds if necessary. Although the access speed is slower than SRAM (Static RAM) because of this refresh operation, a simple circuit makes the unit cost per bit low, and memory with a large capacity is easy to manufacture. Therefore, main memory is usually composed of DRAM chips.
- b) It is an explanation of mask ROM (Read Only Memory).
- c) It is an explanation of EPROM (Erasable Programmable ROM).
- d) It is an explanation of SRAM.

# Question 10

Q10. (q2-10) Which of the following is the storage device that has the shortest access time?

a. CPU L2 cache memory
b. CPU register
c. Hard disk
d. Main memory

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# Question 10: Answer Explanation

- In the storage hierarchy, the closer a storage device is to the CPU, the shorter the access time is in general, and the one-time access amount is also small. Inside the CPU, the register that is always used when instructions are executed has the shortest access time, and therefore, b) is the correct answer.
- When storage devices are arranged in order of shortest access time first after the register, the order is generally as described below. The approximate access time of each device and the storage capacity must be known.
- CPU register $<$ primary (L1) or secondary (L2) cache memory of CPU $<$ main memory $<$ hard disk $<$ (optical disk such as CD and DVD) $<$ (magnetic tape)

# Question 11

Q11. (q2-11) Which of the following is an appropriate description concerning cache memory?

a. It is implemented in two methods. In one method, when a write instruction is executed, data is written to both cache memory and main memory. In the other method, data is written only to cache memory, and is written back into main memory only when it is flushed.

b. If a cache miss occurs, an interrupt is generated and data is transferred from main memory to cache memory by the program.

c. Cache memory is used to bridge the difference in capacity between real memory and virtual memory.

d. Due to a remarkable improvement in the access speed of semiconductor memory, the necessity of cache memory is decreasing.

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d. Due to a remarkable improvement in the access speed of semiconductor memory, the necessity of cache memory is decreasing.

# Question 11: Answer Explanation: Slide I

- The cache memory is a high-speed buffer storage (a holding area for temporary storage) that is implemented for bridging the difference in the speed of the main memory and CPU. By deploying the memory content that has a high probability of being accessed in cache memory, the access frequency to the main memory is reduced and speed is improved. When a write instruction is executed, the "write through" method rewrites both the cache memory and main memory, and the "write back" method rewrites the cache memory first, and then the main memory when the relevant data is flushed from the cache memory.
  Therefore, a) is appropriate.
- b) When a cache miss occurs, generally the data is processed in the hardware within the instruction execution cycle, and an interrupt does not occur.

# Question 11: Answer Explanation: Slide II

- c) The purpose of the cache memory is to bridge the difference in the speed of the main memory and CPU. It is not meant to bridge the difference in the capacity of the real memory and virtual memory. In reality, the capacity of the cache memory is very small as compared to the capacity of the real memory.
- d) Along with an improvement in the access speed of the semiconductor memory, the operation speed of the CPU is also improving. Because of this, the difference in the speed is not being bridged. As a result, the necessity of the cache memory is not decreasing.

# Question 12

Q12. (q2-12) Which of the following is a combination of the access time and hit ratio for cache memory, and the access time for main memory that has the shortest effective access time for the main memory?

| | Cache memory | | Main memory |
|---|---|---|---|
| | Access time (nanoseconds) | Hit ratio (%) | Access time (nanoseconds) |
| a) | 10 | 60 | 70 |
| b) | 10 | 70 | 70 |
| c) | 20 | 70 | 50 |
| d) | 20 | 80 | 50 |

Q12. (q2-12) Which of the following is a combination of the access time and hit ratio for cache memory, and the access time for main memory that has the shortest effective access time for the main memory?

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|---|---|---|---|
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| b) | 10 | 70 | 70 |
| c) | 20 | 70 | 50 |
| d) | 20 | 80 | 50 |

Theme: Computer Components, Category: FE

- Option d)

# Question 12: Answer Explanation: Slide I

In order to bridge the difference in the processing performance of the CPU and the access speed of main memory, a cache memory that supports high-speed access is placed between the two. The hit ratio is the probability of existence of the target data in the cache memory. If the target data does not exist in the cache memory, the data is read from the main memory, but if the hit ratio is $p$, the probability will become $1 - p$. If the access time of the cache memory is $T_c$ and the access time of the main memory is $T_m$, the effective access time is $T_c \times p + T_m \times (1 - p)$. If calculation is performed based on the values of each option, d) has the shortest access time as shown below:

- a) $10 \times 0.6 + 70 \times (1 - 0.6) = 6 + 28 = 34$ (nanoseconds)
- b) $10 \times 0.7 + 70 \times (1 - 0.7) = 7 + 21 = 28$ (nanoseconds)
- c) $20 \times 0.7 + 50 \times (1 - 0.7) = 14 + 15 = 29$ (nanoseconds)
- d) $20 \times 0.8 + 50 \times (1 - 0.8) = 16 + 10 = 26$ (nanoseconds)

# Question 13

Q13. (q2-13) The access time of the cache memory and main memory of systems A and B are as shown in the table below. The hit ratio and effective access time of the cache memory when a particular program is executed in system A are the same as when the program is executed in system B. Which of the following is the hit ratio of the cache memory in such a case?

**Unit:** nanosecond

| | System *A* | System *B* |
|---|---|---|
| Cache memory | 15 | 10 |
| Main memory | 50 | 70 |

a. 0.2
b. 0.3
c. 0.5
d. 0.8

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|---|---|---|
| Cache memory | 15 | 10 |
| Main memory | 50 | 70 |

Theme: Computer Components, Category: FE

a. 0.2
b. 0.3
c. 0.5
d. 0.8

# Question 13: Answer Explanation

If the access time of the cache memory is $T_c$, the access time of the main memory is $T_m$, and the hit ratio is $h$, the effective access time is $T_c \times h + T_m \times (1 - h)$. Since the hit ratio and effective access time of both systems are the same, h can be calculated as follows:

Effective access time of system A = Effective access time of system B

$15 \times h + 50 \times (1 - h) = 10 \times h + 70 \times (1 - h)$

15h + 50 - 50h = 10h + 70 - 70h

25h = 20

h = 0.8.

Therefore, the hit ratio is d) 0.8.

# Question 14

Q14. (q2-14) Which of the following is an appropriate explanation of memory interleaving?

a. In order to improve the speed of access to main memory from the CPU, data is written simultaneously in both the cache memory and main memory.

b. In order to improve the speed of access to main memory from the CPU, the main memory is internally divided into multiple banks and each bank is accessed concurrently.

c. In order to eliminate the bottleneck that is caused by the difference in the access speed of the CPU and main memory, a high-speed and low-capacity memory is allocated.

d. In order to remove factors that disrupt pipeline processing, the cache memory is divided into two segments: one for instructions and the other for data.

Q14. (q2-14) Which of the following is an appropriate explanation of memory interleaving?

Theme: Computer Components, Category: FE

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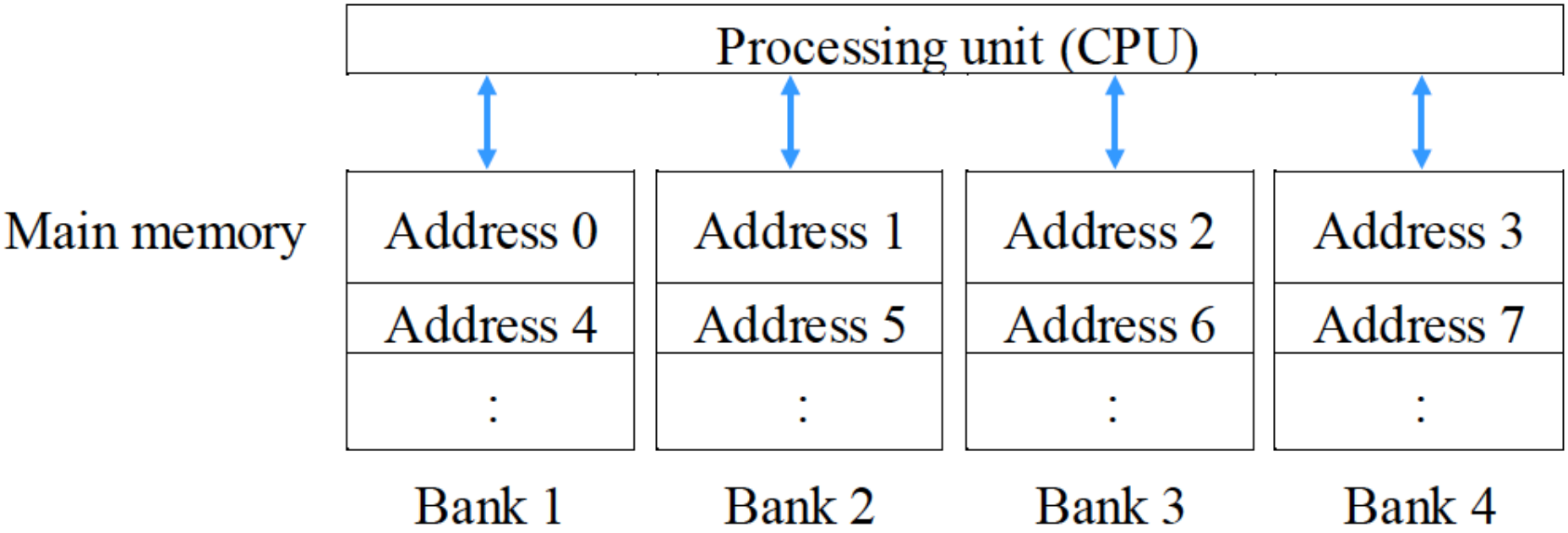
d. In order to remove factors that disrupt pipeline processing, the cache memory is divided into two segments: one for instructions and the other for data.

# Question 14: Answer Explanation: Slide I

Memory interleaving is a technique for the improvement of speed of access to main memory. Main memory is internally divided into multiple sections called banks that operate independently, and as shown in the figure below, by arranging adjacent addresses in separate banks, high speed is achieved through concurrent access.
Therefore, b) is appropriate.
Memory interleaving is a technique that has been used in general-purpose computers, but currently, it is used in some servers and PCs as well.

# Question 14: Answer Explanation: Slide II




- a) When the data to written to the cache memory by the CPU, it is also written to main memory. This method is called "write through." According to this method, the content of both the cache memory and main memory always match, but because data is also written to the main memory every time it is written to the cache memory, the processing speed during writing declines.

# Question 14: Answer Explanation: Slide III

- c) It is a description concerning the purpose of the cache memory.
- d) In the case of CPU architecture in which an instruction cannot be rewritten, if the instruction cache and data cache are separated, writing to the instruction cache is not necessary, which leads to an overall improvement in the cache efficiency. However, this is not directly connected to the method for removing the cause of pipeline processing disruption (such as inclusion of several branch instructions), and is therefore not related to memory interleaving.

# Question 15

Q15. (q2-15) Which of the following is an optical disc that uses organic dye for the recording layer of the storage media, and records data with a laser beam by burning tiny holes called pits?

a. CD-R
b. CD-RW
c. DVD-RAM
d. DVD-ROM

Q15. (q4-15) Which of the following is an optical disc that uses organic dye for the recording layer of the storage media, and records data with a laser beam by burning tiny holes called pits?
Theme: Computer Components, Category: FE

a. CD-R
b. CD-RW
c. DVD-RAM
d. DVD-ROM

# Question 15: Answer Explanation: Slide I

- An optical disc that uses organic dye as the recording layer of the storage media, and records data with a laser beam by burning tiny holes called pits is a) CD-R (CD-Recordable). CD-R is a type of CD that allows data to be written only once, and because of burning pits, once data is written, it cannot be erased.
- b) CD-RW (CD-Re-writable) is a type of CD on which data can be written and erased any number of times. Data is recorded by increasing the temperature with a laser beam, and then changing the properties (degree of reflection) of the material of the recording layer.

# Question 15: Answer Explanation: Slide II

- c), d) DVD is a storage medium that has the same 12 cm diameter as CD. The recording density is higher in comparison with CD, and depending on the type of DVD, recording on both sides or dual-layer recording is possible. DVD-RAM described in c) is a type of re-writable DVD, and DVD-ROM described in d) is a type of read-only DVD. The method of recording data on DVD-RAM is almost same as CD-RW, and on DVD-ROM, data is recorded by making tiny dents called pits in the same way as in CD-ROM.

# Question 16

Q16. (q2-16) Which of the following is an appropriate explanation of a system bus?

a. It is a standard that is used in many PCs for serial data transfer between PCs and modems or between PCs and peripheral devices.

b. It is a mechanism for transferring data between the I/O device and main memory independently of the CPU.

c. It is a digital signal transmission path that is used for backplanes and expansion slots, and is shared among multiple devices.

d. It enables connection of devices in a tree topology through a hub, and makes use of two data transfer modes: high speed and low speed.

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d. It enables connection of devices in a tree topology through a hub, and makes use of two data transfer modes: high speed and low speed.

# Question 16: Answer Explanation: Slide I

- A system bus is a common path (bus) used by the CPU to send data and control signals between main memory and an I/O controller. Therefore, c) is appropriate.
  Buses are classified with various methods, but if the buses are divided into a computer's internal buses and external buses, the system bus is an internal bus that is the same as the processor bus (connection between the components of the CPU) and memory bus (connection between the CPU and main memory). The external buses include I/O buses for connections between an I/O controller and auxiliary storage, and also for connections between I/O controllers.
- a) This is a description concerning RS-232C.
- b) This is a description concerning DMA (Direct Memory Access) and I/O channels.

# Question 16: Answer Explanation: Slide II

- d) This is a description concerning USB. The high-speed mode (480 Mbps) was added from USB2.0, and the super-speed mode (5 Gbps) was added from USB3.0.

# Question 17

Q17. (q2-17) Which of the following is an explanation of USB?

a. It is a parallel interface that is used for connection of a CD-ROM drive or a DVD drive installed in a PC.

b. It is a parallel interface used for connection of a hard disk or a printer in a daisy chain.

c. It is a serial interface that enables devices to be connected in a tree topology via a hub.

d. It is a serial interface that transfers data to a printer by using infrared rays.

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Theme: Computer Components, Category: FE

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b. It is a parallel interface used for connection of a hard disk or a printer in a daisy chain.

c. It is a serial interface that enables devices to be connected in a tree topology via a hub.

d. It is a serial interface that transfers data to a printer by using infrared rays.

# Question 17: Answer Explanation: Slide I

- USB (Universal Serial Bus) is a serial interface that enables the PC and all peripheral devices to be connected via the same connector. By using a USB interface, a maximum of 127 devices can be connected in a tree topology via a hub (this is called the cascade connection). Therefore, c) is the correct answer.
  Three types of transfer speeds, namely the low speed (1.5 Mbps), full speed (12 Mbps), and high speed (480 Mbps) are available, and the high-speed mode is supported only by USB2.0. The hot plug is supported, which enables removal and insertion of the connector while power is being supplied to the computer. The super-speed mode (5 Gbps) has been added to USB3.0, with a power supply increased from 500 mA to 900 mA.
- a) The parallel interface used for connecting the PC and the CD-ROM or DVD drive provided in the PC is ATA/ATAPI (AT Attachment/AT Attachment Packet Interface).

# Question 17: Answer Explanation: Slide II

- b) The parallel interface used for connecting the hard disk or a printer through a daisy chain is SCSI (Small Computer System Interface; pronounced "skuzzy") defined by ANSI (American National Standards Institute).
- d) The serial interface that transfers data to a printer by using infrared rays is IrDA (Infrared Data Association).

# Question 18

Q18. (q2-18) Which of the following is an appropriate characteristic of serial ATA?

a. It has bidirectional compatibility with SAS (Serial Attached SCSI).
b. It uses a daisy chain connection.
c. It has compatibility with parallel ATA in terms of cable and connector.
d. It is hot swappable.

Q18. (q2-18) Which of the following is an appropriate characteristic of serial ATA?

Theme: Computer Components, Category: FE

a. It has bidirectional compatibility with SAS (Serial Attached SCSI).
b. It uses a daisy chain connection.
c. It has compatibility with parallel ATA in terms of cable and connector.
d. It is hot swappable.

# Question 18: Answer Explanation: Slide I

- The IDE (Integrated Drive Electronics) specification, which is the industry common standard for hard disk connection interfaces in PCs, standardized by ANSI (American National Standards Institute) is referred to as the (parallel) ATA (Advanced Technology Attachment) standard. According to this standard, up to two built-in hard disks can be connected within a computer through parallel transfer. Following this, extended standards such as E-IDE (Enhanced IDE) and ATAPI (ATA Packet Interface) were defined, which have enabled the connection of CD and DVD drives besides hard disks. Serial ATA is aimed at a reduction in operating voltage, reduction in size of the connector and cable, and increase in the transfer speed by using simple serial transfer as the transfer method, and has a transfer speed of 1.5 Gbps and 3 Gbps. Furthermore, the hot swap function that enables removal and insertion of connectors while power is supplied was not supported by parallel ATA, but is supported by serial ATA.

# Question 18: Answer Explanation: Slide II

Therefore, d) is appropriate.

- a) The SAS controller has upward compatibility with serial ATA, but does not have mutual compatibility.
- b) This refers to SCSI.
- c) In comparison with parallel ATA, the cable thickness and the connector shape are very different.

# Question 19

Q19. (q2-19) Which of the following is the software that is provided for each peripheral device to serve as an interface between the OS and each peripheral device that is connected to a PC so that the application software can use such a peripheral device?

a. Installer
b. Device driver
c. Device manager
d. Formatter

Q19. (q2-19) Which of the following is the software that is provided for each peripheral device to serve as an interface between the OS and each peripheral device that is connected to a PC so that the application software can use such a peripheral device?
Theme: Computer Components, Category: FE

a. Installer
b. Device driver
c. Device manager
d. Formatter

# Question 19: Answer Explanation: Slide I

- In peripheral devices such as a printer, the details of control methods are different for each model, which makes it impossible to include the control functions of all models beforehand in the OS, and also leads to inefficiency. Therefore, rather than including the control program of the peripheral devices in the OS, a program is made available for each peripheral device as necessary. Such a program that acts as an interface between the OS and a peripheral device is called a "device driver,"
  so b) is the correct answer.
- a) This is a program that enables software to be embedded in the hard disk for use, and allows the copying of necessary files and specification of the environment settings.

# Question 19: Answer Explanation: Slide II

- c) This is a function that is embedded in the OS that manages the connection state of peripheral devices, settings of the drivers, and settings of the interrupt request signal (IRQ) from the peripheral devices.
- d) This is a program that initializes (or formats) media such as floppy disks, hard disks, and MO disks to enable them to be used.

# Question 20

Q20. (q2-20) Which of the following is a display that requires no backlight because it is self-luminous upon the application of electric voltage, and is characterized by low voltage operation and low power consumption?

a. CRT
b. PDP
c. TFT liquid crystal
d. Organic Light Emitting Diode (OLED)

Q20. (q2-20) Which of the following is a display that requires no backlight because it is self-luminous upon the application of electric voltage, and is characterized by low voltage operation and low power consumption?
Theme: Computer Components, Category: FE

a. CRT
b. PDP
c. TFT liquid crystal
d. Organic Light Emitting Diode (OLED)

# Question 20: Answer Explanation: Slide I

- The display that emits light by itself when electric voltage is applied, and satisfies all characteristics including "no backlight required," "low voltage operation," and "low power consumption" is an Organic Light Emitting Diode (Electro Luminescence), therefore, d) is the correct answer.
  The OLED display has a structure in which an organic compound that emits light in response to an electric voltage is sandwiched between glass (or plastic) substrates, and displays images when a 5 to 10 volt of direct-current voltage is applied. OLED displays are also available as thin types that have a thickness of 1.8 mm. Unlike liquid crystal displays, a backlight is not needed, which leads to a low power consumption.

# Question 20: Answer Explanation: Slide II

- a) **CRT (Cathode Ray Tube):** This refers to the brown tube in TVs. A surface is coated with a fluorescent material, and an electron beam is deflected by a magnetic field or electrode and made to hit the surface so that the fluorescent material glows. The power consumption is higher than liquid crystal.
- b) **PDP (Plasma Display Panel):** This is a display in which a gap between two glass plates is filled with gas such as helium or neon, and light is emitted by applying an electrical voltage to the gas. The display is thin, lightweight, and has a high brightness, but consumes more power than liquid crystal.

# Question 20: Answer Explanation: Slide III

- c) **TFT liquid crystal:** This is a display device in which a substance called liquid crystal, whose molecular structure changes in response to electric voltage and the degree of light transmission varies, is inserted between glass substrates. A liquid crystal in which electric voltage is applied by a thin film transistor to each bit of a pixel is called TFT (Thin Film Transistor). Since liquid crystal does not emit light by itself, it needs a backlight.

# Question 21

Q21. (q2-21) Which of the following is an appropriate explanation of a plasma display?

a. It displays images by using the light emitted from a gas discharge.

b. It does not emit light by itself, so it uses a backlight to display images.

c. It has a structure in which an organic compound is sandwiched between electrodes, and displays images through the use of the light emitted when electricity is passed through this structure.

d. An electron beam is discharged from an electron gun, and light is emitted when the beam hits the fluorescent material on the surface of the tube to display characters and images.

Q21. (q2-21) Which of the following is an appropriate explanation of a plasma display?

Theme: Computer Components, Category: FE

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b. It does not emit light by itself, so it uses a backlight to display images.

c. It has a structure in which an organic compound is sandwiched between electrodes, and displays images through the use of the light emitted when electricity is passed through this structure.

d. An electron beam is discharged from an electron gun, and light is emitted when the beam hits the fluorescent material on the surface of the tube to display characters and images.

# Question 21: Answer Explanation: Slide I

- A plasma display is a display in which a gap between two thin glass plates is filled with neon gas or xenon gas, and an electrical discharge is produced by applying a high voltage to the gas. Ultra violet rays that are generated by this electrical discharge then hit the red, green, and blue (RGB; three primary colors of light) fluorescent material on the surface of the glass and light is emitted. Therefore, the description in a) is appropriate. At present, the power consumption is not high, and in some cases the power consumption is actually reduced by the addition of the backlight used in liquid crystal displays.
- b) This is a description concerning liquid crystal displays such as a TFT (Thin Film Transistor). Since the display itself does not emit light, a backlight is installed at the back or side of the display as a light source.

# Question 21: Answer Explanation: Slide II

- c) This is a description concerning an OLED (Electro-Luminescence) display. An OLED has a structure in which a thin film of an organic substance is sandwiched between electrodes, and this structure has been put into practical use in some places. Unlike a liquid crystal display such as a TFT, a light source is not needed, so the structure can be slimmed down so far as to become a film.
- d) This is a description concerning the brown tube (CRT; Cathode Ray Tube).

# Question 22

Q22. (q2-22) A hard disk has a rotation speed of 5,000 rpm, and an average seek time of 20 milliseconds. The memory capacity per track of the hard disk is 15,000 bytes. What is the average access time, in milliseconds, that is necessary for transferring one block when one block has 4,000 bytes of data?

a. 27.6
b. 29.2
c. 33.6
d. 35.2

Q22. (q2-22) A hard disk has a rotation speed of 5,000 rpm, and an average seek time of 20 milliseconds. The memory capacity per track of the hard disk is 15,000 bytes. What is the average access time, in milliseconds, that is necessary for transferring one block when one block has 4,000 bytes of data?

Theme: Computer Components, Category: FE

a. 27.6
b. 29.2
c. 33.6
d. 35.2

# Question 22: Answer Explanation: Slide I

The average access time of a hard disk can be calculated with the following formula:

**Average access time = Average seek time + Average rotational latency + Data transfer time**

The average seek time is 20 milliseconds.

The average rotational latency is the time required for half (1/2) rotation.

The rotation speed of the disk is 5,000 rpm, that is, 5,000 rotations in one minute (60 seconds).

Time required for one rotation = 60 ÷ 5,000 (seconds)

= 0.012 seconds

= 12 milliseconds

Average rotational latency = 12 milliseconds ÷ 2 = 6 milliseconds

15,000 bytes of storage capacity of one track is transferred in 12 milliseconds, which is the time for one rotation, and therefore, the data transfer speed per millisecond will be as follows: 15,000 ÷ 12

# Question 22: Answer Explanation: Slide II

(bytes/millisecond) = 1,250 (bytes/millisecond). And since one block is 4,000 bytes, the data transfer time will be as follows:
Data transfer time = 4,000 (bytes) ÷ 1,250 (bytes/milliseconds) = 3.2 (milliseconds).
Based on the above, the average access time is 20 + 6 + 3.2 = 29.2 milliseconds.
Therefore, b) is the correct answer

# Question 23

Q23. (q2-23) In a system, one block is composed of 8 sectors and a sector comprises 500 bytes. The system manages files by allocating file area in units of blocks. When files with a size of 2,000 bytes and 9,000 bytes are saved, what is the total number of sectors that is allocated to these two files? Here, sectors occupied by management information such as directories are ignored in the calculation.?

a. 22
b. 26
c. 28
d. 32

Q23. (q2-23) In a system, one block is composed of 8 sectors and a sector comprises 500 bytes. The system manages files by allocating file area in units of blocks. When files with a size of 2,000 bytes and 9,000 bytes are saved, what is the total number of sectors that is allocated to these two files? Here, sectors occupied by management information such as directories are ignored in the calculation.?

Theme: Computer Components, Category: FE

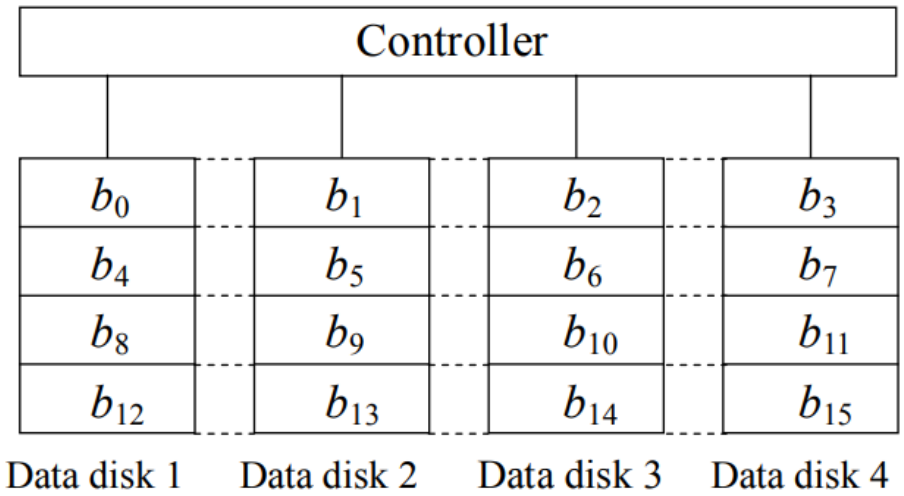
a. 22
b. 26
c. 28
d. 32

# Question 23: Answer Explanation: Slide I

Since one block is composed of 8 sectors, the memory capacity per block is 500 bytes $\times$ 8 sectors/block = 4,000 bytes/block.
Since file area is allocated in units of blocks, 2,000 bytes $\div$ 4,000 bytes/block = 0.5 (rounded up to 1), to indicate that 1 block is used to store a file of 2,000 bytes. Also, 9,000 bytes $\div$ 4,000 bytes/block = 2.25, which is rounded up to 3, to indicate that 3 blocks are necessary to store a file of 9,000 bytes.
Therefore, a total of 4 blocks are allocated, and the necessary number of sectors is 4 blocks $\times$ 8 sectors/block = 32 sectors.
Therefore, d) is the correct answer.

# Question 24

Q24. (q2-24) Which of the following is the mechanism of segmenting and storing data on multiple hard disks, as shown in the figure below? Here, $b_0$ to $b_{15}$ indicate the order in which each bit of data is stored in the data disk.




a. Striping
b. Disk cache
c. Blocking
d. Mirroring

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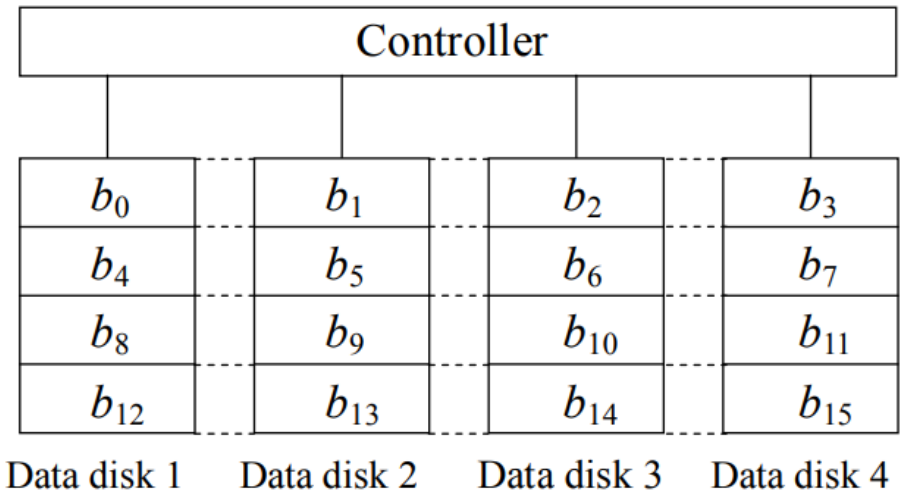


Theme: Computer Components, Category: FE

a. Striping
b. Disk cache
c. Blocking
d. Mirroring

# Question 24: Answer Explanation: Slide I

- **Striping** refers to the distribution and recording of data of a constant size and the recording it on multiple hard disks so that data is read and written in parallel. In RAID (Redundant Array of Inexpensive Disks), striping corresponds to RAID0. Therefore, a) is the correct answer.
- b) **Disk cache:** This is a device or function that increases the speed of data exchange between a CPU and disk. The data that is transferred as a block from the hard disk can be stored in the cache to increase the speed of reading.
- c) **Blocking:** The logical unit of data for I/O is called a block, and collecting several records as blocks is called blocking. For sequential access, processing efficiency can be improved in comparison with cases where data is read record-by-record.

# Question 24: Answer Explanation: Slide II

- d) **Mirroring:** This is a method by which exactly the same data is written to multiple hard disks, and even if a failure occurs in one disk, the data processing is not affected. Mirroring corresponds to RAID1.

# Question 25

Q25. (2021 A FE AM-q10) Which of the following is an appropriate description of XML?

a. An exclusive editor is required to produce XML documents.
b. It is an integration of the logical structure and document style.
c. It is based on HTML and offers more extended functions.
d. The attributes and logical structure of a document can be defined with user-defined tags.

Q25. (2021 A FE AM-q10) Which of the following is an appropriate description of XML?

a. An exclusive editor is required to produce XML documents.
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# Question 26

Q26. (2021 A FE AM-q11) Which of the following is an appropriate term for a special register that contains the address of the next instruction to be fetched?

a. Accumulator
b. Instruction register
c. Program counter
d. Status register

Q26. (2021 A FE AM-q11) Which of the following is an appropriate term for a special register that contains the address of the next instruction to be fetched?

Theme: Computer Components, Category: FE

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# Question 27

Q27. (2021 A FE AM-q13) Which of the following is a computer architecture where each instruction is divided into multiple stages (e.g., fetch, decode, and execute) in the processor and multiple functional units execute two or more instructions in parallel by slightly shifting execution stages of the instructions?

a. Multicore
b. Pipeline
c. RISC
d. VLIW

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Theme: Computer Components, Category: FE

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# Question 28

Q28. (2021 S FE AM-q12) Which of the following is the performance of a CPU in MIPS when the instruction mix of the CPU is as listed in the table below? Here, the CPU does not use a pipeline architecture.

| Instruction type | Instruction execution time in μs | Appearance ratio |
|---|---|---|
| Register to register operation | 0.1 | 40% |
| Register from memory operation | 0.3 | 50% |
| Unconditional branch operation | 0.6 | 10% |

a. 0.04
b. 0.25
c. 4
d. 25

Q28. (2021 S FE AM-q12) Which of the following is the performance of a CPU in MIPS when the instruction mix of the CPU is as listed in the table below? Here, the CPU does not use a pipeline architecture.

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Theme: Computer Components, Category: FE

a. 0.04
b. 0.25
c. 4
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# Question 29

Q29. (2021 S FE AM-q13) Which of the following is a computer system or architecture where the CPU sequentially reads and executes the programs that are stored in the main memory?

a. Addressing system
b. DMA control architecture
c. Stored program architecture
d. Virtual memory system

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Theme: Computer Components, Category: FE

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b. DMA control architecture
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d. Virtual memory system

# Question 30

Q30. (2020 S FE AM-q10) Which of the following is classified as an internal interrupt?

a. An interrupt due to an abnormal power condition, such as a momentary loss of the commercial power supply
b. An interrupt due to having performed division by zero
c. An interrupt due to the completion of input or output
d. An interrupt due to the occurrence of a memory parity error

Q30. (2020 S FE AM-q10) Which of the following is classified as an internal interrupt?

Theme: Computer Components, Category: FE

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d. An interrupt due to the occurrence of a memory parity error

# Question 31

Q31. (2020 S FE AM-q11) Which of the following is an appropriate characteristic of SRAM compared with DRAM?

a. Compared with DRAM, SRAM consumes more power while it is idle.
b. Compared with DRAM, SRAM needs a fewer number of transistors to store one bit of data.
c. SRAM does not need to be refreshed periodically as flips flops retain data, and DRAM needs to be refreshed at fixed intervals to retain data.
d. SRAM stores data in a combination of capacitors and transistors, and DRAM stores data in a set of transistors called flip-flops.

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# Any Questions?

# References

 IT Fundamentals (New FE Textbook Vol. 1)