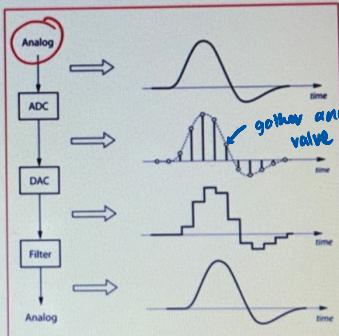


# Lecture (12/13)

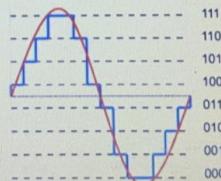
Which of the following procedure is carried out when digitizing an analog signal?

- A. Sample the voltage level of the analog wave form at fixed time interval. ①
- B. Limit the voltage range of the analog waveform to +/- 5V
- C. Match the voltage level of the analog waveform to the closest level available in the digital domain. — quantisation ②
- D. Reduce the analog waveform voltage level to a range used by the digital domain

Forcefully reducing the analog voltage level will distort the analog waveform, hence it is not carried out when digitizing the analog signal.



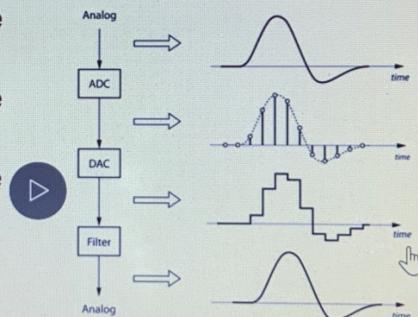
get the analog value of this signal & quantise it to a level to conform to ADC



- ⇒ More ADC bits, more accurate signal
- ⇒ Analog signal is digital signal with infinite sampling rate

What is the minimum sampling rate required in order for a digital signal to be able to represent the analog equivalent adequately?

- A. 1X the frequency of the analog signal
- B. 2X the frequency of the analog signal
- C. 3X the frequency of the analog signal
- D. As fast as the system can support



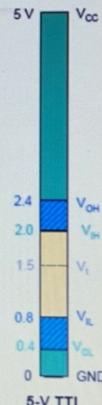
Nyquist Theorem

⇒ 2x the base frequency, based  
on Nyquist Theorem

⇒ e.g. if analog signal is 1 K hertz,  
need max 2K sampling rate  
in order to replicate /  
sample signal properly

## Which conditions are needed in order for the input device (Din) to sense the logic of the output device(Dout) correctly?

- A.  $V(OH)$  of Dout >  $V(IH)$  of Din,  
 $V(OL)$  of Dout >  $V(IL)$  of Din
- B.  $V(OH)$  of Dout <  $V(IH)$  of Din,  
 $V(OL)$  of Dout <  $V(IL)$  of Din
- C.  $V(OH)$  of Dout <  $V(IH)$  of Din,  
 $V(OL)$  of Dout >  $V(IL)$  of Din
- D.  $V(OH)$  of Dout >  $V(IH)$  of Din, 0 ALWAYS  
 $V(OL)$  of Dout <  $V(IL)$  of Din 0 of IC



VOH => device's min output voltage level if it is outputting a logic '1'  
 VIH => the min voltage level at its input pin in order of the device to consider the signal as a Logic '1'.



will  
 have some  
 resistance;  
 causing voltage drop



ground will have some  
 noise that affect transmission

		A			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>OH</sub>	High-level output current			-0.4	mA

PARAMETER	TEST CONDITIONS‡	B			UNIT
		MIN	TYP§	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -0.4 mA	2.4	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA		0.2	0.4	V

Is the electrical signal level of device B's output compatible with device A's input?

↓ transmitter

↓ look at "0" side of it

- ✓ A. Yes
- B. No

$$V_{OA} \text{ of } B > V_{OH} \text{ of } A$$

⇒ compatible

B's min VOH is larger than A's min VIH value.  
 ⇒ Logic '1' can be detected correctly.  
 B's max VOL is lower than A's max VIL.  
 ⇒ Logic '0' can be detected correctly.

Which of the following scenario(s) will increase the skew between a set of well-behaved signals?

- ✓ A. Applying additional serpentine/trombone routing to the PCB traces.
- ✓ B. Have different PCB trace width but keep the length constant.
- C. Preserving the PCB trace length and width for each signal in the data bus.
- ✓ D. Loading some of the data lines within the same data bus with capacitors.

means signals arrive at receiver at the same time

→ charge resistance

time constant  
affect

$$t = RC$$

affect propagation delay

Look at scenarios where there is a change  
in propagation delay

for signal skew:



affect resistance  
of line &  
parasitic capacitors  
and inductance (L)

Well behave implies the signal propagation delay in the system has been tweaked so that there are no signal skew among signals that has some dependency, e.g. individual data bit lines in a data bus.

So any change in parameters that may alter the propagation delay will increase the signal skew.

## Which of the following scenario will result in the most crosstalk?

- A. 8 PCB traces running side by side to each other transmitting 1Mhz signal, with **ground** plane in the PCB layer below.
- B. 8 PCB traces running **side by side** to each other transmitting **10Mhz** signal.
- C. 8 PCB traces running side by side to each other transmitting 1Mhz signal.
- D. 8 **shielded cables** running side by side to each other transmitting 1Mhz signal

high frequency  
help to reduce amt of noise  
→ reduce crosstalk

- Crosstalk increases as signal frequency increases,
- interference (crosstalk) on neighbouring signal increases when the lines are close together and when the number of closely packed line increases (more interference sources).

restrict amt of  
EM wave wire  
can radiate out  
→  
reduce crosstalk

## Which of the following is False?

- A. Parallel bus implementation leads to more bulky cabling compared to Serial Bus.
- B. Parallel Bus is more affected by signal skew and cross talk because of concentration of multiple signals in close vicinity.
- C. Signal Skew and Cross Talk affects the quality of signal transmission, putting a limit on the minimum bus clocking speed. ~~(X)~~ ✓ *should be maximum*
- D. Parallel Bus interface design tend to be simpler as it only needs a strobe signal.

- Signal Skew and Cross Talk will limit the max bus clocking frequency because the effect of Cross talk increases when data signal frequency (proportional to clock speed) increases.
- Increase in frequency also result in a smaller allowed margin of error (tolerance ) before any signal skew results in wrong data being latched,
- which means the probability of wrong data latched increases as data signal frequency increases.

↳ for serial , more complex

↳ parallel by nature ↳

conversion logic  
added complexity

Which factor(s) below will cause a change in propagation delay?

- ✓ A. Presence of capacitors and inductors in the signal line
- ✓ B. PCB trace width
- ✓ C. PCB trace length
- ✓ D. Bad soldering of components/wires to PCB, thus increasing the resistance of the signal path.

$$t = RL$$

$\Rightarrow$  affected propagation delay

- Bad soldering will introduce more parasitic resistance into the system due to poorer electrical connection.
- Changing PCB width/length will change the overall impedance (resistance, capacitance and inductance) of the system.

## Which of the following is False?

serial bus less affected by signal skew, cross talk

- A. All things equal, Serial Bus can achieve a higher clocking rate compared to Parallel Bus.
- B. Given the same clock rate, Serial bus is able to transfer data further and faster.
- C. Serial bus is less affected by signal skew compared to Parallel bus.
- D. Serial bus implementation is less bulky compared to Parallel bus.

- With the same clock rate, Serial Bus suffers less Cross Talk compared to Parallel bus which has more lines (more interference sources).
- As are less signal skew (only between the data bit and its clock) compared to parallel bus with multiple data lines.
- But Serial bus at same clock rate will have slower data transfer rate compared to the Parallel Bus since it could only transfer one bit each clock.

(c)

parallel :



signal skew:  
lines depended on  
each other com?  
in at the same time

Serial :



\ interdepend  
signals

## What is true for synchronous and asynchronous serial transfer?

- A. Synchronous transfer uses a common clock line to synchronize data transfer between transmitter and receiver.
- B. Asynchronous transfer does not need any form of synchronization at all to transfer the data.
- C. Asynchronous transfer requires transmitter and receiver to have a prefix transfer clock frequency on a common clock line.
- D. Synchronous transfer does not need a common clock between the transmitter and receiver.

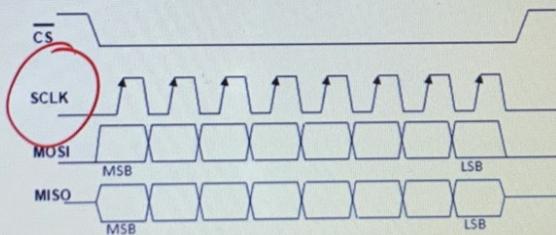
Anych transfer still needs some form of synchronisation in order for transmission to be reliable, just that they transfer these synch info via the data line.



(B) Any form of transmission will require some synchronization  
⇒ embed synchronization material in Matlab

## Which of the following serial bus(es) are synchronous in nature?

- A. UART
- B. SPI
- C. USB
- D. RS232



Which of the following UART control/data bit(s) has a LOGIC LOW?

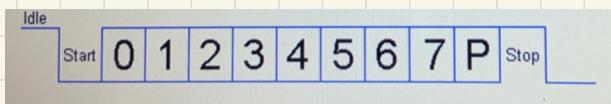
- ✓ A. Data '0'
- B. STOP Bit
- ✓ C. START Bit
- D. IDLE State

3 states in UART that has fixed logic.

⇒ IDLE → '1'

⇒ Start → '0'

⇒ Stop → '1'



Based on chat

- Advantage to asynch over synch  $\rightarrow$  less lines
- common clk signal is a kind of sync information  
(NOT the other way)
- Synchronous go out of sync less often than  
asynch ones  $\Rightarrow$  Transmitter & receiver has  
different clk.

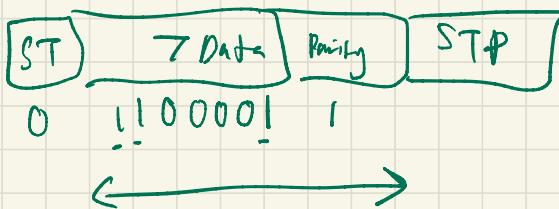
What is the value of the Parity bit if the number of '1's in the data packet is even? Assume Even Parity Scheme is used.

- ✓ A. 0  
B. 1

e.g Configuration cost:

Start bit  
always 1 bit for  
VR  
transmit(?)

Data	Even Parity	Stop bit (S1P)
↑ ↑		



$p=1$  to make it  
have even number of ones

## What is parity bit used for?



- A. Error Correction
- B. Error Prediction
- C. Error Detection
- D. Error Detection and Correction

- The parity scheme in UART can only detect that there are some issues with the transmission.
- It is not able to identify exactly which bit is wrong, that means it also cannot perform error correction.

e.g. original : 1 0 0 1 1 0 1 0

But something happens during transmission and a bit gets flipped

New : 1 0 0 1 1 0 0 0

receiver receives this and counts, realized only 3 ones, know something is wrong but

don't know exactly what

Which of the following UART control/data bit(s) is represented by a +15V signal when transmitted via PC COM port using RS232 transmission standard?

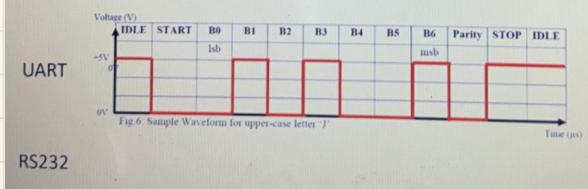
- A. DATA '1'
- B. STOP
- C. IDLE State
- D. START

Logic '0'  $\rightarrow$  +15 V

Logic '1'  $\rightarrow$  -15 V

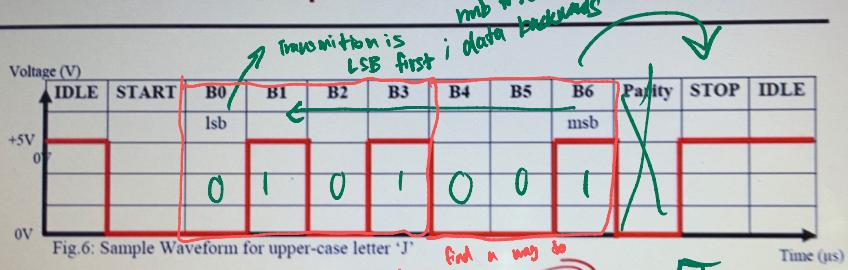
only one with  
logic 0

- RS232 standard uses the UART protocol transmission, i.e. START bit has a Logic '0', STOP bit has a Logic '1' and IDLE has a Logic '1'.
- But it uses an electrical standard interface that employ a 'negative logic', i.e. Logic '1' is represented by a voltage smaller than that of Logic '0'.
- E.g. Logic '1' can be equal to -15V while Logic '0' can be equal to +15V.



Will see in lab:

## UART Tx Example



- Figure 6 above correspond to the configuration 701 (7 Data, 1 STOP and Odd parity).
- Capital Letter 'J' => Ascii value = 0x4A *as above read backwards*
- 0x4A => 100 1010 (binary)
- Presented in LSB first => 0101 001
- IDLE=1, START=0, STOP=1.
- Parity bit logic depends on number of 1's in Data Field and the Parity Scheme (Odd or Even) used.

e.g. 7 0 1 , 7 E 1 , 7 N 1  
↑ ↑ ↑  
Data Parity Stop  
No parity

⇒ if no parity, parity field will disappear

\* LSB tends to have 4 bits

MSB gets remaining

⇒ Parity bit transmitted by transmitter

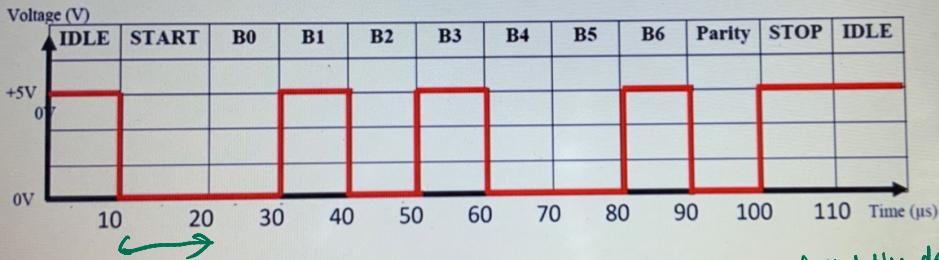
# UART Rx Example

800000

→ every bit  
example twice  
including start, stop, parity

Tx baud rate =  $1/(10 \text{ us}) = 100000 \text{ bps}$ . Configuration = 701.

$$T = \frac{1}{\text{Baud}} = 10 \mu\text{s}$$



- RX Data = 1001010b
- RX Data = 0011000b ?
- Information Sampled @ 200000 bps:  
 $\underbrace{00001100}_{S} \underbrace{110000}_{P} \underbrace{1100}_{S} \underbrace{11}_{P}$  → instead of 4 bits, 20 bits

initially decoded  
using whatever  
configuration  
(701 in this case)

- complication comes when transmitter baud rate is different from receiver baud rate
- baud rate used by transmitter to decide how fast they should transmit each bit of information
- used by receiver to determine how fast they should sample information
- for Cost : treat it as the receiver will receive all the data regardless if parity error, etc.