EE314 Experiment 3 Parallel Adders, Subtractors and Complementors

Nail Tosun - 2094563
Electric and Electronic Engineering Departmant, METU

2018
March

2)

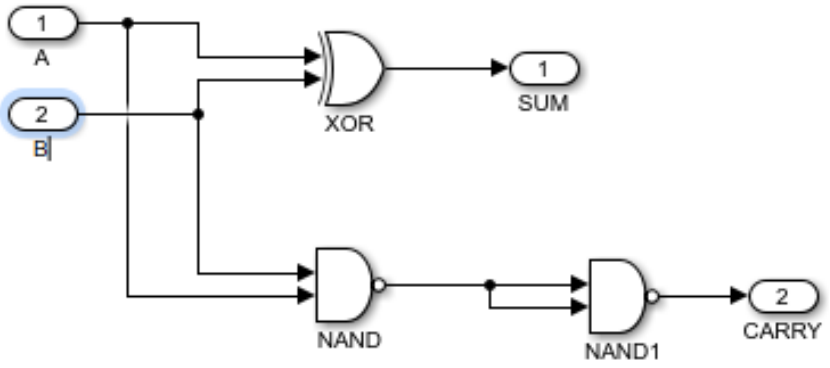

Figure 1: Half-adder circuit using NAND and XOR gates

Table 1: Truth table of half adder

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

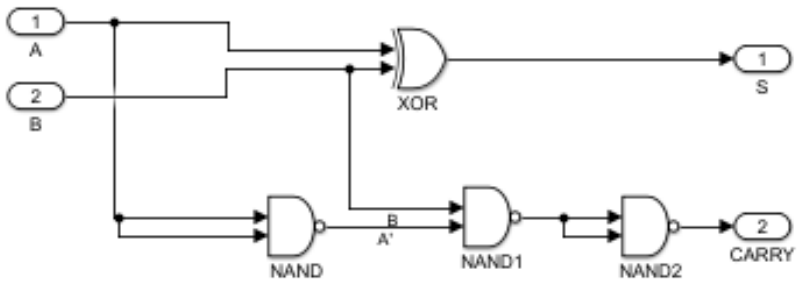

Figure 2: Half-subtractor consists of NAND and XOR

Table 2: Truth table of half subtractor

A	B	CARRY	S
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

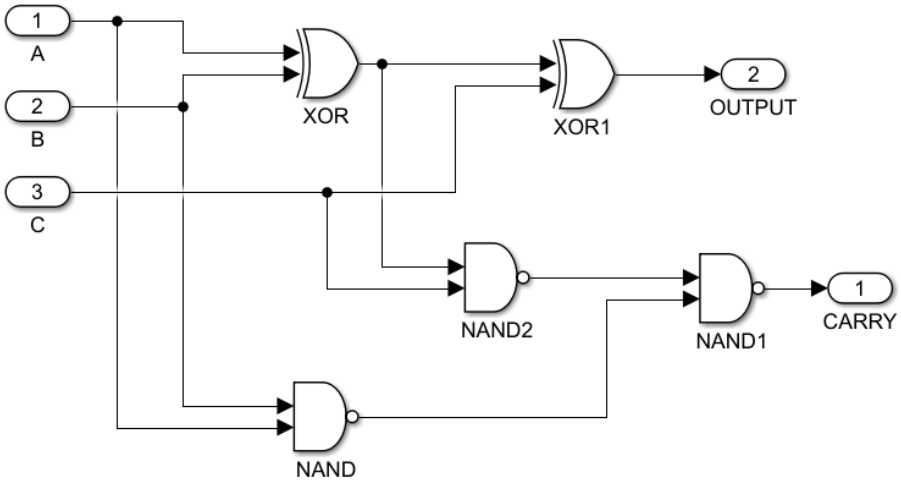

Figure 3: Full-adder circuit using NAND and XOR gates

Table 3: Full-adder truth table

A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

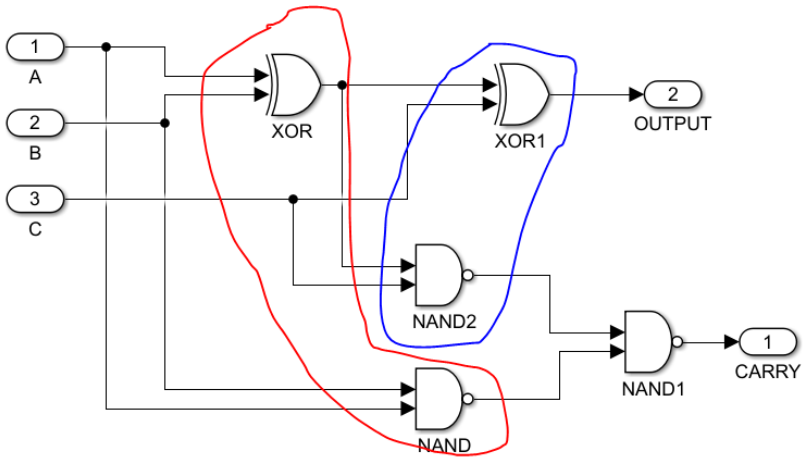

Figure 4: Full adder consists of two half adder

4)

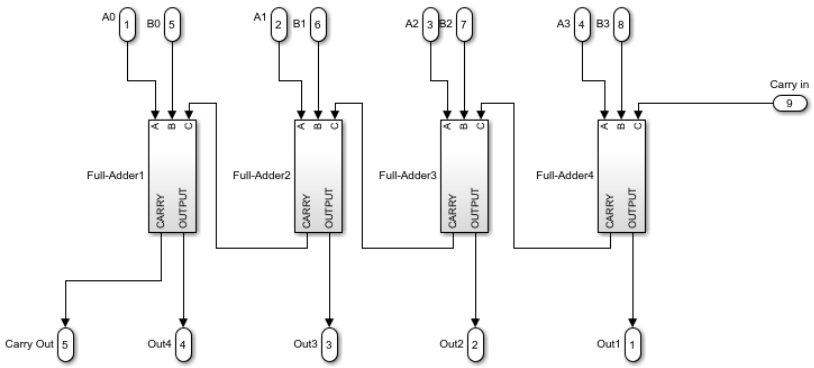

Figure 5: Four bit adder using full adders using Simulink (I)

6)

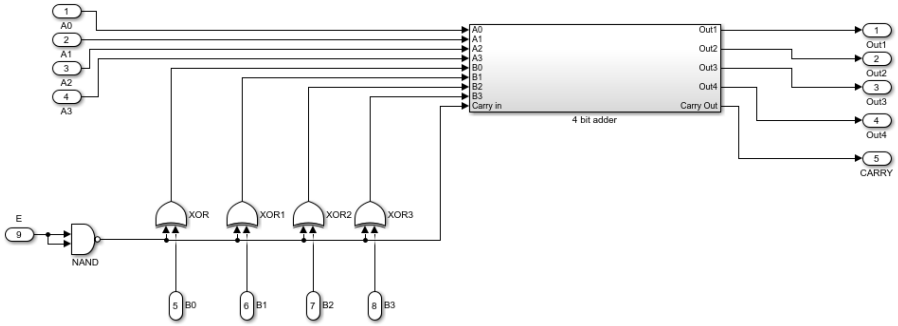

Figure 6: Four bit adder and substractor using 2's complement technique with enable pin using Simulink (I)

7)

References and Notes: (I) If figure is not clear original document can found by following URL.

8)

Table 4: Truth table

E	X	Y	OUT	CARRY
1	0110	0011	1001	0
1	0111	0001	1000	0
0	0110	0001	0101	0
0	0011	0100	1111	0
1	1010	0111	0001	1
1	1011	invalid	invalid	invalid
0	1001	0110	0011	1
0	1111	invalid	invalid	invalid

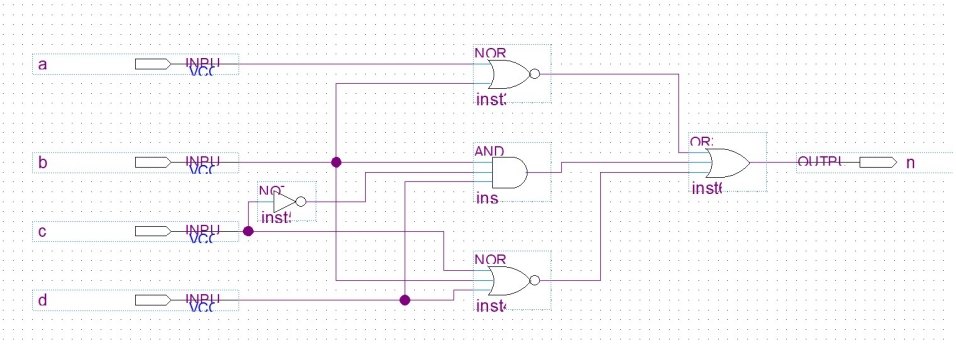

Figure 7:

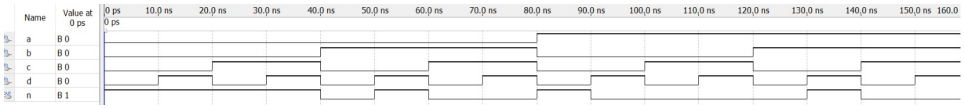

Figure 8:

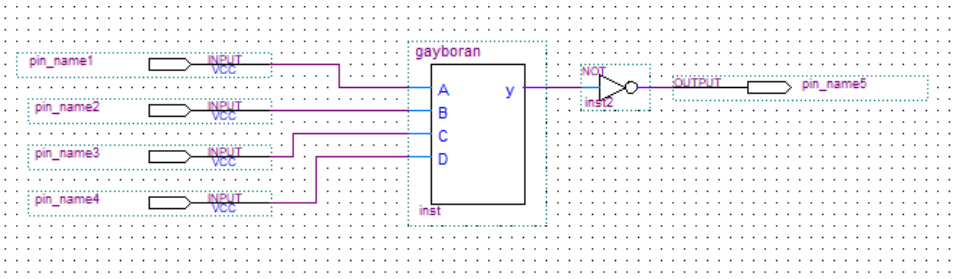

Figure 9:

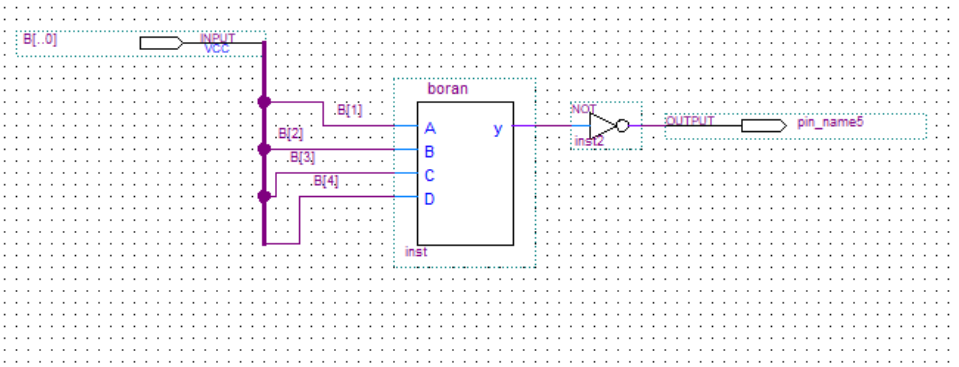

Figure 10:

Since i have problem with Quartus simulation results didn't work.