

EE312 Take-Home Exam 3

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1)

Saturation only enhancement load

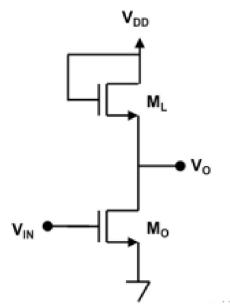


Figure 1: Saturation only enhancement load

Output high calculation

Since M_L is always in saturation;

$$V_{DS} > V_{GS} - V_{TN} \quad V_D = V_G$$

$$I_{DS} = K_L \left(\frac{V_{GS} - V_{TN}}{2} \right)^2 = 0$$

$$V_{GS} = V_{TN} \quad V_G = V_{DD}$$

$$V_S = V_{OUT} = V_{DD} - V_{TN} = 5 - 0.8 = 4.2 \text{ V}$$

Input low calculation

After M_O open since both transistor in saturation region;

$$I_{DS} = \frac{K_O(V_{in} - V_{TH})^2}{2} = \frac{K_L(V_{DD} - V_{out} - V_{TH})^2}{2}$$

by mean before M_L goes into linear region V_{out} is linearly change with V_{in} . Therefore we have to choose conservative input low voltage;

$$V_{IL} = V_{TH} = 0.8 \text{ V}$$

Output low calculation

To find output low voltage first assume after some point M_L is go into linear region since V_{DS} is sufficiently dropped. Keep in mind M_L is always in saturation region.

$$I_{DS} = \frac{K_O(V_{DD} - V_{TH} - V_{out})^2}{2} = K_N(V_{in} - V_{TH})(V_{out}) - \frac{K_N V_{out}^2}{2}$$

$$V_{in} = 4.2 \text{ V}$$

Put $V_{in} = 4.2 \text{ V}$ and solve for V_{out}

$$V_{OL} = 1.12 \text{ V}$$

Input high calculation

To find input high calculation we should find $\frac{dV_{out}}{V_{in}} = -1$ point.

$$I_{DS} = \frac{K_O(V_{DD} - V_{TH} - V_{out})^2}{2} = K_N(V_{in} - V_{TH})(V_{out}) - \frac{K_N V_{out}^2}{2}$$

Taking derivative both side with $\frac{d}{dV_{in}}$;

Critical Voltage

The voltage with when M_0 goes into linear region.

$$V_{DS} = V_{GS} - V_{TN}$$

$$V_{out} = V_{in} - 0.8 \quad (1)$$

$$I_{DS} = \frac{K_O(V_{GS} - V_{TN})^2}{2} = \frac{K_N(V_{DD} - V_{TH} - V_{out})^2}{2}$$

$$\sqrt{\frac{3}{2}}(V_{in} - 0.8) = 4.2 - V_{out} \quad (2)$$

Putting (1) and (2) together;

$$V_{in} = 2.69V$$

$$V_{critical} = 1.89V$$

Voltage Transfer Characteristic

Resistive loaded NMOS

First ($V_{in} = 0$) NMOS is in cut-off region. When V_{in} pass the threshold voltage it is go into saturation region since large V_{DS} then eventually it goes into linear region.

Input low voltage

$$I_{DS} = \frac{K_N(V_{GS} - V_{TH})^2}{2} = \frac{V_{DD} - V_{out}}{R_L}$$

To be able to find input low voltage we should look at $\frac{dV_{out}}{dV_{in}} = -1$;

$$\frac{(V_{in} - 0.8)^2}{2} = \frac{5 - V_{out}}{K_N R_L}$$

$$V_{in} - 0.8 = -0.44 \frac{dV_{out}}{dV_{in}}$$

$$V_{IL} = 1.24 V$$

Output high voltage

Since NMOS is in cut-off when input low and output high $V_{OH} = 5 V$

Input high voltage

Since both expression for current is true;

$$(V_{in} - V_{TN})V_{out} - \frac{V_{out}^2}{2} = \frac{V_{DD} - V_{out}}{R_L K_n} \quad (3)$$

Taking derivative of both side with $\frac{d}{dV_{in}}$;

$$2V_{out} - V_{in} + 0.8 = 0.44 \quad (4)$$

Putting (3) and (4) in same equation and solve for V_{in} ;

$$V_{IH} = 2.78 \text{ V}$$

Output low voltage

$$\begin{aligned} I_{DS} &= K_N((V_{GS} - V_{TN})V_{out} - \frac{V_{out}^2}{2}) \\ I_{DS} &= K_N(4.2V_{out} - \frac{V_{out}^2}{2}) = \frac{5 - V_{out}}{R_L} \\ (4.2V_{out} - \frac{V_{out}^2}{2}) &= \frac{5 - V_{out}}{K_N R_L} \\ (4.2V_{out} - \frac{V_{out}^2}{2}) &= 0.44(5 - V_{out}) \end{aligned}$$

Solving quadratic equation;

$$V_{OL} = 0.50 \text{ V}$$

Depletion mode NMOS load

Firstly, when $V_{in} = 0V$ M_O is cut-off and M_D is in linear region since there is no I_{DS} current.

Input low voltage

$$\begin{aligned} I_{DS} &= \frac{K_O(V_{GS} - V_{TH})^2}{2} = K_D((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}) \\ I_{DS} &= \frac{K_O(V_{in} - 0.8)^2}{2} = K_D((-V_{TH})(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})^2}{2}) \end{aligned}$$

Taking derivative two side with $\frac{d}{V_{in}}$

$$V_{in} - 0.8 = -0.8 \frac{dV_{out}}{dV_{in}} + \frac{dV_{out}(5 - V_{out})}{dV_{in}}$$

Then putting $\frac{dV_{out}}{dV_{in}} = -1$

$$V_{out} = 3.4 + V_{in}$$

Putting above equation into current equation and solve for V_{in}

$$V_{in} = 1.37 V$$

Input high voltage

Then M_D is in saturation region whereas M_O linear region

$$\begin{aligned} I_{DS} &= \frac{K_D(V_{GS} - V_{TH})^2}{2} = K_O((V_{in} - 0.8)V_{DS} - \frac{V_{DS}^2}{2}) \\ 0.32 &= (V_{in} - 0.8)V_{DS} - \frac{V_{DS}^2}{2} \\ 0.32 &= (V_{in} - 0.8)V_{out} - \frac{V_{out}^2}{2} \end{aligned}$$

Taking derivative two side with $\frac{d}{V_{in}}$

$$V_{in} - 0.8 = 2V_{out}$$

Putting above equation into current equation and solve for V_{in}

$$V_{IH} = 1.72 V$$

Output low voltage

To find V_{out} we should give input as 5V to the input high case current equation(where M_D is in saturation region M_O linear region).

$$V_{OL} = 0.08 V$$

Output high voltage

Since we used depletion mode NMOS transistor in pull-up network (V_{TNj0})
 $V_{out} = V_{DD} = 5 V$

Conclusion

Voltage Swings

Only with depletion load NMOS inverter we can achieve rail-to-rail operation. With saturation only load NMOS inverter since up transistor in saturation region $V_{GS} > V_{TN}$ (with positive threshold voltages) $V_S = V_{out}$ always less than V_{DD} . Moreover with resistive NMOS inverter although we have V_{DD} at output high still we have nonzero output low and we have significant static power consumption. If we order voltage swings numerically;

$$VS_{depletion} > VS_{resistive} > VS_{saturation-only}$$

Noise Margins

Depletion NMOS load case:

$$NMH = V_{OH} - V_{IH} = 3.28 \text{ V}$$

$$NML = V_{IL} - V_{OL} = 1.29 \text{ V}$$

Saturated-only NMOS load case:

$$NMH = V_{OH} - V_{IH} = 1.42 \text{ V}$$

$$NML = V_{IL} - V_{OL} = -0.32$$

Since V_{IL} can't be smaller than output low voltage this inverter don't work properly.

Resistive only NMOS load case:

$$NMH = V_{OH} - V_{IH} = 2.21 \text{ V}$$

$$NML = V_{IL} - V_{OL} = 0.31 \text{ V}$$

2)

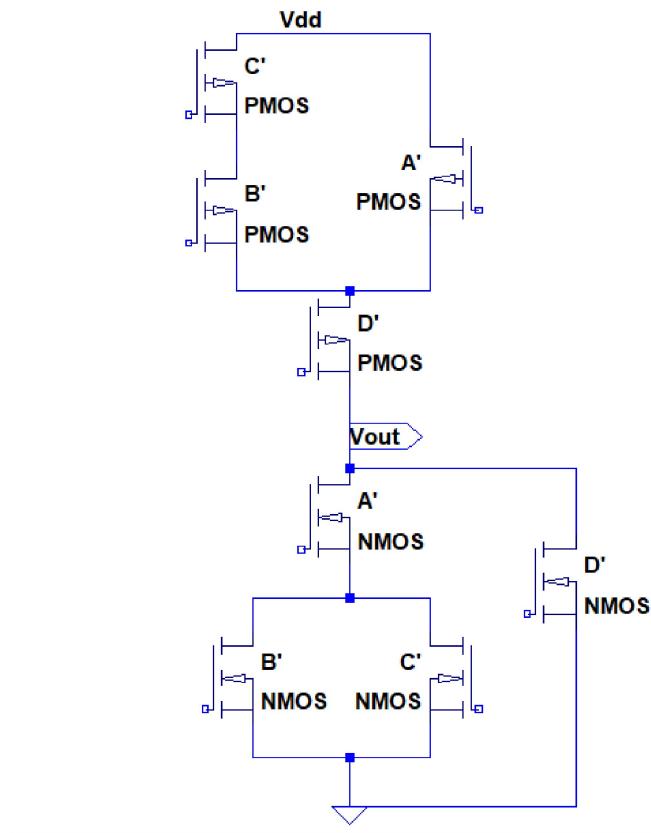


Figure 2: CMOS design

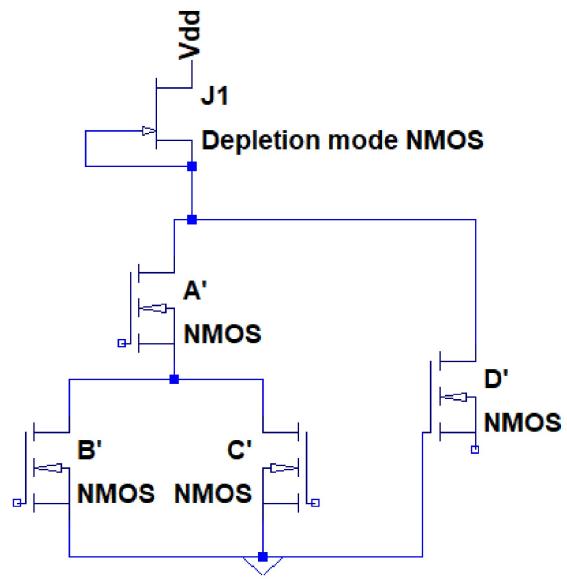


Figure 3: NMOS depletion loaded design