

EE314 Experiment 5 Flip-Flops and Sequential Circuits

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1)

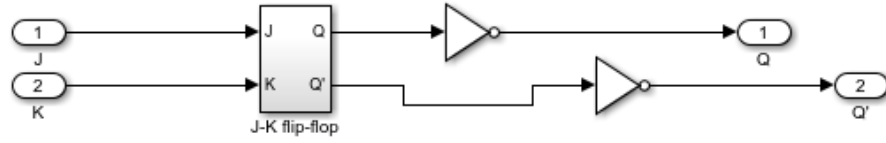


Figure 1: Logic design for Question 1

2)

$$\begin{aligned}
 Q_{1n} &= JQ'_{1n-1} + K'Q_{1n-1} \\
 J &= Q'_{3n-1}Q'_{2n-1} \quad K = Q_{3n-1}Q_{2n-1} \\
 K' &= Q'_{3n-1} + Q'_{2n-1} \\
 Q_{1n} &= Q'_{3n-1}Q'_{2n-1}Q'_{1n-1} + (Q'_{3n-1} + Q'_{2n-1})Q_{1n-1} \\
 Q_{2n} &= JQ'_{2n-1} + K'Q_{2n-1} \\
 J &= Q_{1n} \quad K' = Q_{1n} \\
 Q_{2n} &= Q_{1n}Q'_{2n-1} + Q_{1n}Q_{2n-1} \\
 Q_{2n} &= 2Q_{3n-1}Q'_{2n-1}Q'_{1n-1} + Q'_{2n-1}Q_{1n-1} + Q_{2n-1}Q_{1n-1}Q'_{3n-1} \\
 Q_{3n} &= JQ_{3n-1} + KQ'_{3n-1} \\
 J &= Q_{2n} \quad K = Q_{2n} \\
 Q_{3n} &= 2Q_{3n-1}Q'_{2n-1}Q'_{1n-1} + Q_{3n-1}Q'_{2n-1}Q_{1n-1}
 \end{aligned}$$

3)

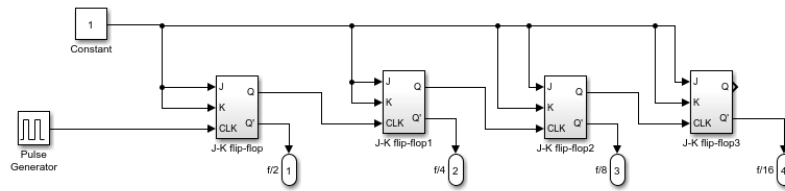


Figure 2: Frequency Converter Logic Design

4)

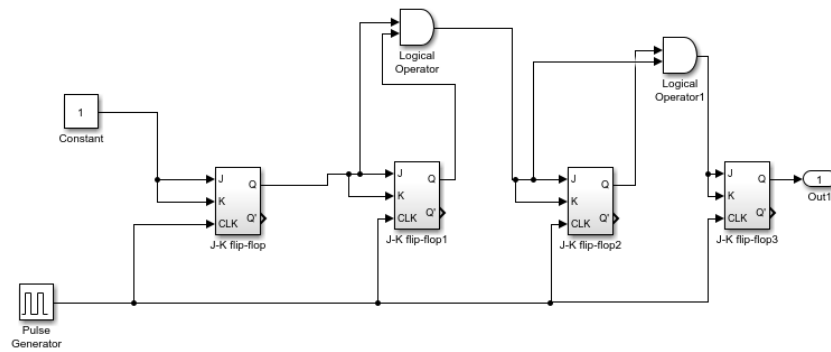


Figure 3: Ripple Up Counter

5)



Figure 5: Verilog Code

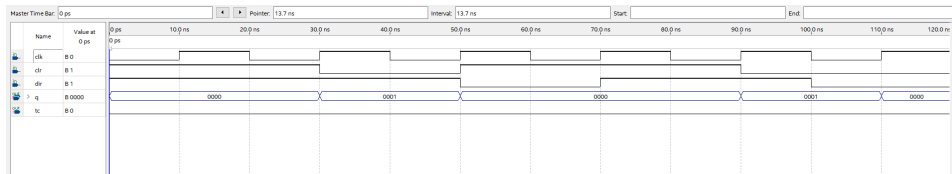


Figure 6: BCD counter Simulation results