EE314 Experiment 5 Flip-Flops and Sequential Circuits

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1)

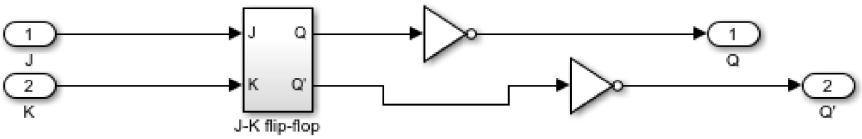

Figure 1: Logic design for Question 1

2)

$$Q_{1n} = JQ'_{1n-1} + K'Q_{1n-1}$$

$$J = Q'_{3n-1}Q'_{2n-1} \quad K = Q_{3n-1}Q_{2n-1}$$

$$K' = Q'_{3n-1} + Q'_{2n-1}$$

$$Q_{1n} = Q'_{3n-1}Q'_{2n-1}Q'_{1n-1} + (Q'_{3n-1} + Q'_{2n-1})Q_{1n-1}$$

$$Q_{2n} = JQ'_{2n-1} + K'Q_{2n-1}$$

$$J = Q_{1n} \quad K' = Q_{1n}$$

$$Q_{2n} = Q_{1n}Q'_{2n-1} + Q_{1n}Q_{2n-1}$$

$$Q_{2n} = 2Q_{3n-1}Q'_{2n-1}Q'_{1n-1} + Q'_{2n-1}Q_{1n-1} + Q_{2n-1}Q_{1n-1}Q'_{3n-1}$$

$$Q_{3n} = JQ_{3n-1} + KQ'_{3n-1}$$

$$J = Q_{2n} \quad K = Q_{2n}$$

$$Q_{3n} = 2Q_{3n-1}Q'_{2n-1}Q'_{1n-1} + Q_{3n-1}Q'_{2n-1}Q_{1n-1}$$

3)

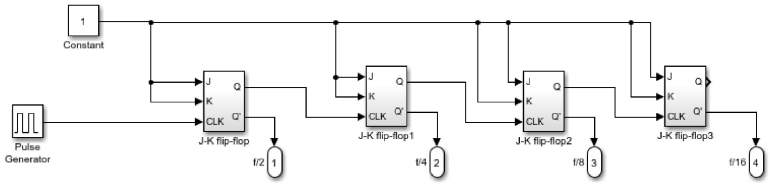

Figure 2: Frequency Converter Logic Design

4)

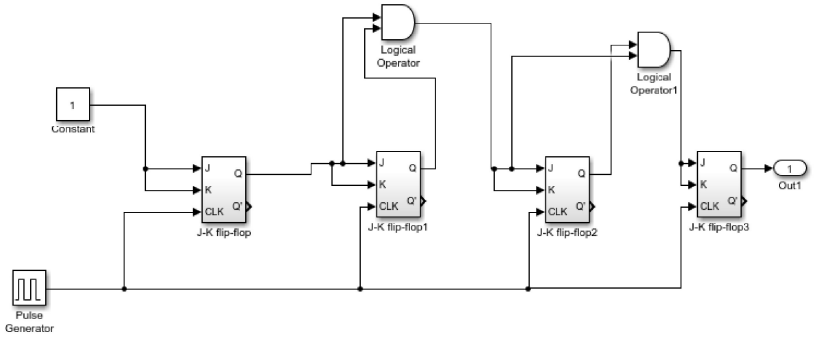

Figure 3: Ripple Up Counter

5)

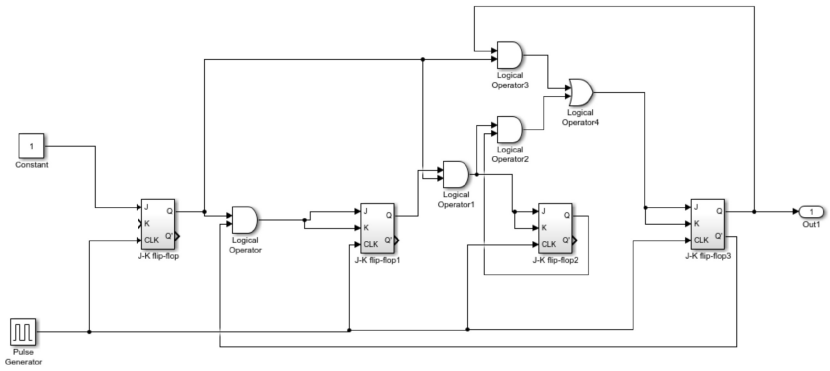

Figure 4: BCD counter

6)

```
module counter(clr,clk,dir, tc, q);

input clr,clk,dir;
output reg tc;
output reg[3:0] q;
always@(posedge clk,posedge clr)
begin
if(clr==1)
q=4'd0;
else
begin
if (dir==1)
q=q+1;
else if(dir==0)
q=q-1;
if(dir==1 & q==4'd10)
begin
q=4'd0;tc=1'b1;
end
else if(dir==0 & q==4'd15)
begin
q=1'd9;tc=1'b1;
end
else tc=1'b0;
end
end
endmodule
```

Figure 5: Verilog Code

Figure 6: BCD counter Simulation results