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Realization of digital Oscilloscope with FPGA for education

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Abstract

In this study, it is aimed to implement a digital oscilloscope by FPGA architectures to correspond the requirements of laboratories in the educational institutions in an economic way. It is shown that non-professional oscilloscopes can be implemented with low-cost, educational purposed FPGAs. It is also able to measure high frequency signal by high speed FPGAs. Terasic DE0 kit is used as hardware and Quartus II is used as software in this application. The sine signal which is a widely known signal used to measure is generated by the signal generator. The graphical view of the sampled signal in the FPGA is shown on a 640x480 pixelated VGA monitor.

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1. Introduction and Purpose

The aim of the realization of digital oscilloscope with FPGA (Field Programmable Gate Arrays) structures is to get a digital oscilloscope in an economic way. The principal reason of this phenomenon is the extraordinary evolution of the Digital Electronics [1]. Every time the manufacturers of Digital chips manage to realize smaller chips, with major number of transistors, capable of working every time to more speed and to minor cost. The basic functioning of the digital oscilloscope we can see it in the Figure 1. It has an ADC (Analog to Digital Converter) for conditioning signal. The ADC is in charge of sampling the signal and of the quantification of this value.

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This part of the oscilloscope is especially critical, since depending on the sampling rate and the precision level of the converter (levels of quantification), it will define the principal characteristics of the oscilloscope [5]. Once sampled the values are stored in a digital memory for later processing and visualization. The Digital oscilloscope, by the advantage of the digital logic, can realize complex calculations on the information stored in the memory. This one is a great advantage of the digital oscilloscopes opposite to the analogical ones the Major Productivity. The design is simpler and rapid on our chip that the design with devices of different manufacturers and with characteristics that surely are not exactly the wished ones[6].

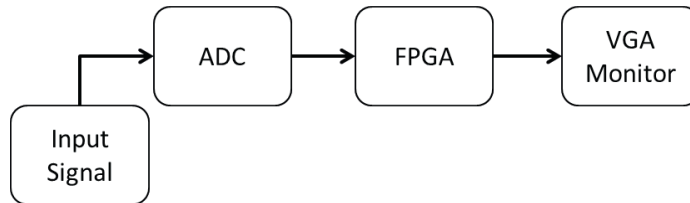


Figure.1: Schematic digital oscilloscope

2. Altera DE0 Board

The Altera DE0 board is a well-known kit of Terasic Technologies and it is shown in Figure 2. It depicts the layout of the board and indicates the location of the connectors and key components. The DE0 board has many features that allow the user to implement a wide range of designed circuits, from simple circuits to various multimedia projects. To provide the maximum flexibility for the user, all connections are made through the Cyclone III FPGA device. Thus, the user can configure the FPGA to implement any system design [3].

The concept of the DE0 Control Panel is illustrated in Figure 3. The "Control Codes" that perform the control functions is implemented in the FPGA board. It communicates with the Control Panel window, which is active on the host computer, via the USB Blaster link. The graphical interface is used to issue commands to the control codes. It handles all requests and performs data transfers between the computer and the DE0 board [3].

The DE0 Control Panel can be used to light up the LEDs, change the values displayed on 7-segment, monitor buttons/switches status, read/write the SDRAM and Flash Memory, read data from a PS/2 keyboard, output color pattern to LCD monitor via VGA connector, and read SD-CARD specification information. The feature of reading/writing a word or an entire file from/to the Flash Memory allows the user to develop multimedia application (Flash Picture Viewer) without worrying about how to build a Memory Programmer [3].

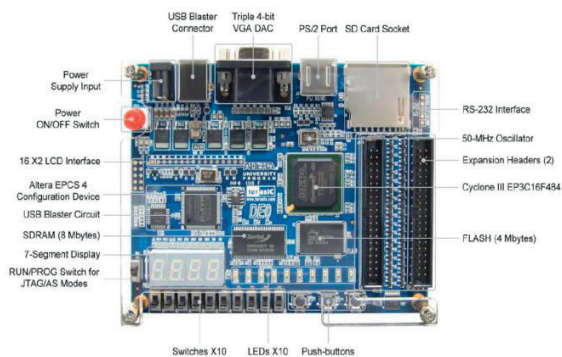


Figure.2: DE0 Kit

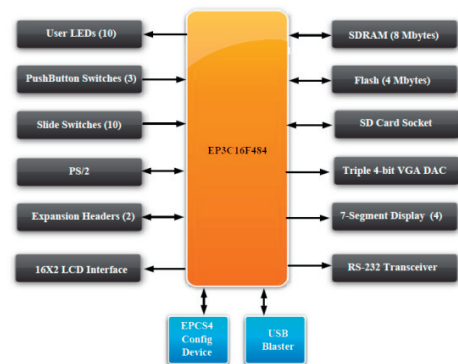


Figure.3: DE0 Block diagram

3. FPGA and VHDL

Modern field-programmable gate arrays (FPGAs) contain hundreds of thousands of lookup tables (LUTs), hundreds of embedded memories, and hundreds of multipliers connected through a programmable interconnect fabric. Obviously it is intractable to program the FPGA at the granularity of these individual elements. However, with modern synthesis and layout tools, it is possible to describe a design simply by writing logical expressions, a level higher than gates, and letting the tools do the rest [2].

Register transfer level (RTL) design is a popular discipline for describing these logical expressions. It allows the designer to express the design by describing the logic between each pair of register stages. This allows her to carefully control register-to-register logic depth while freeing her from selecting the actual gates and their mapping to the FPGA. Very High-Speed Integrated Circuit Hardware Description Language (VHDL) is one popular programming language that supports RTL hardware descriptions [4].

VHDL enjoys widespread popularity among designers in the industry, along with its close cousin, Verilog. Indeed, almost all modern CAD tools that perform simulation, synthesis, and layout support both. Verilog differs from VHDL primarily in the syntax it uses (VHDL is derived from Ada; Verilog, from C), but both languages are IEEE standards and are periodically reviewed to reflect changing industry realities and expectations.

4. Digital Oscilloscope with FPGA

An oscilloscope is an instrument of visualization of signals as seismic, beatings of the heart, electromagnetic waves etc. when it has been provided with a suitable transducer. The measurements that an oscilloscope has to do have to be very precise and it is here where the system of acquisition has been generated by a memory of double port synthesized and optimized by Altera DE0 for its FPGAs. The FPGA is programmed to measure the digital a module that manages the reading and writing of the same one. The writing fulfills consecutively from the address 0 up to 640 when the control of the trigger indicates it to us. This does that for our VGA it is so simple to read all the information that it contains whenever we draw one of 480 vertical lines that has the screen.

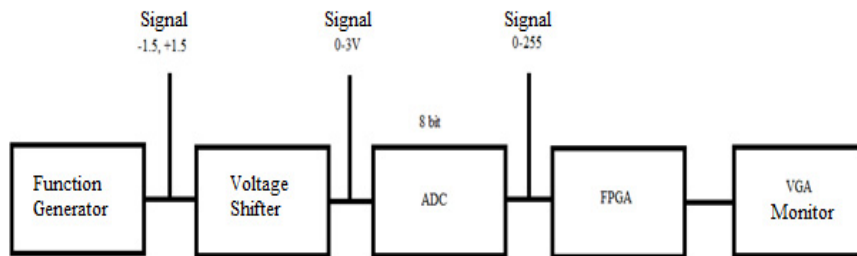


Figure.4: The Block diagram of the system

The oscilloscope module is the part of the system which deals with the analog signal and converts it in to a digital form that is then stored in to a memory [7]. In the project, the reference voltage of ADC is 3.3 V. So, the maximum voltage that measures is 3.3 V. The values that bigger than the reference voltage must be converted by transformer or divided by resistance. For testing in the project it is used a function generator and adjusted its values as below.

Signal type	: Sine wave
Amplitude	: 1.5 Volt
Frequency	: 50 Hz

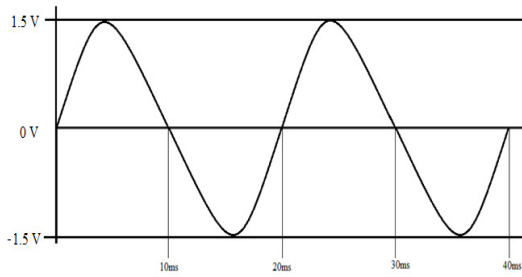


Figure.5: Sine wave

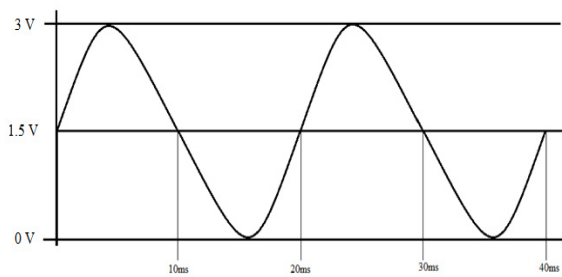


Figure.6: Shifted Sine wave

The sine wave has a negative and a positive pole in one cycle. So the maximum value is +1,5 V and the minimum value is -1.5 V. To measure both negative and positive values a DC signal adder is designed and the sine wave scope is altered from (-1.5 V, +1.5 V) to (0 V, +3 V) values. The new sine wave can be seen in the Figure 6. [8].

In the Figure 7 the non-inverting adder circuit can be seen. In the circuit, if the $R_a=R_b$ and $R_f=R_i$ then the output voltage will be $V_{out}=V_a+V_b$

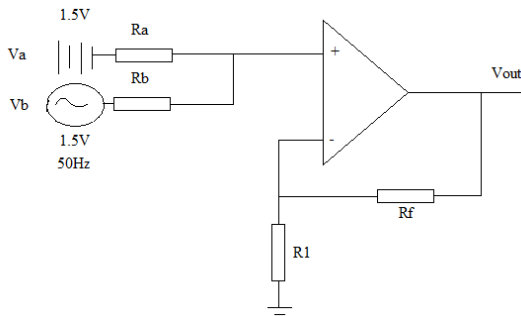


Figure.7: Non-inverting voltage adder

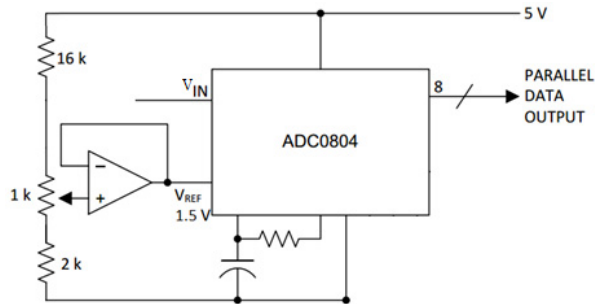


Figure.8: ADC0804

The output of the voltage adder circuit is connected to the ADC's input and the ADC converts this analog value to the digital value. The ADC has a resolution of 8 bits and converts the 0-3 V to the digital state of 0-255. According to the design -1.5 V corresponds to 0 and +1.5 V corresponds to 255.

The measured voltage can be calculated by the formula of

$$V = (\text{ADC_Output_Value} * 3 / 256) - 1,5$$

The VGA monitor with the resolution of 640x480 screens the image of obtained sinusoidal wave. Number of pixels on horizontal axis is 640 and number of pixels on vertical axis is 480. According to the design every horizontal pixel represents 1 msec and also every vertical pixel represents 10 mV [8].

The VGA monitor connector on the ALTERA DE0 board consists of five signals, RED(4 bits), GREEN(4 bits), BLUE(4 bits), HORIZ_SYNC, and VERT_SYNC. The timing relationships among this signal are shown in Figures 9 and 10. The generation of signals needed for the raster on the VGA monitor begins with dividing the frequency of the 50 MHz clock on the ALTERA DE0 board down to a 25 MHz pixel clock which is further divided down to the horizontal and vertical sync frequencies [9].

This means your design will contain a horizontal counter and a vertical counter. The horizontal and vertical sync

pulses of appropriate lengths are then produced from the two counters. A video display consists of 640 pixels in the horizontal direction and 480 lines of pixels in the vertical direction. The monitor starts each refresh cycle by updating the pixel in the top left-hand corner of the screen, which can be treated as the origin (0,0) of an X-Y plane. After the first pixel is refreshed, the monitor refreshes the remaining pixels in the row. When the monitor receives a pulse on the **HORIZ_SYNC** pin, it refreshes the next row of pixels. The time required for the sweep, the horizontal sweep period, is nominally 31.77 μs [9].

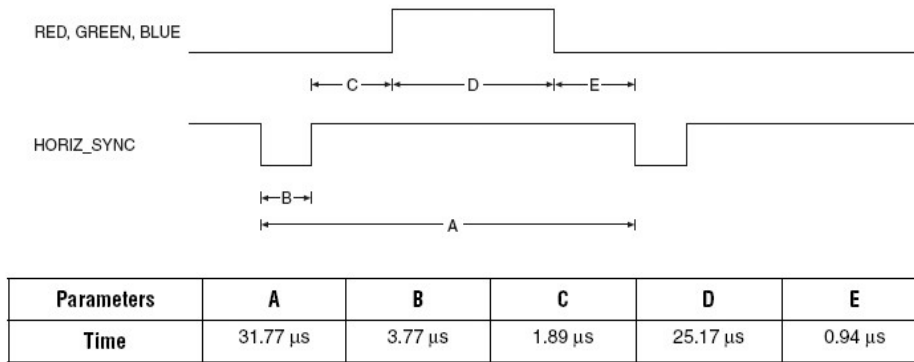


Figure.9: Horizontal Refresh Cycle.

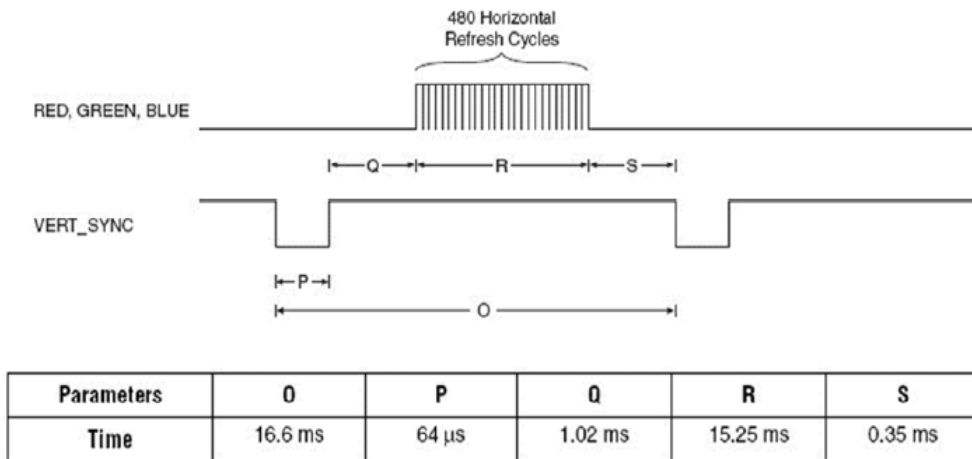


Figure.10: Vertical Refresh Cycle.

This process is repeated until the monitor reaches the bottom of the screen. When the monitor reaches the bottom of the screen, a 64 μs pulse applied to the **VERT_SYNC** pin, causing the monitor to begin refreshing pixels at the top of the screen (i.e., at [0,0]). As shown in Figure 8, the **VERT_SYNC** pulse must be repeated every 16.6 ms (vertical sweep period). A complete screen of information is being traced by the electron beam every 16.6 ms for a frame rate of 60 Hz [9].

In this context, we use the non-inverted voltage bus, ADC, DE0 Kit and VGA 640x480 monitor the process of implementation through the elements we have reflected on the screen. The sinusoidal waveform obtained through the following image we have achieved is shown in Figure 11 [8].

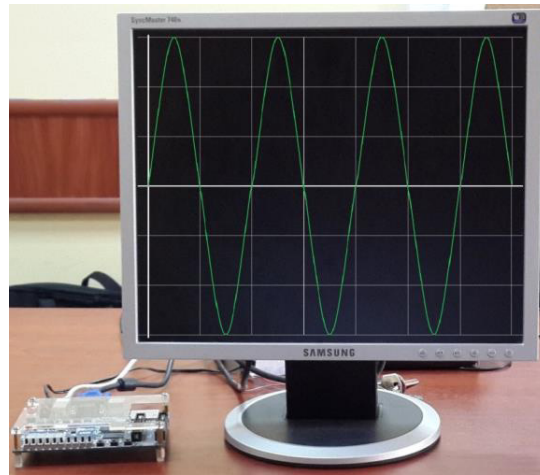


Figure.11: VGA 640x480 output sine wave

Above on the screen that is reflected, in the range of 3V that means between +1.5V and -1.5V, non-inverting voltage integrator term is used to acquiring a sinusoidal wave on the screen. In the view on the screen that is showed are the main dots of sinusoidal wave's (view on the screen that is reflected is between +150pix and -150pix). During the process of FPGA DE0, the function is on the basis of pixel and every detail of view that is the reflected on the screen is calculated over pixels. It is impossible to see by pixel's this view on the screen because FPGA's are functioning very fast and this is the reason why the view is not reflected clearly on the screen [8].

Conclusion

In this project is worked by FPGA DE0 kit to verify the quantitative oscilloscope. The kits (or materials) that are used for purpose of educating and for non-professional to perform the oscilloscopes are quite low costed. During this project work, there was a signal of sine wave that was attained from generator. An improving kit that we have ADC has no module. Therefore the module was connected from the outside by the ADC. The sine (sinus) wave include both positive and negative pole. Because of this reason by inverting and shifting term, the exit of functional generator is shifted to the positive pole. The exit of the ADC is connected to the DE0 kit and is written by VHDL.

Then the code that was written is synthesized and loaded to the FPGA and the enter signal of DE0 that is connected to the VGA's port, is watched on the monitor.

In the project, even the sine signal is tested as the input signal, it is arranged for all the signal terms to be readable. Moreover, all these readable values are saved in memory module where exist in the DE0's kit (or material) memory card. Therefore, all values are backed up.

Instead of using external ADC module, it can be used new version kits of internal ADC modules. By this way, not just low frequency signals but also on high frequency signals can be followed.

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