ON-BOARD COMMUNICATION

- Digital Communication
- Digital Data Bus System
- ARINC-429
- MIL-STD-1553
- Commercial Standard Digital Bus
- Fiber Optic Communication

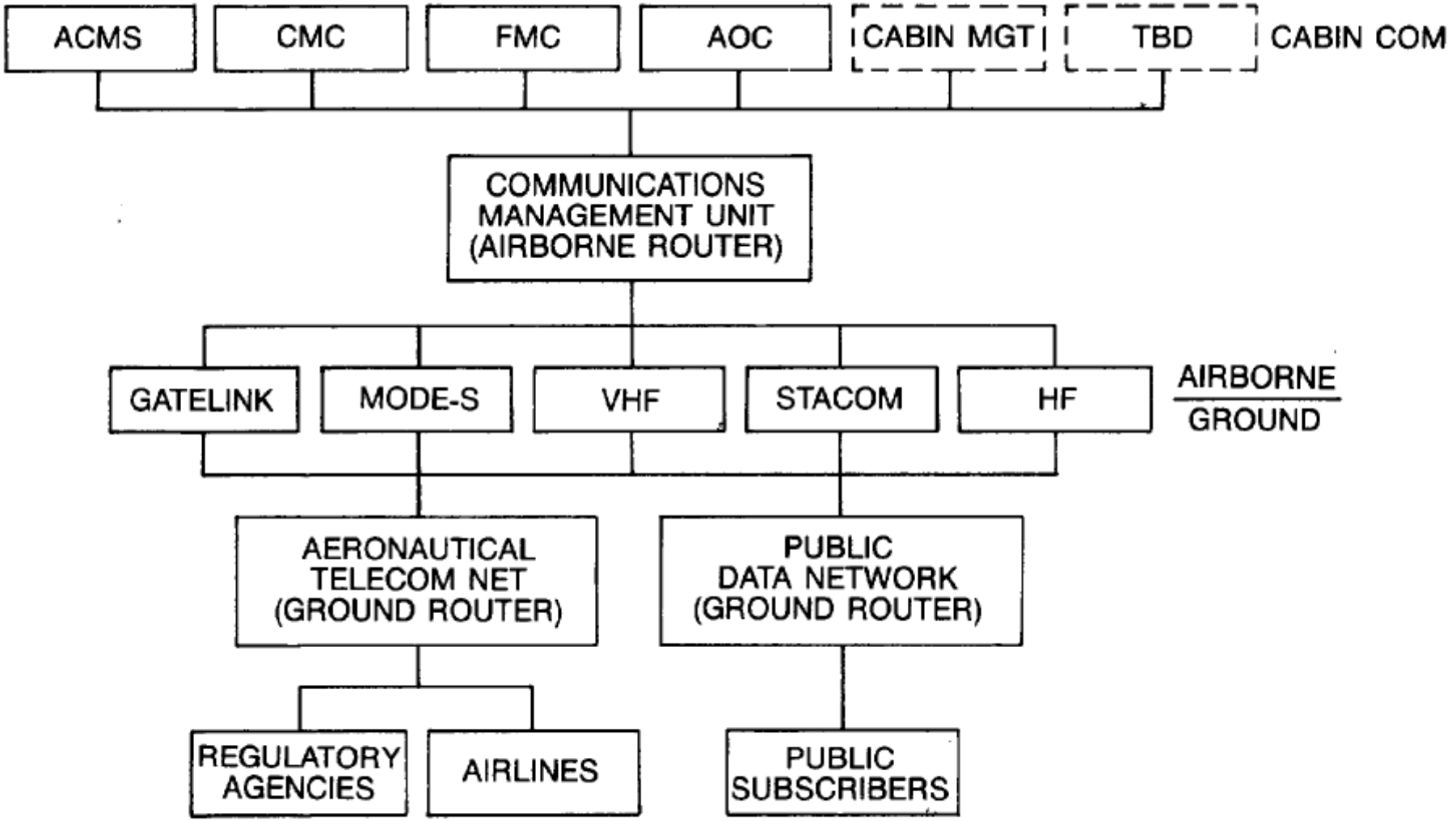
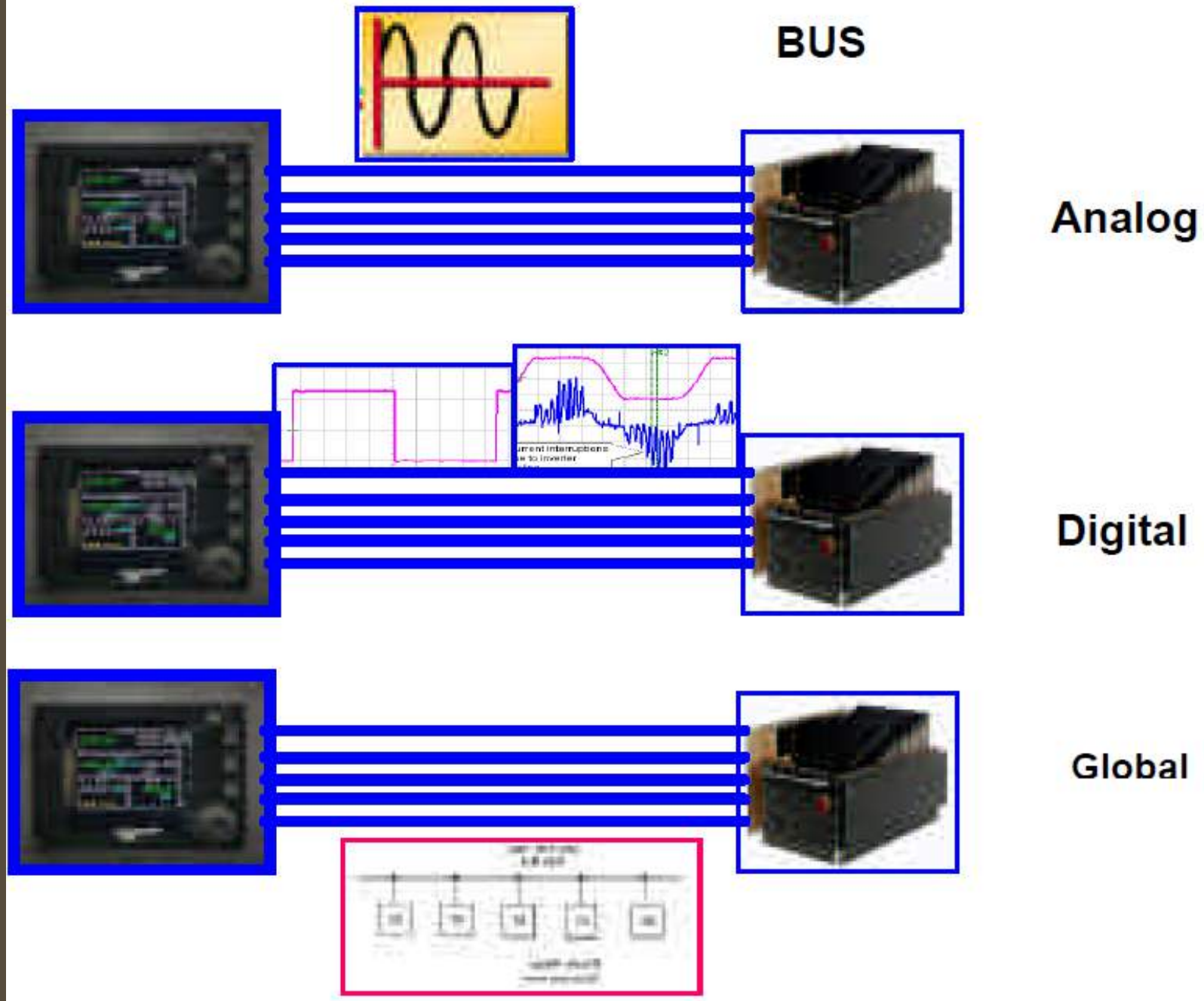
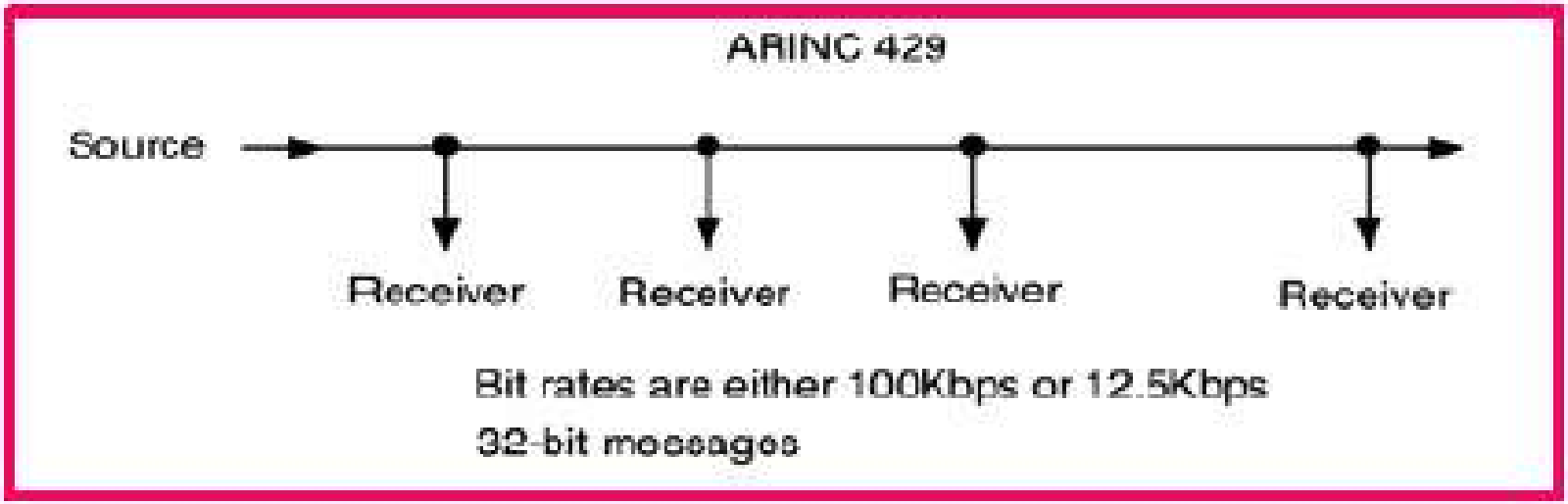


Figure 1. Aeronautical Data Communications System Integration.


BUS
Analog
Digital
Global

Communication Data Bus



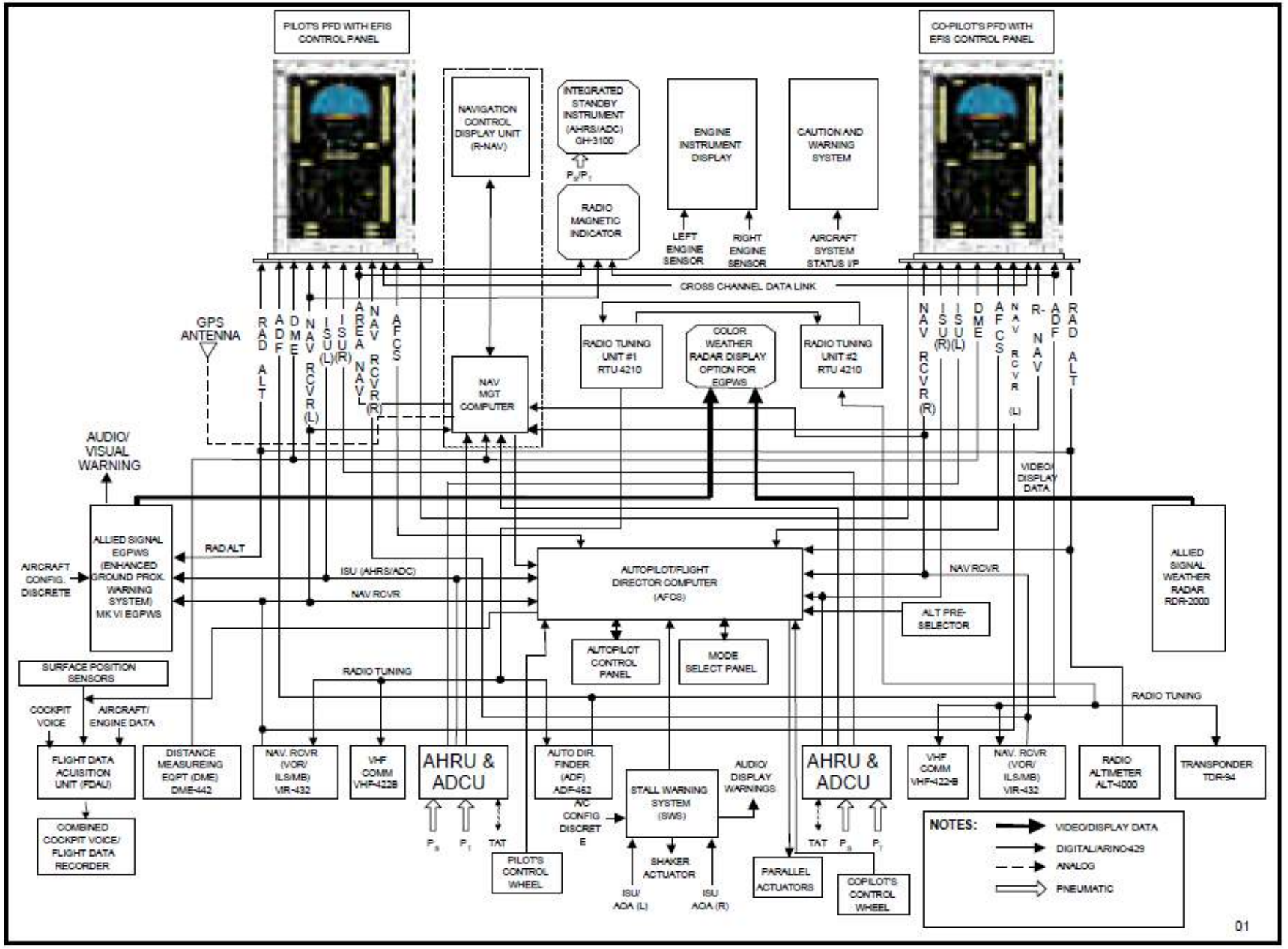


Fig. 1 SARAS Avionics Architecture

DIGITAL DATA BUS SYSTEM

- ARINC 429
- MIL-STD-1553

Digital Data Bus System

Data Bus

Data bus architectures use 16, 32 or 64 bit data paths. Wider bus structures allow significant increases in data transfer rates.

1. **MIL-STD-1553 -**The current 1553B data bus is widely used in military applications. It is a 16-bit architecture with a nominal throughput of 1 Mb/s. Many existing military avionics systems are compatible with the 1553, but most new commercial systems are not. New commercial and some military applications use the VME or PCI bus architectures, or proprietary solutions. Mil-Std 1553B was adopted in 1978 and served well, but bandwidth is becoming a limiting factor.

2. **Optic Fiber MIL-STD-1773 -**defines a fiber optic bus. This system is widely used for on-board command and telemetry transfer between military spacecraft components, subsystems and instruments, and within complex components themselves. 1773 systems achieve a 1 Mb/s data rate at 32 bits, but the AS 1773 implementation, now in development, has a dual rate of 1 Mb/s or 20 Mb/s.

   Fiber optic systems are uniquely resistant to radiation and other electro-magnetic environment effects.

3. VersaModule Eurocard (VME) Bus -VME, developed by combining the commercial Motorola Versa bus and Signetics, Mosteks and Thompson CSFs Eurocard format, is now defined by the IEEE P1014-1987 standard.

It is widely used in industrial, commercial and military applications with over 300 manufacturers of VME bus products worldwide. VME is based on 680xxx family of processors. VME is a 32-bit architecture with a 40 Mb/s throughput.

4. Peripheral Component Interconnect (PCI) Bus PCI is in widespread use in the computer industry. Although PCI was developed by Intel, it is not tied to any specific processor.

It appears that PCI may eventually replace the older ISA bus and is competing with VME for industrial use.

PCI can be 32 or 64-bits wide. It has peak transfer rates of 132 Mb/s, with a sustained transfer rates around 25 Mb/s. The PCI standard is maintained by the PCI Manufacturers Group with the electrical interface defined by IEEE P1386.1.

5. Futurebus+ -Futurebus+ was designed to offer great potential throughout up to 500-600 Mb/s, as well as a large (300mm x 300mm) board size for installation of peripherals.

It is supported by a fully developed IEEE standard (ANSI/IEEE 896). Although it is an open interface, only 3 or 4 manufacturers actually produce to it.

One drawback to Futurebus+ is the larger board size, requiring more volume than the other types of interfaces that have smaller form factors. Typical throughput is 100-125 Mb/s at 32 bits.

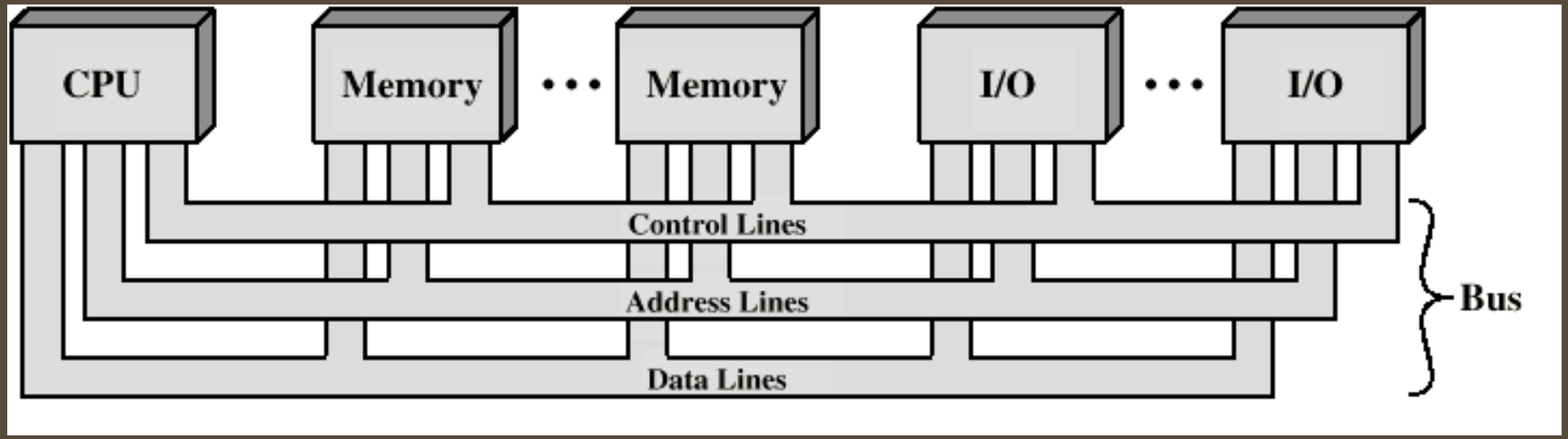
6. VersaModule Eurocard (VME64) Bus -With VME lagging the improved performance of PCI and Compact PCI, the VME group extended throughput with the VME64 configuration.

VME64 expands the architecture to a 64 bit data path. VME64 is also backward compatible with VME. Performance is 80 Mb/s throughput on a 64 bit pathway.

7. ARINC 429 -Aeronautical Radio Inc?s Airlines Electronic Engineering Committee (a group affiliated with and supported by major international airline carriers and manufacturers) manages ARINC Standard 429 - "Mark 33 Digital Information Transfer System" for a commercial aircraft data bus. It is widely implemented in the commercial aircraft avionics industry. Performance is 100Kb/s or 12.5Kb/s at either 25 or 32 bits.

8. Systems Interface Bus (SIB) SIB is a proprietary bus structure, developed for earlier modifications in the B-52 and limited high performance applications. It is used in other parts of the current aircraft architecture. SIB is also employed for signal processing applications in the commercial market. LeCroy, the manufacturer, is migrating its new products to other interfaces. Performance is 5 Mb/s at 16 bits.

9. Industry Standard Architecture (ISA) bus This bus architecture was developed by IBM for the PC/XT and PC/AT and adopted for industrial applications. The ISA architecture is a defacto standard, still in wide use where high performance is not necessary. ISA is being replaced by the PCI bus for high performance applications in desktop computers. Today desktop computers include both ISA and PCI buses, allowing backward compatibility for older components with a migration path for high performance solutions. Performance is 3 Mb/s at 16 bits.


CPU
Memory
Memory
I/O
I/O
Control Lines
Address Lines
Data Lines
Bus

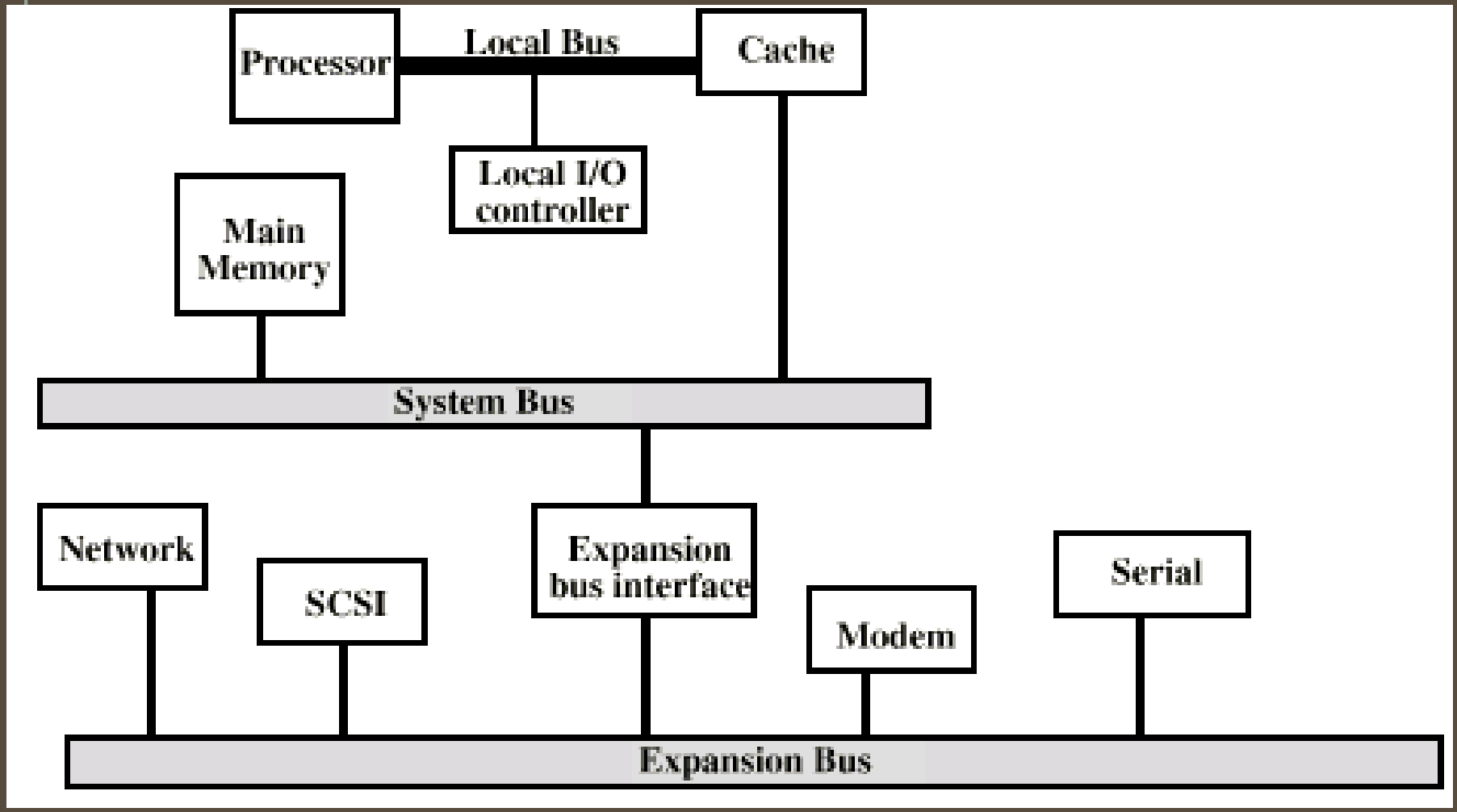
SINGLE BUS PROBLEMS

Lots of devices on one bus leads to:

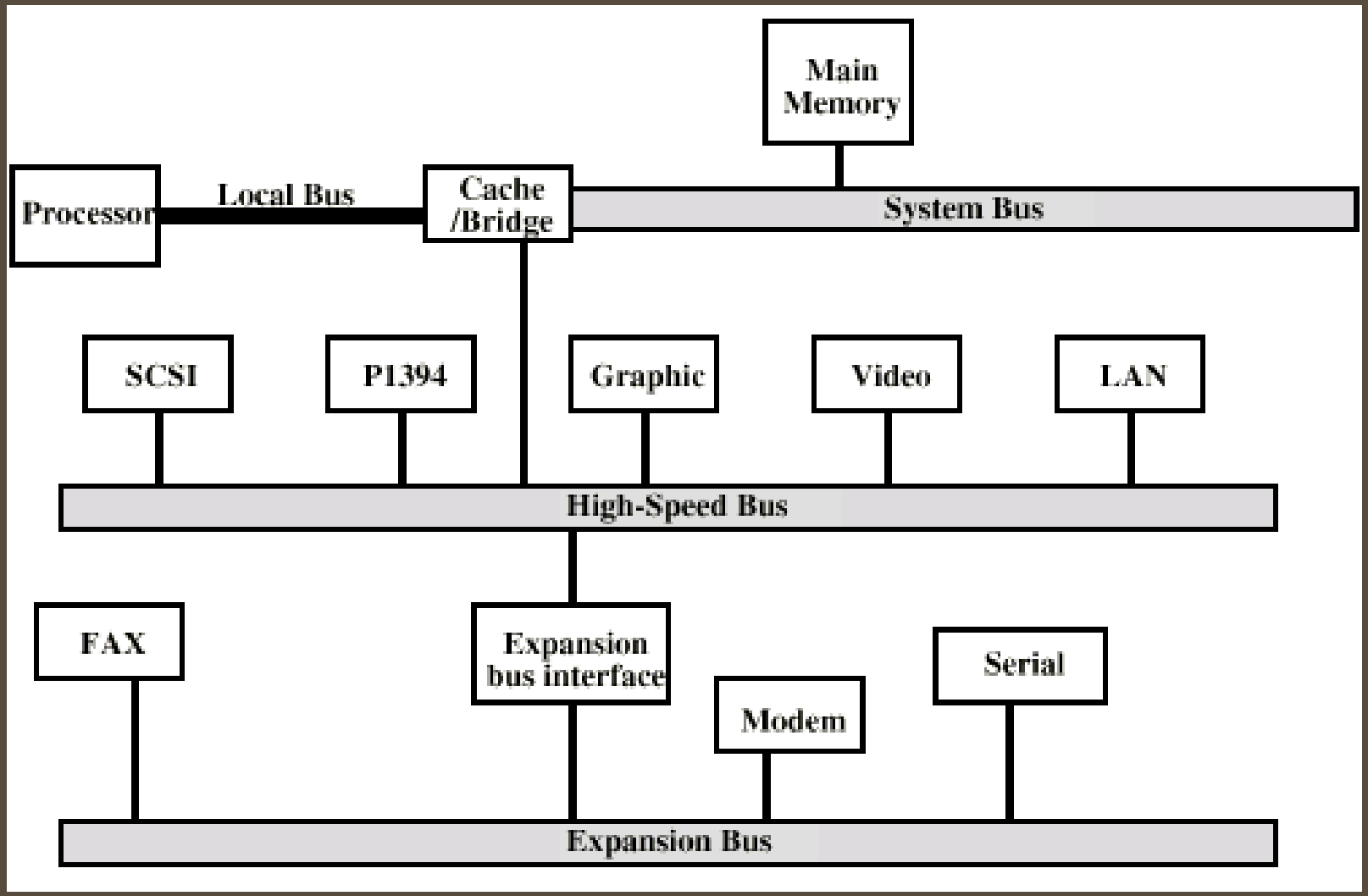
- Propagation delays
  - Long data paths mean that co-ordination of bus use can adversely affect performance
  - If aggregate data transfer approaches bus capacity

Most systems use multiple buses to overcome these problems

TRADITIONAL (ISA) (WITH CACHE)



HIGH PERFORMANCE BUS //



Description	Controlling Standard and Date	Market Acceptance	Performance	Notes
1553 Data Bus	Mil Std 1553B (1978)	Most US military aircraft systems now 1553 based.	1 Mb/s throughput at 16 bits	
Optic Fiber	Mil Std 1773 (1989)	Widely used in space craft systems	1 Mb/s throughput, 32 bits (Dual rate AS 1773 in development to provide 1 Mb/s or 20 Mb/s)	Used for on-board command and telemetry transfer between spacecraft components and subsystems
VME bus	IEEE P1014-1987 (developed from Motorola VersaBus) (1981)	Over 200 manufacturers, wide application in industrial and commercial computing, also significant military application	40 Mb/s sustained throughput at 32 bits.	Extension of the 68xxx microprocessor technology, 32 bit architecture. Current trend is use of mezzanine buses with VME backplane to increase capability.

PCI bus (Peripheral Component Interconnect)	**PCI-SIG 2.1 Local Bus Specification (1987)**	**Widely used in commercial PC market**	**132 Mb/s peak throughput at 32 bits, (25 Mb/s sustained), 264 Mb/s peak throughput at 64 bits**	**Originally based on x86/DOS processor technology**
Futurebus+	IEEE 896.5a (1994)	Proposed for military applications	100 Mb/s at 32 bits	Advertised potential throughput 500 Mb/s; board size 300mmx300mm ◆ twice the size of VME. Few manufacturers. High cost.

VME64	ANSI/VITA 1-1994 (1995)	Developed from VME standard, expected to be produced by many of current VME manufacturers	80 Mb/s sustained at 64 bits (proposed upgrade to 160 Mb/s stalled by development problems)	In production. Growth potential with VME320, with 320 Mb/s throughput is in development
Mark 33 Digital Information Transfer System	ARINC 429 (1977)	Commercial aircraft data bus	100Kb/s or 12.5Kb/s at 25 or 32 bits	Wide use in the commercial aircraft avionics industry.
SIB (Systems Interface Bus)	LeCroy P1123 (1990)	Proprietary bus, some military applications	5 Mb/s throughput at 32 bits	
ISA	IEEE P-1882.1 (1996) (From IBM P-ISA, 1982)	De facto industry standard for commercial PC until	3 Mb/s throughput at 16 bits	Widely used in commercial PC applications

	AFDX	ARINC 429	CAN	TTP
Max. frame length	1518 bytes	32 bits	8 bytes	240 bytes
Frame types	normal	broadcast, file transfer	data, remote, error, overload	initialization, normal, x-frames
Max. bit rate of current implementations	10/100 Mbit/s	100 kbit/s	1 Mbit/s	25 Mbit/s
Media access	direct	direct	CSMA/CA	TDMA
Max. bus length	< 100 m	~ 65 m	40 m recommended	typically < 100 m (not limited by protocol)
Latency	depends on network load	very small; only controller-dependent	depends on message priority and network load	TTA usage: typically < 20 us
Jitter	depends on network load	very small; only controller-dependent	depends on message priority and network load	< precision (configurable, typically 5 us)
Error containment	yes; by independent switch device	no; single error can cause total loss of communication	no; single error can cause total loss of communication	yes; per node (communication network interface, bus guardian)

	AFDX	ARINC 429	CAN	TTP
Error handling strategy	shut off erroneous nodes	ignored by receivers	immediate retry, passive state via error counters, shut off erroneous nodes (bus-off)	replicated channels, shut off erroneous nodes (fail-silent in bus, fail-operational in star)
Components	available, incl. TCP/IP protocol implementations, expensive	available, relatively inexpensive;	available, inexpensive	available, low-cost
Voltage mode	shielded twisted pair or optical fibers	twisted pair	twisted pair	shielded twisted pair, optical fiber or 100Base T/F (Ethernet-like)
Price per chip	250 – 700 $	30 – 200 $	1 – 2 $	15 – 40 $
Net data rate	–	53 kbit/s	< 300 kbit/s for 500 kbit/s network	< 4000 kbit/s (dual) for twisted pair < 20000 kbit/s (dual) for 100BaseT/F
Cost per switch	~ 15,000 $	–	–	~ 75 $

CAN

Controller Area Network (CAN) is a serial data communications bus developed in the mid-eighties by Robert Bosch GmbH for the German car industry. It has since been adopted worldwide for automobile data communications, and in a wide range of other applications.

The principal needs which drove the development of CAN were similar to those which spawned avionic data buses, i.e. to provide real-time data communication, with reduced cabling size and weight, and standardized I/O specification.

CAN belongs to the class of event-triggered protocols where the temporal control signals are derived primarily from events occurring outside or inside the computer system. Messages are sent if the host computer requests the transmission of a message, the channel is idle and the message priority wins over the messages that other nodes intend to send at the same time. CAN is deployed in a bus topology (see Fig. 2).

Key Attributes

- Multimaster priority-based serial communications protocol supporting distributed real-time control and multiplexing using non-destructive contention-based arbitration
- Bit rates: 1 Mbit/s (with 40m bus), 100 kbit/s (with 500m bus)
- Encoding: non return to zero (NRZ)
- Message length: 0 to 8 bytes
- Classes of service: periodic and sporadic
- Media access: carrier sense multiple access with collision avoidance (CSMA/CA)
- Topology: terminated differential two wire bus
- Media: screened or unscreened twisted pair or flat pair telephone cable

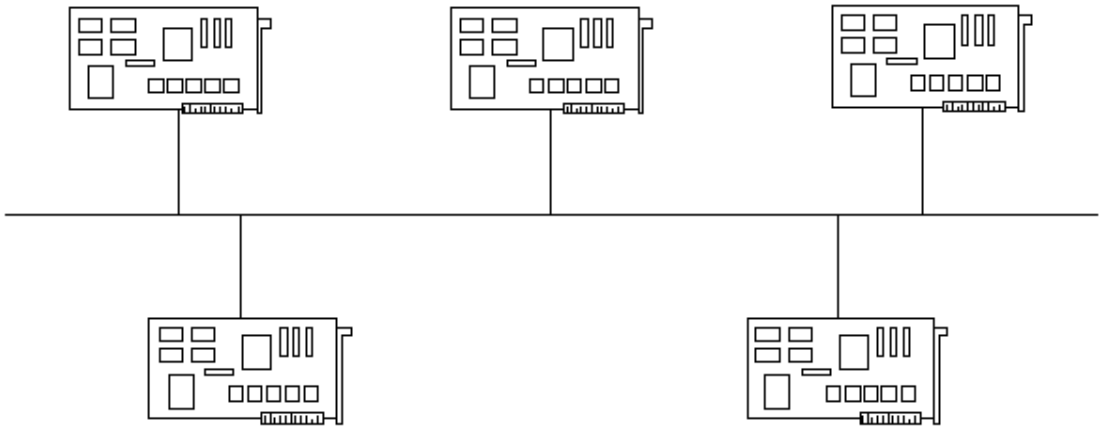


Fig. 2: CAN topology

TTP

Time-Triggered Protocol (TTP) has initially been developed more than 20 years ago at the Vienna University of Technology and is now being maintained by the international cross-industry consortium TTA-Group since 2001.

The protocol is at the heart of the Time-Triggered Architecture (TTA), which is a distributed computer platform for highly dependable real-time systems in the automotive, aerospace and other transport industry applications.

A TTA system has effective consistency services and error detection mechanisms implemented to provide a maximum degree of fault tolerance, safety, and availability. Fault tolerance is dependent on the network topology used.

TTA can be implemented in a bus or star topology with controllers as bus interface units (see Fig. 3).

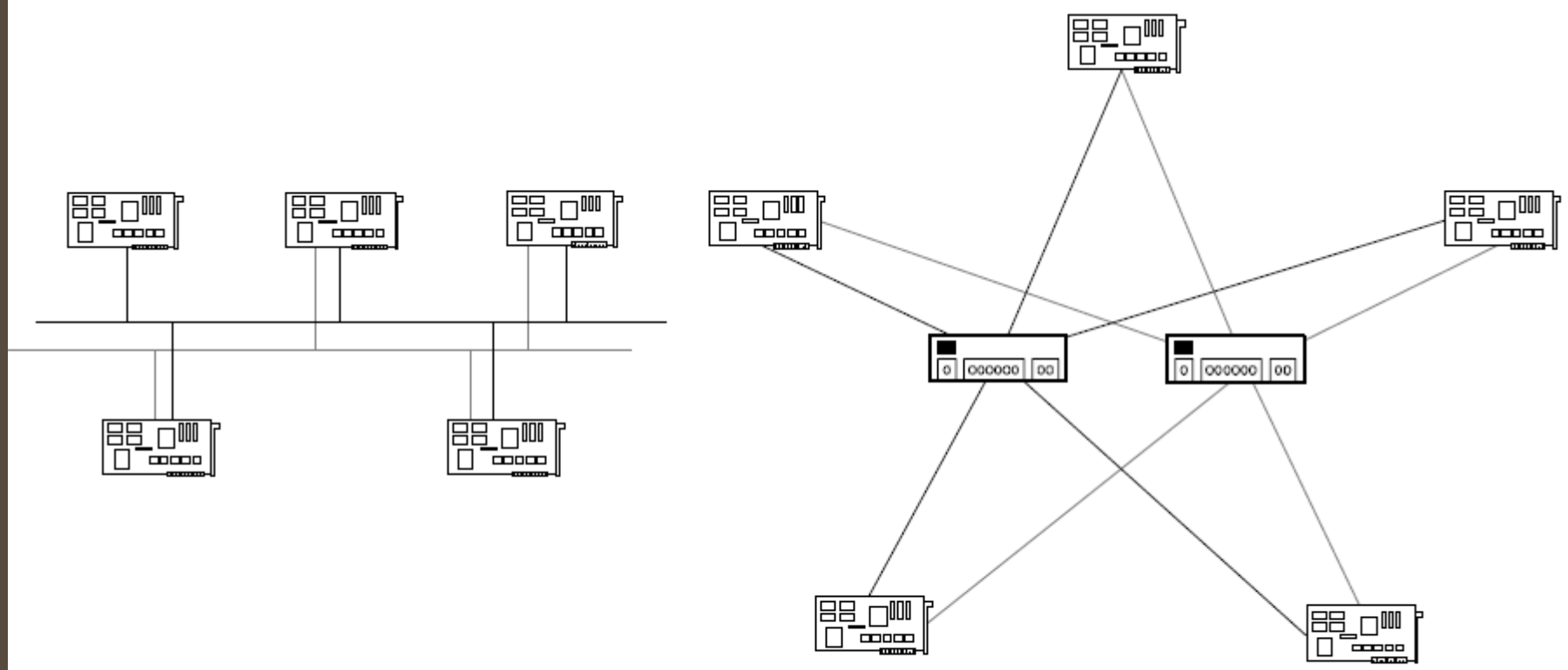


Fig. 3: TTP in star and bus topology

Key Attributes

- Real-time communication protocol for interconnection of LRUs in distributed real-time fault-tolerant systems but also backplane (see FADEC)

- Bit rates: currently available TTP controllers support up to 25 Mbit/s synchronous and up to 5 Mbit/s asynchronous transmission.
  Upper range is not limited by TTP itself and can be extended with new implementations of the TTP communication controller.

- Encoding: modified frequency modulation (MFM) and Manchester (both up to 5 Mbit/s), and MII (up to 25 Mbit/s) with currently available TTP controllers
- Message length: up to 240 byte with 4-8 bit header and 24-bit CRC
- Media access: distributed Time Division Multiple Access
- Topology: dual channel linear bus and star topology or mixed
- Media: copper and optical fiber
- Number of nodes: up to 64 nodes

AFDX (ARINC 664)

Avionics Full-Duplex Switched Ethernet (AFDX) is used as the main avionics data bus network on board the Airbus A380. Based on commercial 10/100 Mbit/s switched Ethernet, AFDX uses a special protocol for deterministic timing and redundancy management to provide secure and reliable communications of critical and non-critical data.

The AFDX communication protocol has been derived from commercial data bus standards to achieve the deterministic behavior for avionics applications.

AFDX protocol is specifically defined by ARINC 664 part 7 and is supported by other parts of ARINC 664.

End systems (equipped with an AFDX controller) communicate based on virtual links by use of bandwidth allocation gaps. Switches (central AFDX switch) incorporate functions for filtering and policing, switching based on configuration tables, end-system and network monitoring.

Switched Ethernet is based on a star topology with full-duplex transmission, i.e. a node may send and receive at the same time (see Fig. 4).

All nodes are connected to a switch that forms the center of the star.

This switch distributes the messages in the system. If two or more nodes start to transmit at approximately the same time, their messages will be buffered in the switch and relayed sequentially.

Key Attributes

- Full-Duplex Switched Ethernet
- Bit rates: 10/100 Mbit/s cross data rate
- Encoding: PAM5x5
- Message length: 64 – 1518 bytes
- Classes of service: station to station, multicast and broadcast
- Topology: dual redundant star network
- Media: copper and fiber
- Number of nodes: up to 1024 (without bridges)

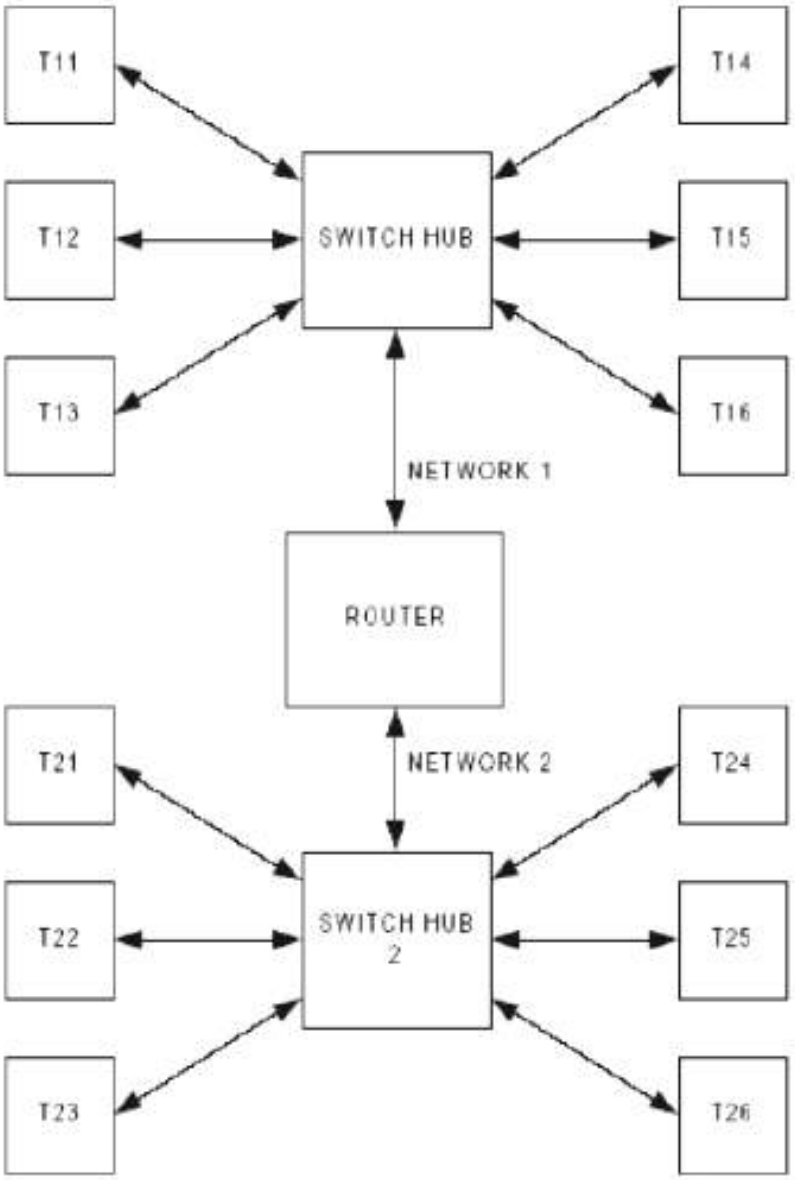


Fig. 4: Two networks connected by a router in AFDX

ARINC-429

Overview of ARINC

- ARINC stands for Aeronautical Radio, Inc., a private corporation organized in 1929, and is comprised of airlines, aircraft manufacturers and avionics equipment manufacturers as corporate shareholders.

- ARINC was developed to produce specifications and standards for avionics equipment outside the government for domestic and overseas manufacturers.

- ARINC copywrites and publishes standards produced by the Airlines Electronic Engineering Committee (AEEC).

- The AEEC is an international standards organization made up of major airline operators, avionics industry manufacturers and ARINC members.

- The AEEC sets standards for avionics equipment and systems and provides industry defined requirements for standardization of form, fit and function between various manufacturers products.

ARINC 429 Specification Overview

- The ARINC 429 Specification defines the standard requirements for the transfer of digital data between avionics systems on commercial aircraft. ARINC 429 is also known as the Mark 33 DITS Specification.

- Signal levels, timing and protocol characteristics are defined for ease of design implementation and data communications on the Mark 33 Digital Information Transfer System (DITS) bus.

- ARINC 429 is a privately copywritten specification developed to provide interchangeability and interoperability of line replaceable units (LRUs) in commercial aircraft.

- Manufacturers of avionics equipment are under no requirement to comply to the ARINC 429 Specification, but designing avionics systems to meet the design guidelines provides cross-manufacturer interoperability between functional units.

ARINC publishes the AEEC produced standards under three types of documents:

1. ARINC Characteristics

- Characteristics are definitions of the form, fit and function of avionics equipment.
- These documents are equipment specific and define how a unit will operate.
- The ARINC 500 Series of Characteristics define older analog avionics equipment where the ARINC 700 Series are more current documents and are typically digital versions of the analog specs.
- 400 Series documents are general design and support documentation for the 500 Series avionics equipment characteristics.
- 600 Series documents are general design and support documentation for the 700 Series avionics equipment characteristics.

2. ARINC Specifications

Specifications are used to define

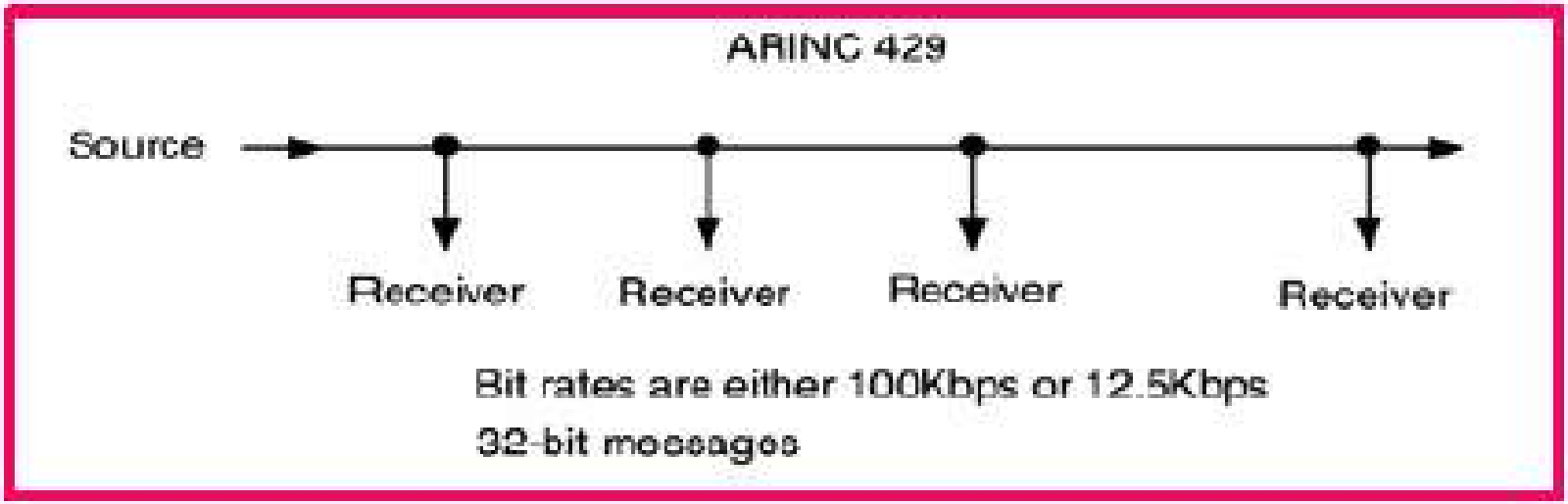
- Physical packaging and mounting of avionics equipment
- Data communications standards
- High level computer languages

The ARINC 429 Specification, Mark 33 Digital Information Transfer System falls under the Specification document category.

3. ARINC Reports

Reports provide general information and best practice guidelines for airlines. Reports predominately refer to maintenance and support procedures.

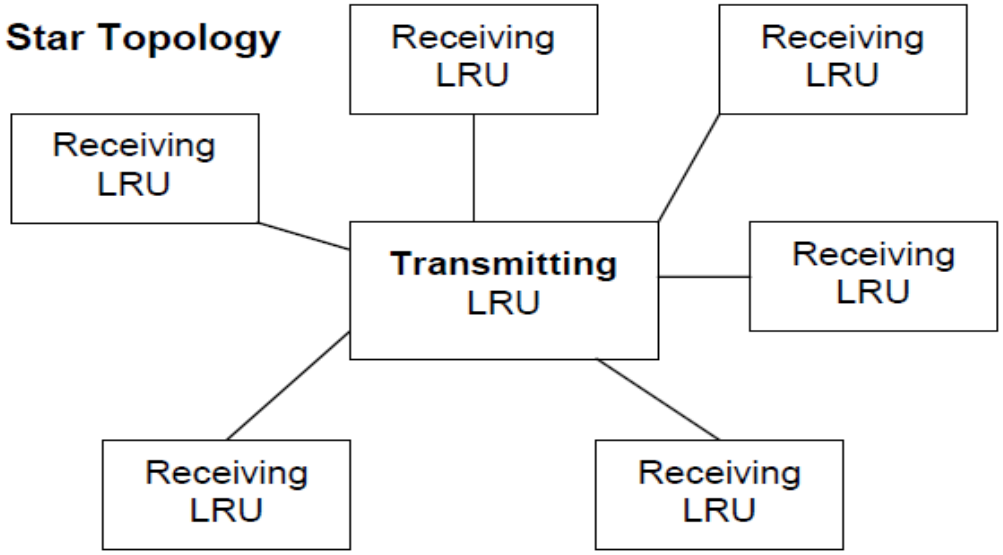
Communication Data Bus

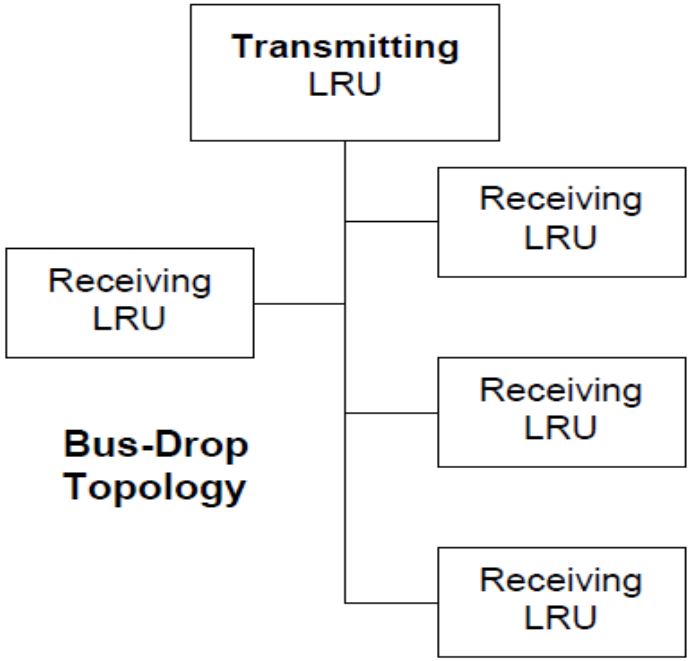


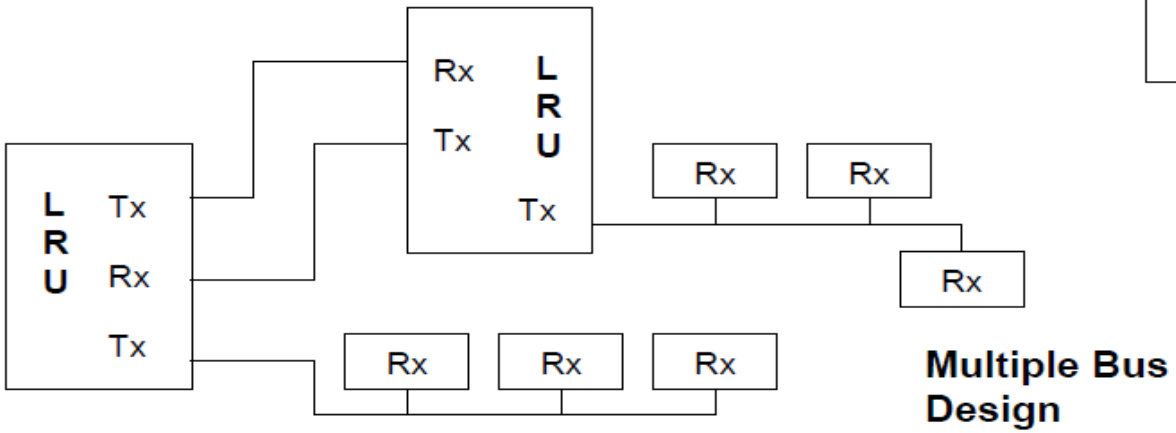
The ARINC 429 Specification

- ARINC 429 defines both the hardware and data formats required for bus transmission.
- Hardware consists of a single transmitter – or source – connected to from 1-20 receivers– or sinks – on one twisted wire pair.
- Data can be transmitted in one direction only –simplex communication – with bi-directional transmission requiring two channels or buses.
- The devices, line replaceable units or LRUs, are most commonly configured in a star or bus-drop topology.
- Each LRU may contain multiple transmitters and receivers communicating on different buses.
- This simple architecture, almost point-to-point wiring, provides a highly reliable transfer of data.

The ARINC 429 Specification







The ARINC 429 Specification

- Transmission from the source LRU is comprised of 32 bit words containing a 24 bit data portion containing the actual information, and an 8 bit label describing the data itself.

- LRUs have no address assigned through ARINC 429, but rather have Equipment ID numbers which allow grouping equipment into systems, which facilitates system management and file transfers.

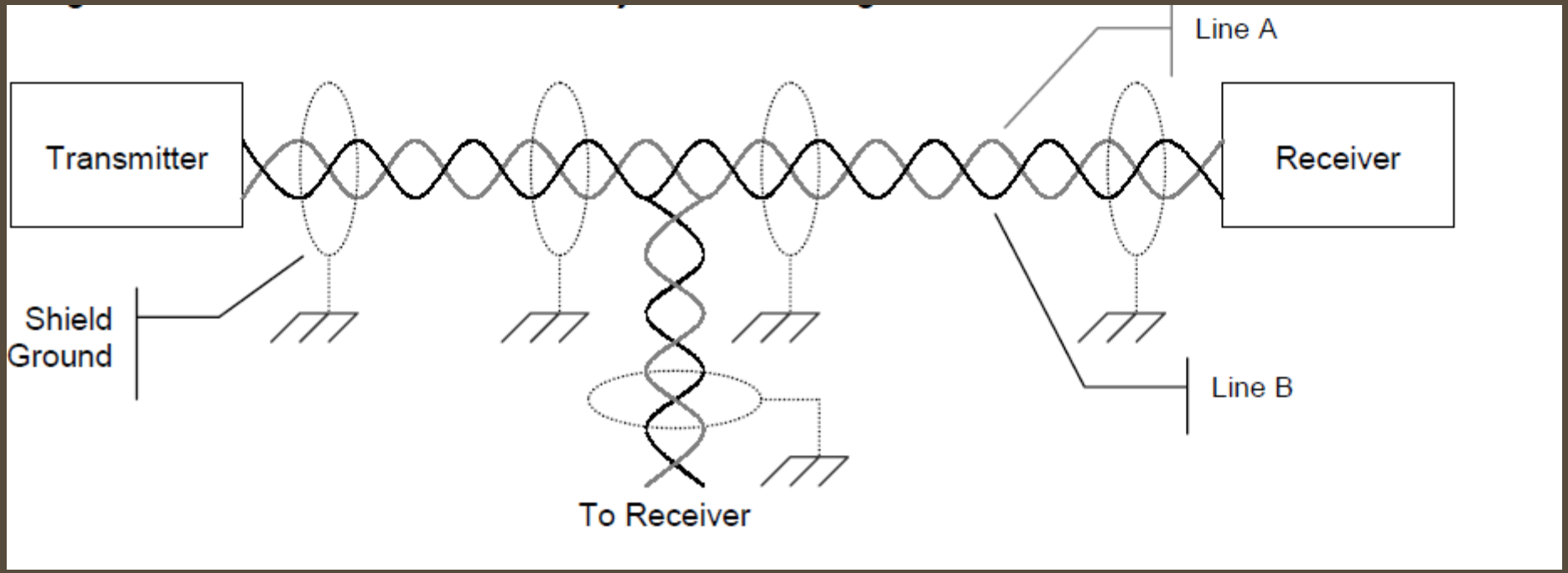
- Sequential words are separated by at least 4 bit times of null or zero voltage. By utilizing this null gap between words, a separate clock signal is unnecessary.

- Transmission rates may be at either a low speed – 12.5 kHz – or a high speed – 100kHz.

Cable Characteristics

- The transmission bus media uses a 78 Ω shielded twisted pair cable. The shield must be grounded at each end and at all junctions along the bus.
- The transmitting source output impedance should be 75 Ω ± 5 Ω divided equally between Line A and Line B.
- This balanced output should closely match the impedance of the cable. The receiving sink must have an effective input impedance of 8k Ω minimum.
- Maximum length is not specified, as it is dependent on the number of sink receivers, sink drain and source power.
- Most systems are designed for under 150 feet, but conditions permitting, can extend to 300 feet and beyond.

Cable Characteristics



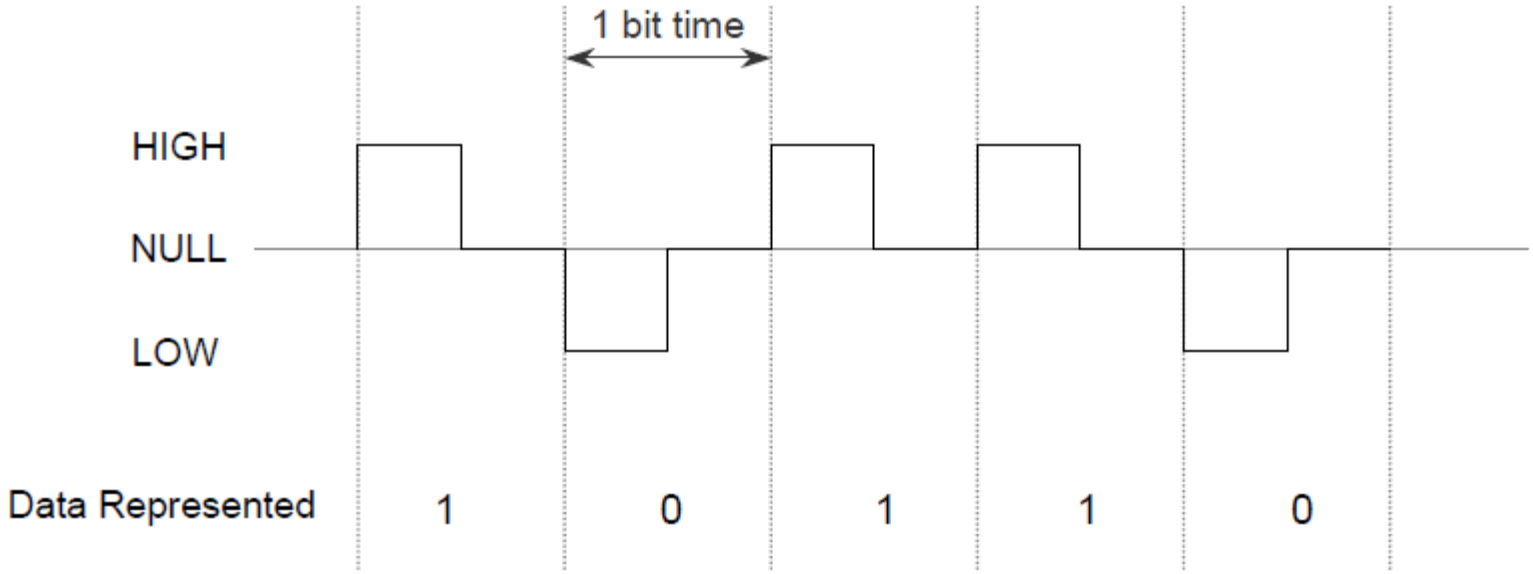
Transmission Characteristics

- ARINC 429 specifies two speeds for data transmission. Low speed operation is stated at 12.5 kHz, with an actual allowable range of 12 to 14.5 kHz.
- High speed operation is 100 kHz ± 1% allowed. These two data rates can not be used on the same transmission bus.
- Data is transmitted in a bipolar, Return-to-Zero format. This is a tri-state modulation consisting of HIGH, NULL and LOW states.
- Transmission voltages are measured across the output terminals of the source.
- Voltages presented across the receiver input will be dependent on line length, stub configuration and the number of receivers connected.
- The following voltage levels indicate the three allowable states:

TRANSMIT	STATE	RECEIVE
+10.0 V ± 1.0 V	HIGH	+6.5 to 13 V
0 V ± 0.5V	NULL	+2.5 to -2.5 V
-10.0 V ± 1.0 V	LOW	-6.5 to -13 V

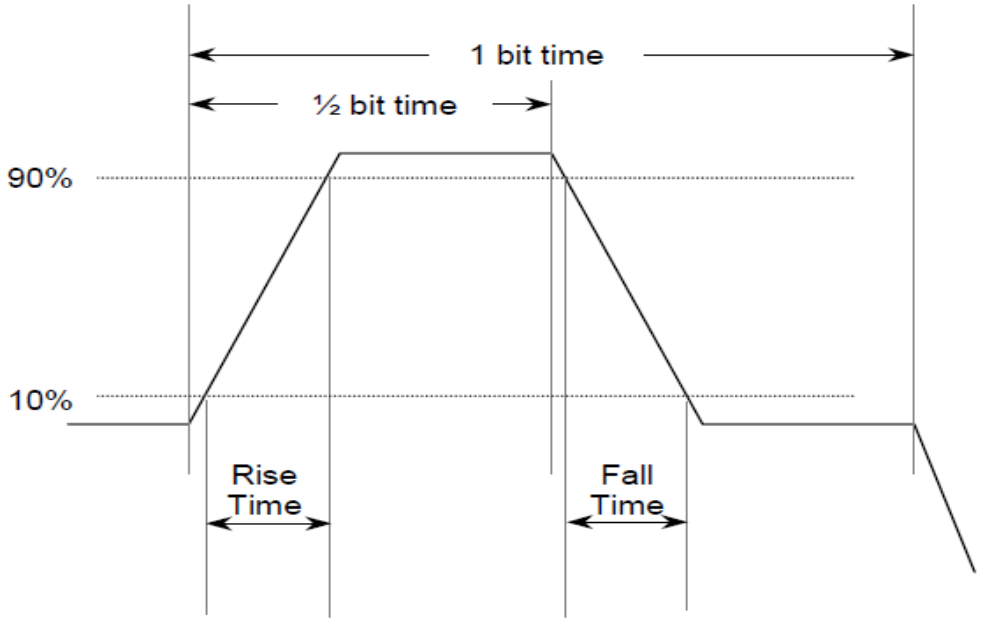
- In bipolar, Return-to-Zero – or RZ – format, a HIGH (or 1) is achieved with the transmission signal going from NULL to +10 V for the first half of the bit cycle, then returning to zero or NULL.
- A LOW (or 0) is produced by the signal dropping from NULL to –10 V for the first half bit cycle, then returning to zero.
- With a Return-to-Zero modulation format, each bit cycle time ends with the signal level at 0 Volts, eliminating the need for an external clock, creating a self-clocking signal.
- An example of the bipolar, tri-state RZ signal is shown here:

An example of the bipolar, tri-state RZ signal is shown here:



Waveform Parameters

Pulse rise and fall times are controlled by RC circuits built into ARINC 429 transmitters. This circuitry minimizes overshoot ringing common with short rise times. Allowable rise and fall times are shown below for both bit rates. Bit and ½ bit times are also defined.



	High Speed	Low Speed
Bit Rate	100 kbps ± 1%	12 – 14.5 kbps ± 1%
1 bit time	10 µsec ± 2.5%	(1/Bit rate) µsec ± 2.5%
½ bit time	5 µsec ± 5%	(1 bit time/2) ± 5%
Rise Time	1.5 µsec ± 0.5 µsec	10 µsec ± 5 µsec
Fall Time	1.5 µsec ± 0.5 µsec	10 µsec ± 5 µsec

Word Formats

- ARINC 429 protocol uses a point-to-point format, transmitting data from a single source on the bus to up to 20 receivers.
- The transmitter is always transmitting, either data words or the NULL state.
- Most ARINC messages contain only one data word consisting of either Binary (BNR), Binary Coded Decimal (BCD) or alphanumeric data encoded using ISO Alphabet No. 5.
- File data transfers that send more than one word are also allowed.
- ARINC 429 data words are 32 bit words made up of five primary fields:

  - Parity – 1 bit
  - Sign/Status Matrix (SSM) – 2 bits
  - Data – 19 bits
  - Source/Destination Identifier (SDI) – 2 bits
  - Label – 8 bits

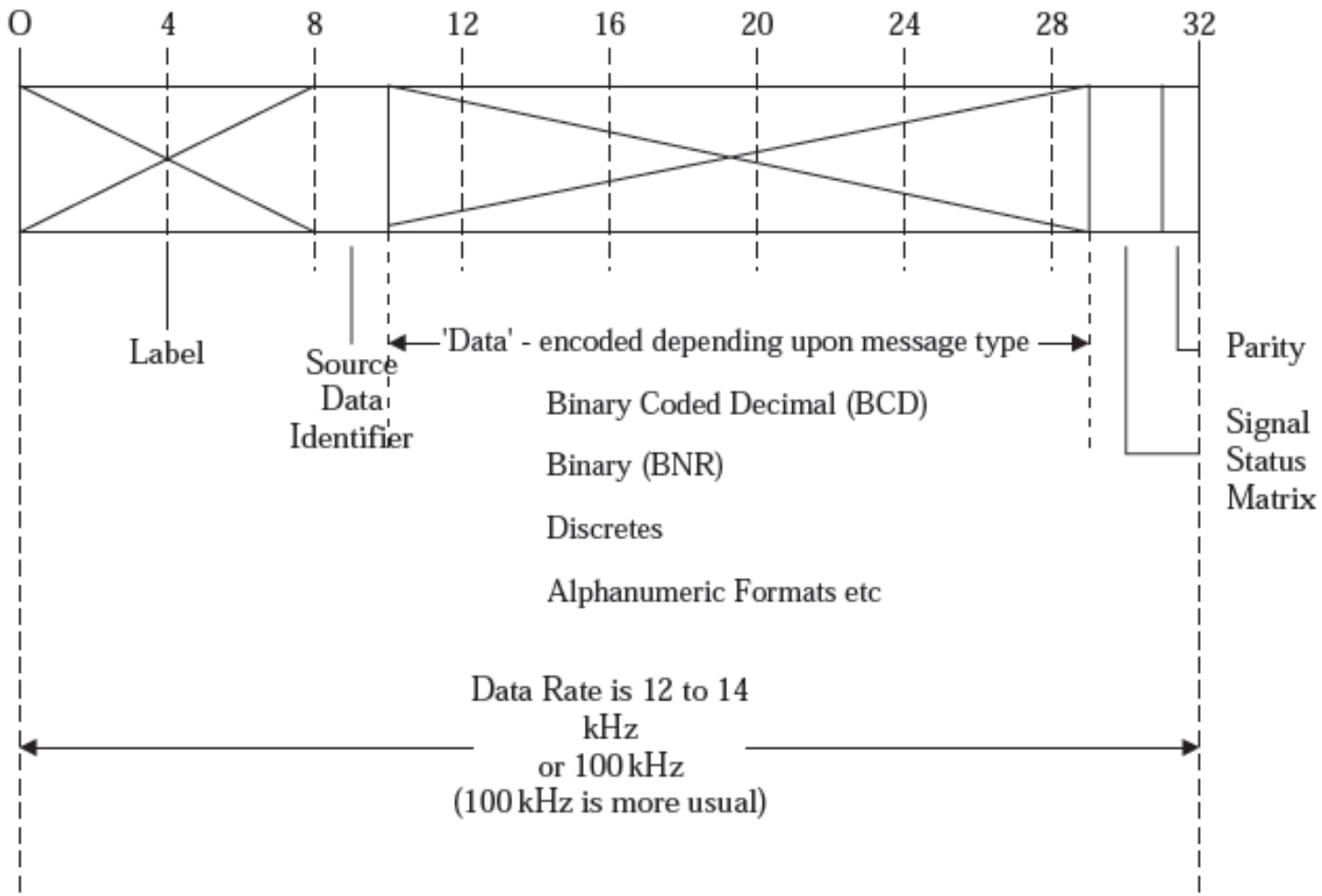
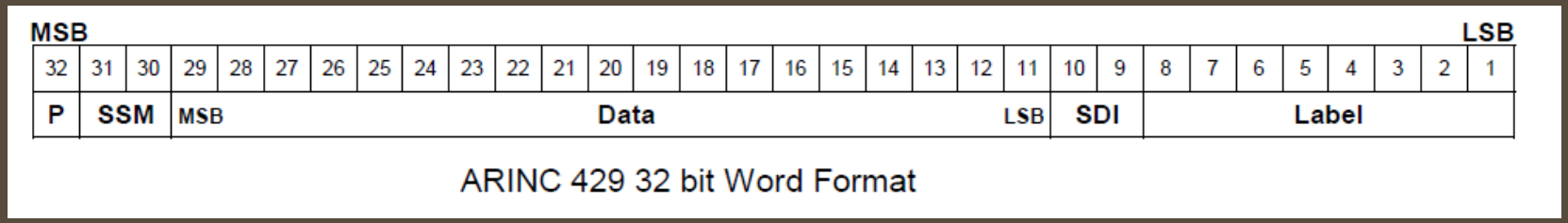


Figure 12.9 A429 data word format



ARINC 429 32 bit Word Format

- The only two fields definitively required are the Label and the Parity bit, leaving up to 23 bits available for higher resolution data representation.
- Many non-standard word formats have been adopted by various manufacturers of avionics equipment.
- Even with the variations included, all ARINC data is transmitted in 32 bit words.
- Any unused bits are padded with zeros.

Parity:-

- ARINC 429 defines the Most Significant Bit (MSB) of the data word as the Parity bit. ARINC uses odd parity as an error check to insure accurate data reception.

- The number of Logic 1s transmitted in each word is an odd number, with bit 32 being set or cleared to obtain the odd count.

- ARINC 429 specifies no means of error correction, only error detection.

Sign/Status Matrix

- Bits 31-30 are assigned as the Sign/Status Matrix field or SSM.

- Depending on the words Label, which indicates which type of data is being transmitted, the SSM field can provide different information.

- This field can be used to indicate sign or direction of the words data, or report source equipment operating status and is dependent on the data type.

Sign/Status Matrix

BCD data SSM Sign Coding

BIT 31	BIT 30	Decoded Information
0	0	Plus, North, East, Right, To, Above
0	1	No Computed Data
1	0	Functional Test
1	1	Minus, South, West, Left, From, Below

BNR data SSM Status Coding

BIT 31	BIT 30	Decoded Information
0	0	Failure Warning
0	1	No Computed Data
1	0	Functional Test
1	1	Normal Operation

BNR data SSM Sign Coding

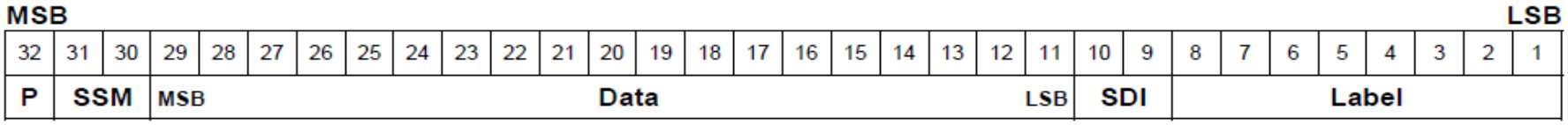
BIT 29	Decoded Information
0	Plus, North, East, Right, To, Above
1	Minus, South, West, Left, From, Below

Discrete data SSM Status Coding

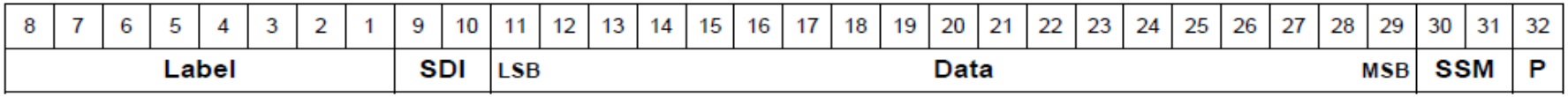
BIT 31	BIT 30	Decoded Information
0	0	Verified Data, Normal Operation
0	1	No Computed Data
1	0	Functional Test
1	1	Failure Warning

Data:-

- ARINC 429 defines bits 11-29 as those containing the word's data information.
- Formatting of the data bits, indeed the entire ARINC 429 word, is very flexible.
- When transmitting data words on the ARINC bus, the Label is transmitted first, MSB first, followed by the rest of the bit field, LSB first. Bit transmission order looks like this:



ARINC 429 32 bit Word Format



ARINC 429 Word Transfer Order

- The Label is always transmitted first, in reverse order to rest of the ARINC word – a compensation for compatibility with legacy systems.

- The receiving LRU is responsible for data translation and regrouping of bits into proper order.

- **Data types available in ARINC 429 are:**

  - Binary – BNR – Transmitted in fractional two's complement notation
  - Binary Coded Decimal – BCD – Numerical subset of ISO Alphabet No. 5
  - Discrete Data – Combination of BNR, BCD or individual bit representation
  - Maintenance Data and Acknowledgement – Requires two-way communication
  - Williamsburg/Buckhorn Protocol – A bit-oriented protocol for file transfers

Data Types

BNR Data

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
P	SSM		MSB																		LSB	SDI		Label							

ARINC 429 BNR Word Format

BCD Data

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
P	**SSM**		**Digit 1**			**Digit 2**				**Digit 3**				**Digit 4**				**Digit 5**				**SDI**		**Label**							

ARINC 429 BCD Word Format

Discrete Data

Discrete data can be made up of BNR and/or BCD data, or as individual bits representing specific equipment conditions. Pass/Fail, Activated/Non-Activated and True/False conditions relating to system or subsystem operational activity can be represented by setting or clearing predefined bits in the word data field.

Maintenance Data and Acknowledgement

Maintenance Data and Acknowledgement implies duplex or two-way communication between source and sink. Since ARINC 429 only provides for one-way simplex transmission, two ARINC channels are required for an LRU to send and receive data. Maintenance messages typically require exchanging a sequence of messages and often utilize a bit oriented protocol such as the Williamsburg/Buckhorn protocol.

Source/Destination Identifier

The Source/Destination Identifier – SDI – utilizes bits 9-10 and is optional under the ARINC 429 Specification. The SDI can be used to identify which source is transmitting the data or by multiple receivers to identify which receiver the data is meant for.

For higher resolution data, bits 9-10 may be used instead of using them as an SDI field. When used as an Identifier, the SDI is interpreted as an extension to the word Label.

Label

Bits 1-8 contain the ARINC label known as the Information Identifier. The Label is expressed as a 3 digit octal number with receivers programmed to accept up to 255 Labels. The Label's Most Significant Bit resides in the ARINC word's Least Significant Bit location.

ARINC Label Bit Structure

	LSB						MSB	
BIT	8	7	6	5	4	3	2	1
Octal Value	4	2	1	4	2	1	2	1

Thanks and Questions