

# Arjun Nair

📞 919-786-3251    ✉ Email    🔗 LinkedIn    🐙 GitHub    🌐 Website

## EDUCATION

**Bachelor of Science in Computer and Electrical Engineering, Double Major** Aug 2019 – May 2024  
*North Carolina State University* *Raleigh, NC*

### Relevant Coursework

- ASIC & FPGA Design in Verilog, Digital System Design in Verilog, Embedded Systems, Computer Systems Programming, Data Structures and OOP, Physics of Microelectronics

## TECHNICAL SKILLS

**Languages:** C/C++, Embedded C, Python, Verilog, VHDL, Git, Assembly, MATLAB, HTML

**Circuit Design:** Altium Designer, Mentor Graphics Xpedition, PSpice, PowerDC, Logic Design, Verification Testing

## WORK EXPERIENCE

### Intel Corporation

May 2022 - Dec 2022

#### R&D IC Package Design Engineer Intern

*Chandler, AZ*

- Assisted in **designing** and **routing** package layout for **DDR**, **UCIe** and **6** other **Intel packages**
- Performed microelectronic **IC package** electrical **modeling** and **simulation** using tools such as Xpedition, PowerDC
- Designed **manufacturing drafts** (die/die bonding diagrams, packing specs, mark specs, Bill of Materials list, etc)
- Worked closely with relative **teams**, **clients** and **vendors** to support **production** and establish problem specifications
- Applied Python and C for **scripting** to streamline processes department-wide

### Edwards Vacuum

May 2021 – Aug 2021

#### Electrical Engineering Intern

*Chelmsford, MA*

- **Designed** and printed circuit board **schematics** to be used in conjunction with **12 product lines**
- Built **test fixtures** to perform Reliability Demonstration Testing on **electrical sub-assemblies**
- Performed **Design Verification Testing** (DVT) on various components and products using a variety of **lab equipment**
- Applied **EMIC** principles to ensure electronics were compliant with **industry standards**

## PROJECTS

### 🐙 Multi-Stage Neural Network | Verilog

Aug 2022

- Implemented a hardware-based multi-stage **neural network**, including a convolutional layer, a fully connected layer and a max pooling layer
- Applied **algorithms** to efficiently read and write data to and from input and output **SRAMs**
- System generates output matrix which can be used to **classify** objects
- **Optimized** design to ensure **top 1%** in cycle-count and area among **300** classmates

### 🐙 Autonomous Car Controlled by IOT | Embedded C, Python, MATLAB

Aug 2021

- **Soldered** and programmed **MSP-430** board in **C** to work in conjunction with 2 DC motors and on-board IR emitter and detector
- Implemented Pulse-Width-Modulation to control wheels using on-board **clocks** and **timers** and modelled motor characteristics in **MATLAB**
- Used **IOT** module to control car navigation via **WiFi** using a custom web interface using **UDP protocol**
- Implemented onboard **serial communication** using **SPI** protocol and tested and **debugged** device using **logic analyzer**

## ACTIVITIES & AWARDS

**Intel Department Recognition Award** (For work on DDR routing)

Nov 2022

**IEEE at NCSU** (Member)

Jan 2022 - Present

**Rock Climbing Club** (Member)

Aug 2021 - Present

**NCSU ESports Club** (Varsity Team)

Aug 2019 - Present