APB UART IP

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1. Introduction

The UART project focuses on designing and implementing a serial communication module for digital systems.
UART converts parallel data into serial data and vice versa, enabling communication between microcontrollers, FPGAs, or computers.
The main objectives of this project are:
- Implement a transmitter and receiver module.
- Verify correct data transmission and reception.
- Detect errors like framing errors.

2. Design Analysis

The UART system consists of two main modules:

Transmitter:
- Accepts parallel input data.
- Adds Start bit and Stop bit.
- Converts data to serial output.
- Uses Baud Rate Generator to control transmission speed.

Receiver:
- Reads serial data.
- Detects start and stop bits.
- Converts data to parallel output.
- Includes error detection logic for framing errors.

3. State Diagrams

Receiver FSM:
- Idle → Start → Data → Done/Error → Idle

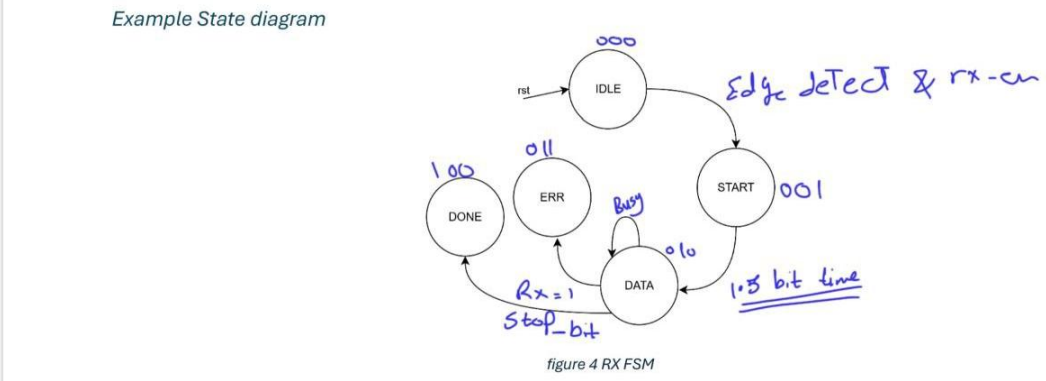


figure 4 RX FSM

4. Design Decisions

- FSM approach used for both APB and receiver for simplicity and reliability.
- Clock frequency chosen based on project specifications.
- Parallel-to-serial and serial-to-parallel conversion implemented to follow standard UART protocol.
- Error detection implemented at the receiver to ensure robust communication.

5. Verification Strategy

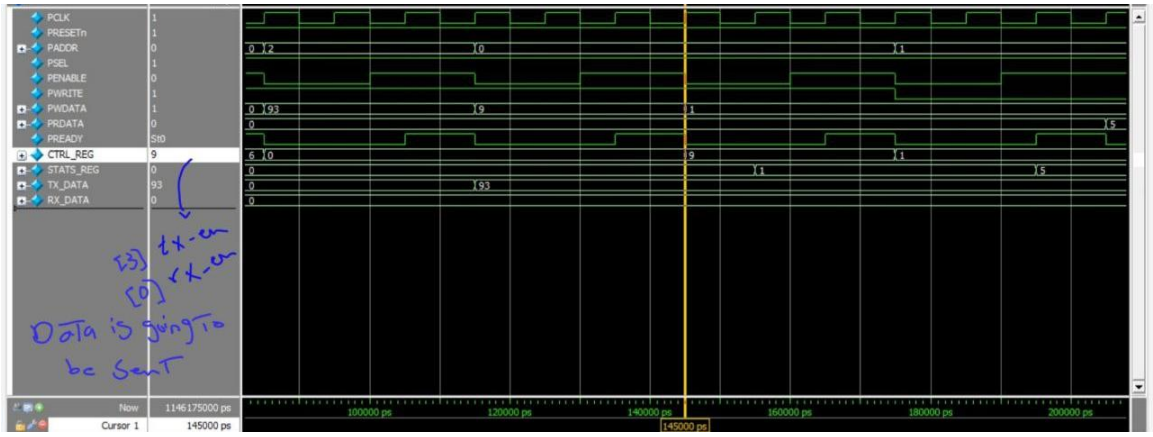
- Testbench created to simulate multiple data transmissions.
- Signals monitored: TX, RX, done, err.
- Scenarios tested:
  1. Normal data transmission (no errors).
  2. Intentional errors to verify error detection.

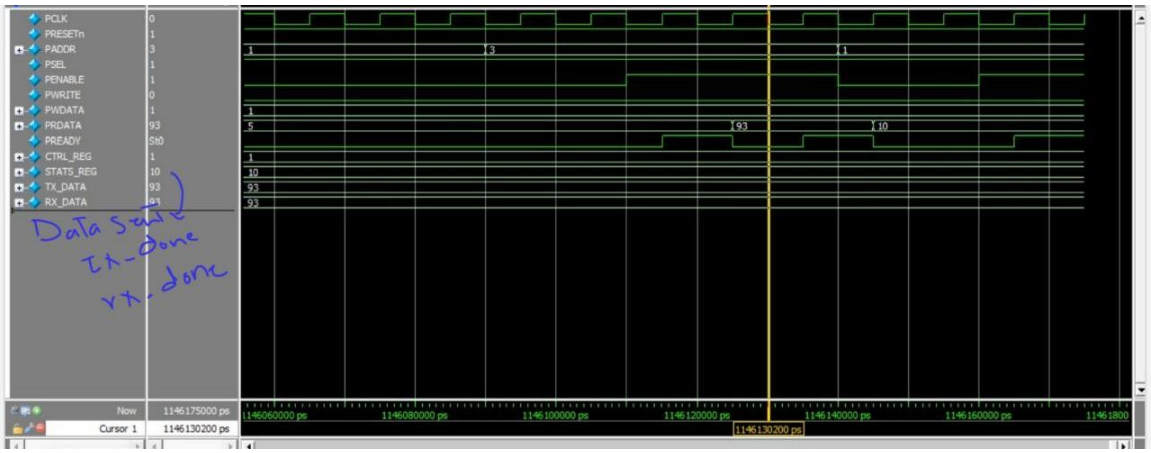
6. Simulation Results

- Transmitter and receiver verified to operate correctly.
- Waveforms demonstrate:
  - Timing of TX and RX signals.
  - Proper start and stop bit detection.
  - Error detection signals when data is invalid.

```
$display("Checking the states of the UART from PRDATA");
$display("tx_busy = %0b, tx_done = %0b", PRDATA[0], PRDATA[1]);
$display("rx_busy = %0b, rx_done = %0b, rx_error = %0b", PRDATA[2], PRDATA[3], PRDATA[4]);
```

```
VSIM 4> run -all
# Checking the states of the UART from PRDATA
# tx_busy = 1, tx_done = 0
# rx_busy = 1, rx_done = 0, rx_error = 0
# RX is = 93
# Checking the states of the UART from PRDATA
# tx_busy = 0, tx_done = 1
# rx_busy = 0, rx_done = 1, rx_error = 0
# ** Note: $stop    : C:/Users/naira/Desktop/training/Project/APB/APB_tb.v(160)
#    Time: 1146175 ns  Iteration: 1  Instance: /APB_tb
# Break in Module APB_tb at C:/Users/naira/Desktop/training/Project/APB/APB_tb.v line 160
```





7. Conclusion

- The UART design is functional, reliable, and ready for use in digital communication systems.
- Testbench verification confirms proper operation under normal and error conditions.
- Design approach using FSM ensures scalable and maintainable implementation.