ELE 3230
Microprocessors and Computer Systems

Chapter 4
8088 System Architecture

(*Hall:ch2; Brey:ch1; Triebel:ch2)

Historical Background

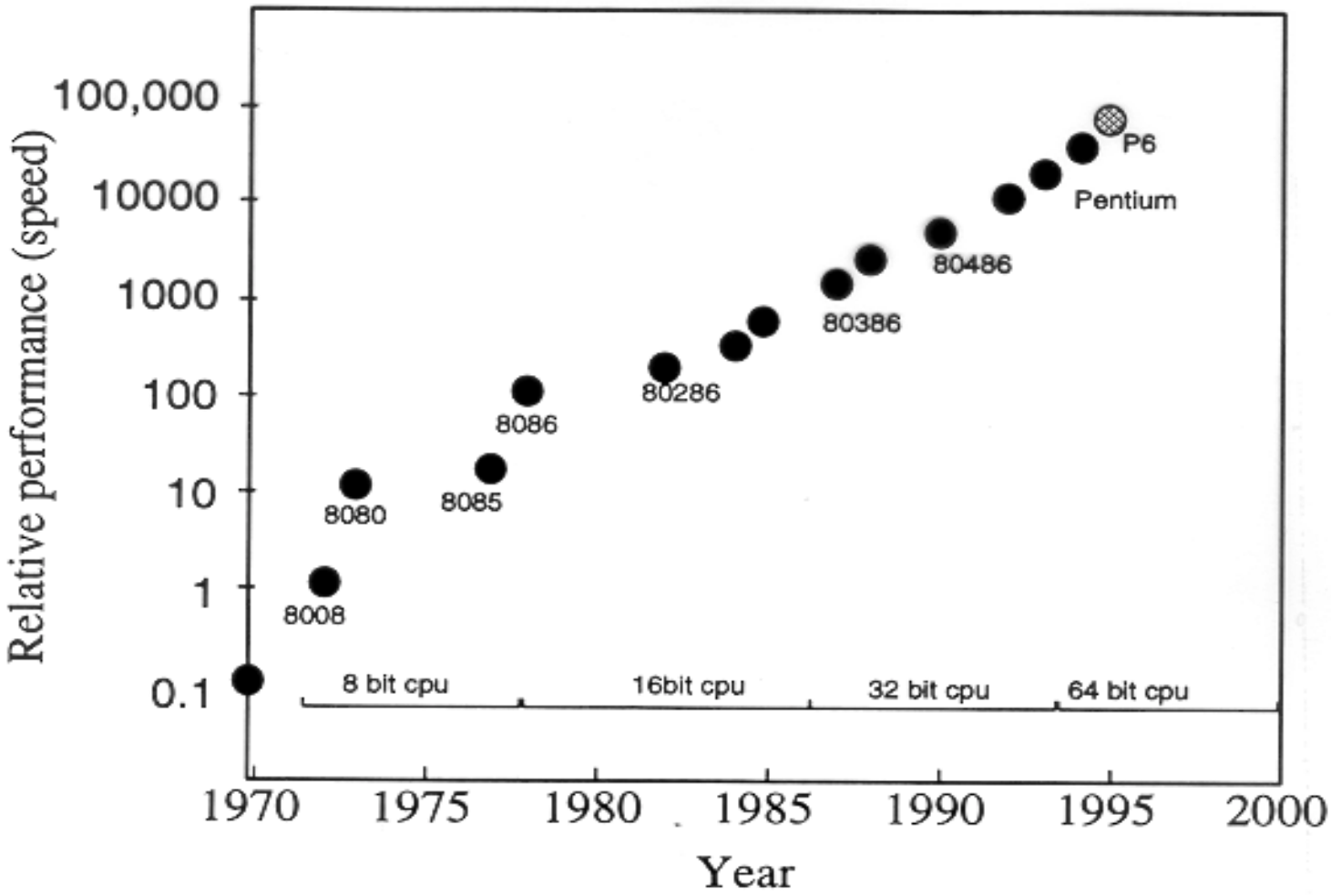
- **1969/70** Intel 4004, **first Microprocessor** (M.E.Hoff) 4 bit microprocessor, originally developed for Busicom, a small Japanese calculator company. Limited to 4096 memory location (of 4 bit data), 45 instructions; integrated 2300 PMOS transistors.
- **1971** Intel 8008, **first 8 bit microprocessor** (16K x 8bit)
- **1973** Intel 8080, 10 x faster than 8008, more memory (64k)
- **1974** Other 8 bit processors: Motorola 6800, Fairchild F8,
- **1975** Signetic 2650, MOS Technology 6502 (used in Apple II), Rockwell PPS-8
- **1976** National IMP-PACE, **first 16 bit microprocessor**, followed by Texas Instrument, TMS9900, **Zilog Z80** (8 bit) (used in Radio Shack TRS-80)
- **1977** Intel 8085 (8080 with built-in clock & system controller)
- **1978** Motorola 6809 (8 bit), **Intel 8086** (16 bit processor, 1M)
- **1978/79** **Intel 8088** - variant of 8086 with 8 external data pins
- **1981** IBM adopts Intel 8088 for IBM PC/XT

(see http://infopad.eecs.berkeley.edu/CIC/archive/cpu_history.html)

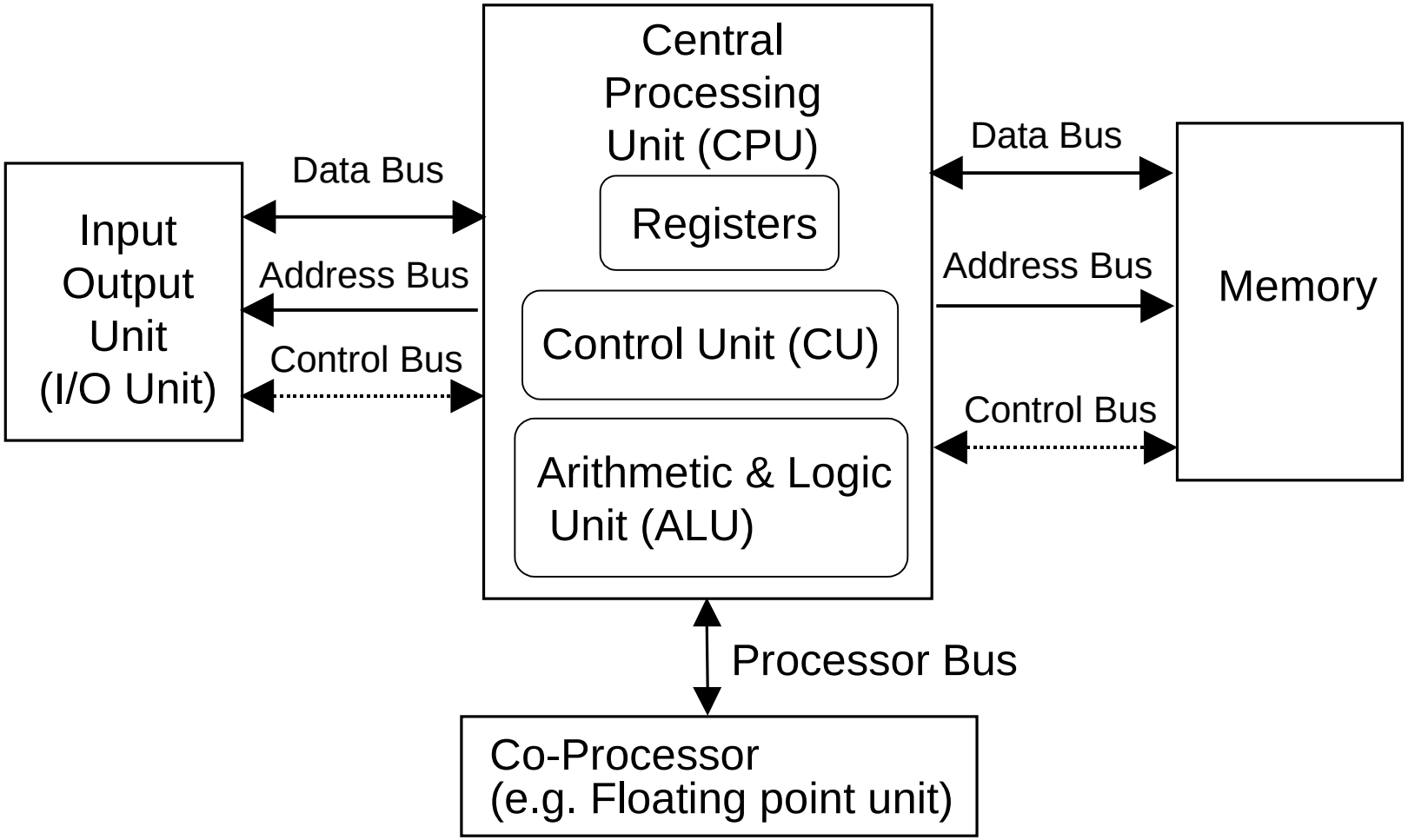
2 most popular microprocessor series:

- INTEL 8086, 80186, 80286, 80386, 80486, Pentium
- Motorola 68000, 68010, 68020, 68030, 68040

Intel Microprocessors Relative Speeds



Microprocessor Computer System



Microprocessor Computer System

- **Control Unit** (CU) generates all the control signals within the CPU. It initializes the registers on power-up, generates the signal to fetch instructions for the ALU.

  The Control unit may be implemented completely by hardware (hard-wired controller e.g. using a state counter and a Programmable Logic Array) or a mixture of software instructions (microcode stored in CPU) and hardware (microprogrammed control). Both the Intel 8086 family and Motorola 68000 family use microprogrammed controllers.

- **Registers** - small, fast memory which usually store data and addresses associated with the instruction being carried out.

- **ALU** performs arithmetic and logic operations

Instruction Execution Cycle

Two main steps in the cycle:

1. Fetch the next instruction from main memory
2. Decode and Execute the instruction

The Fetch cycle consists of

i) Use the instruction pointer (IP) to set the address bus with the address of the next instruction and increment the instruction pointer

ii) Wait (few hundred nanoseconds) for data to be transferred to the data bus from memory

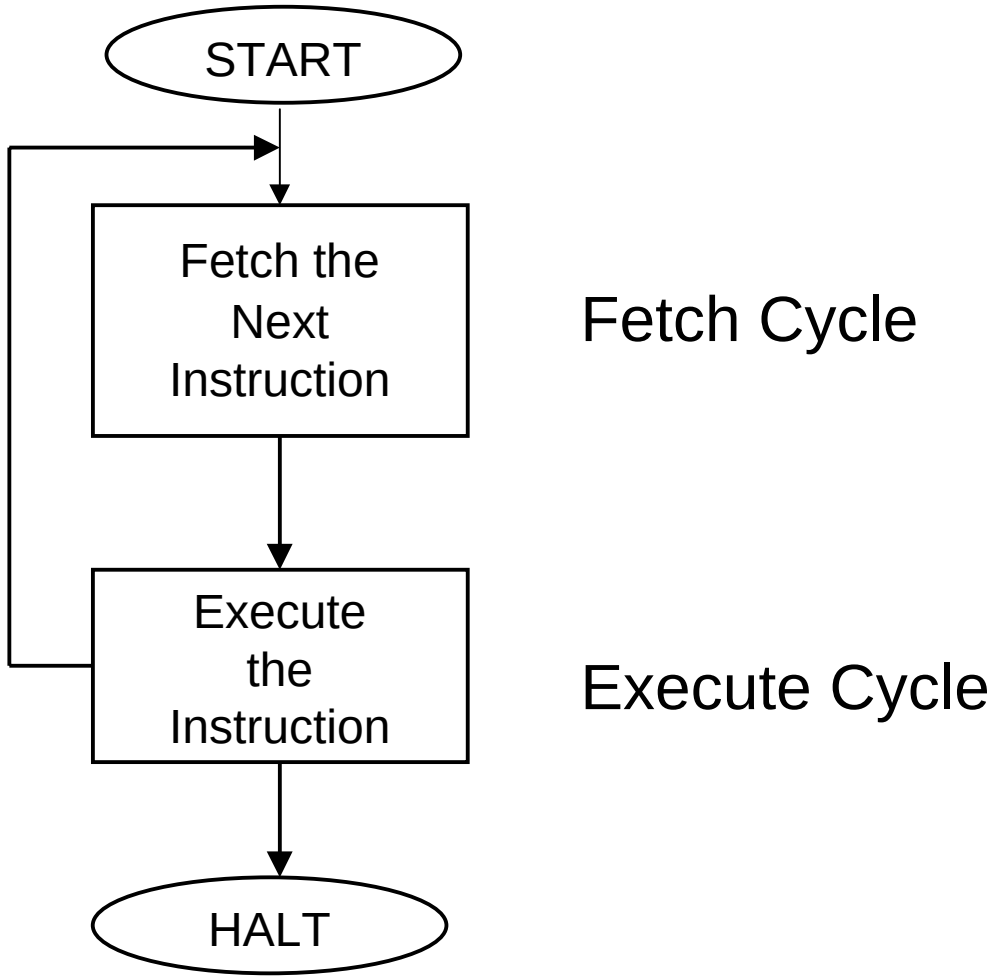
iii) Read the data from the data bus

The Execution Cycle consists of

i) Decode the instruction and generate the correct sequence of internal and external signals

ii) Execute the instruction and restart the Fetch Cycle

Basic Instruction Cycle



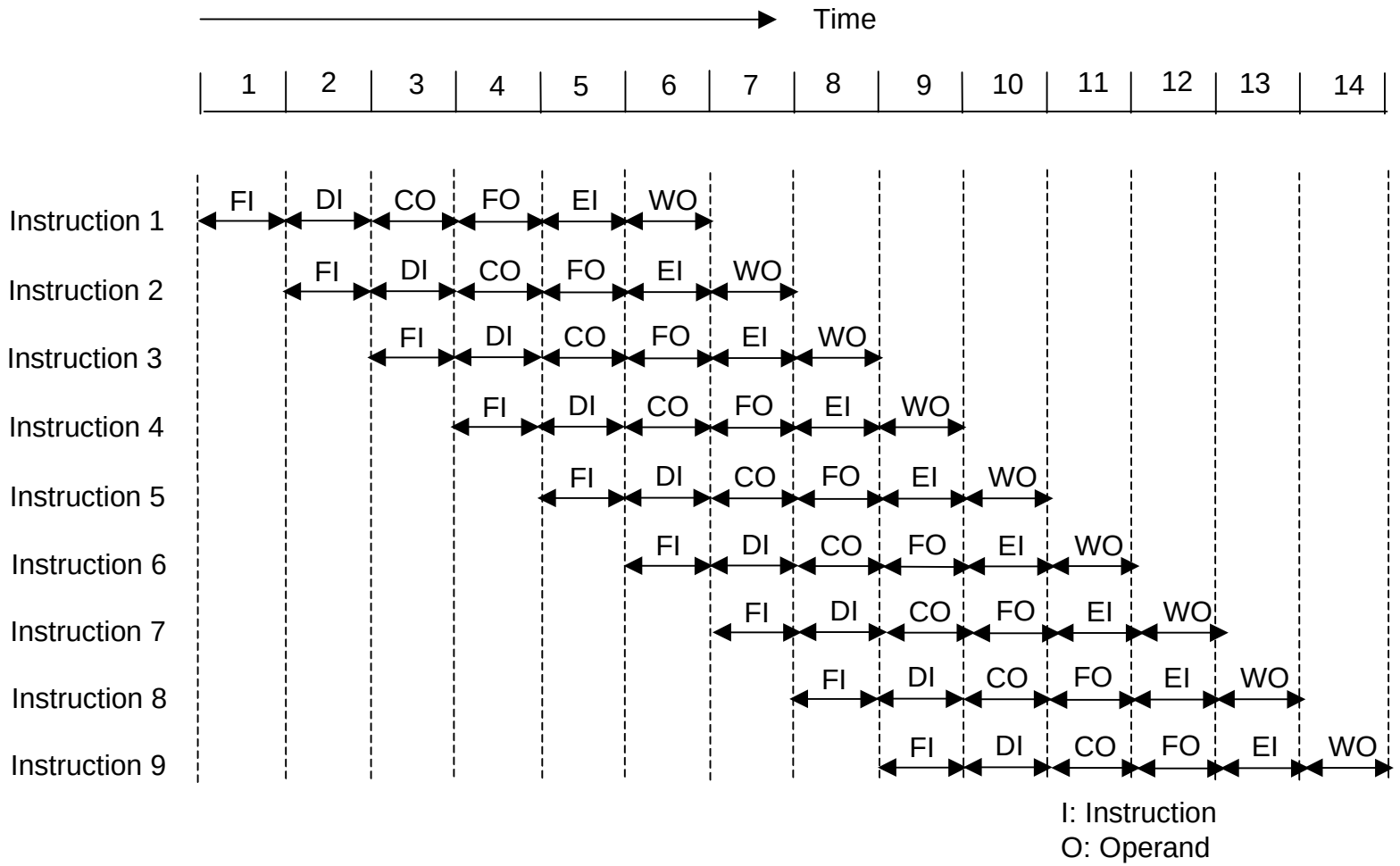
Pipelined Instruction Fetch and Execution Cycles

Instruction Fetch and Execution pipeline

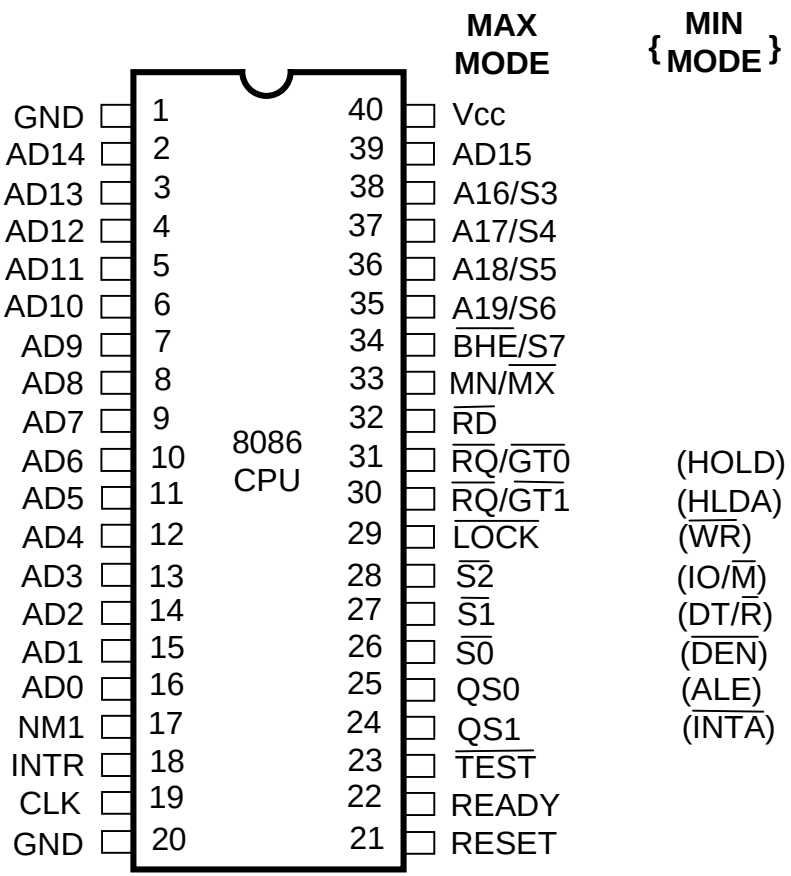
Fetch	Execute	Fetch	Execute	Fetch	Execute	Fetch	

- **Bus Interface Unit (BIU)** fetches instructions from memory, passes the instruction to the instruction stream byte queue and starts to fetch the next instruction immediately
- **Execution Unit (EU)** removes instructions from the instruction queue
- Both BIU and EU may be working simultaneously in time (pipelined parallel processing)

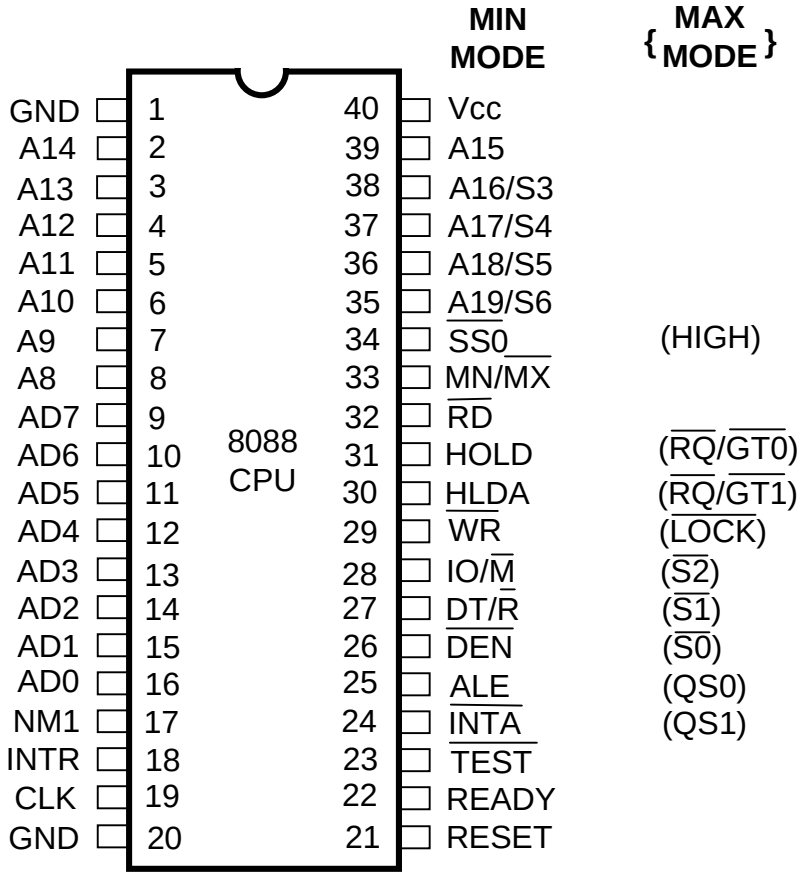
Timing Diagram for Instruction Pipeline Operation



Introduction to Intel 8086/8088 Microprocessors



8086 pin diagram



8088 pin diagram

Introduction to Intel 8086/8088 Microprocessors

8088 and 8086 are almost identical except that 8088 has only 8 external data lines whereas the 8086 has 16 external data lines.

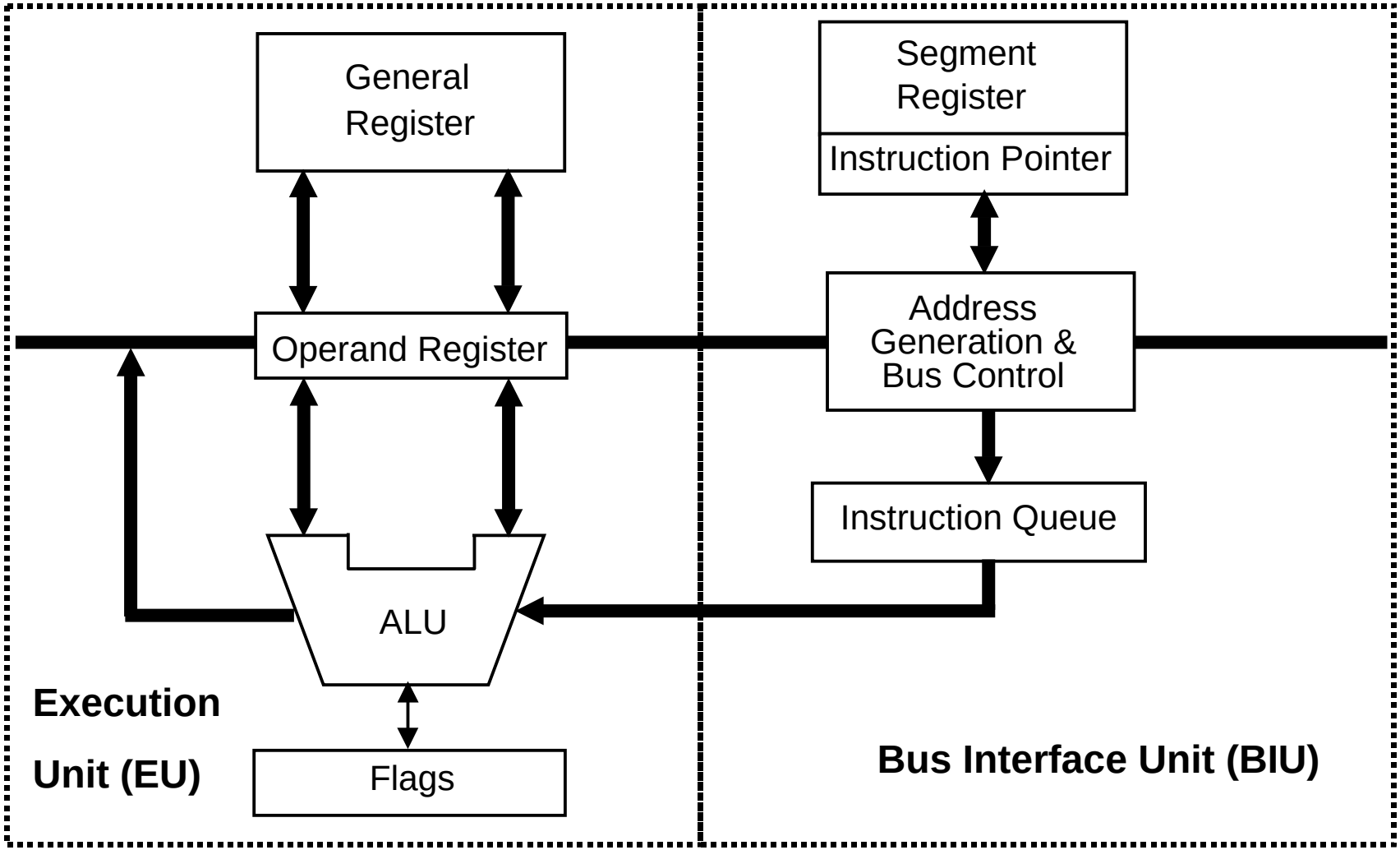
Both have

- 16 bit wide data bus internally
- 20 address pins (16 address/data + 4 address/status) allowing a maximum memory address range of 1MByte
- multiplexed address/data pins (8088 only multiplexes 8 pins)
- 2 modes of operation (maximum and minimum mode)
- Same instruction set

Internal Architecture of the 8088

- Both 8088/8086 employ *parallel processing.*
- Contains two processing units: *Execution unit* (EU) and *Bus interface unit* (BIU); operate at the same time.
- The BIU sends out addresses, fetches instructions from memory, reads data from ports and memory, and writes data to ports and memory, i.e. *the BIU handles all transfers of data and addresses on the buses for the execution unit*.
- The EU tells BIU where to fetch instruction or data from, decodes instructions, and executes instructions.

Internal Architecture of the 8088



8086 Internal Block Diagram

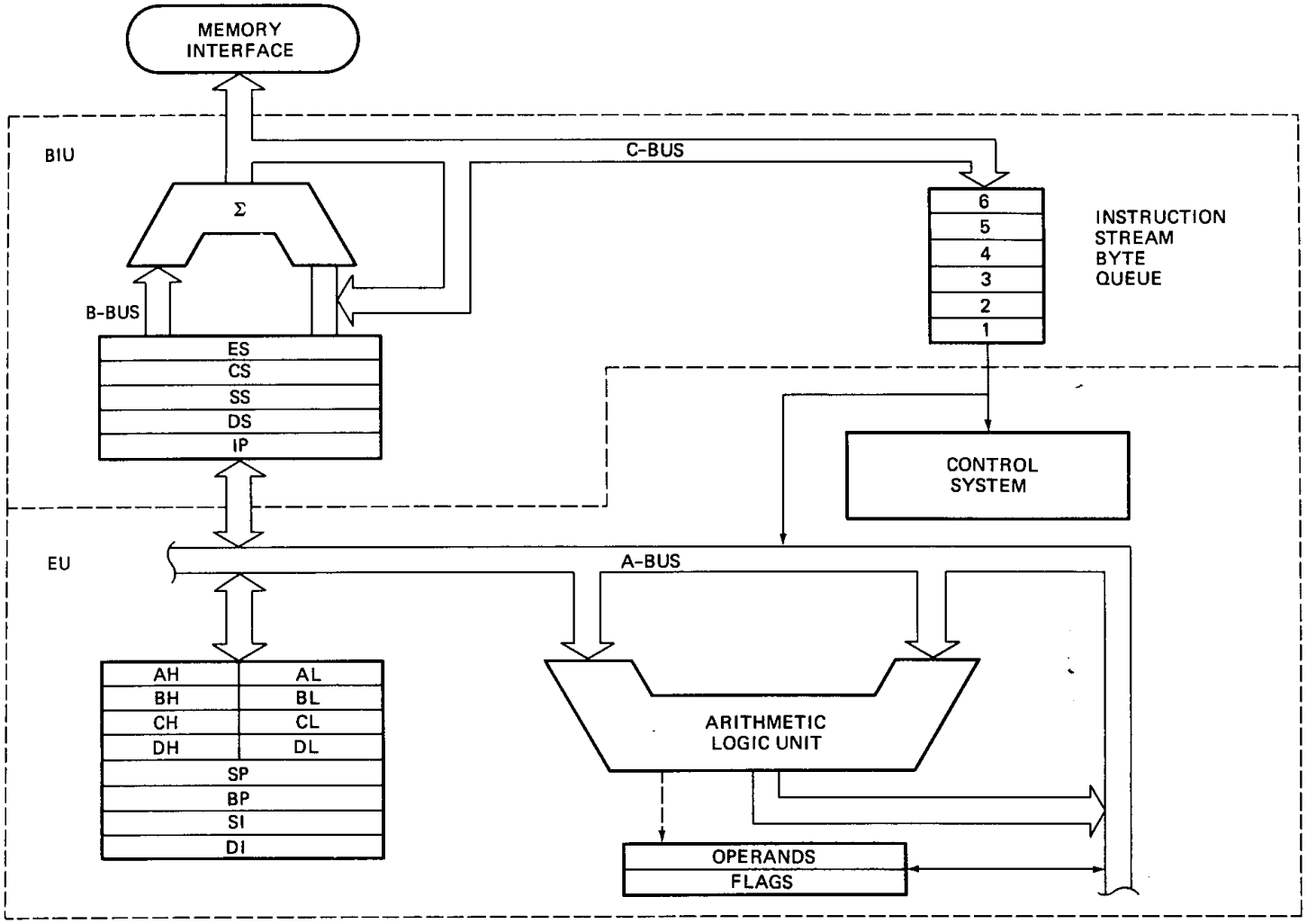


FIGURE 2-7 8086 internal block diagram. (*Intel Corp.*)

Bus Interface Unit (BIU)

- Perform bus operation such as instruction fetching, reading/writing of data operand for memory, inputting/outputting data for I/O peripherals.
- Perform other functions such as instruction queuing and data acquisitions.
- 8-bit (16-bit) bi-directional data bus for 8088 (8086).
- 20-bit address bus → can address any one of the 2^{20} (1,048,576) bytes.
- Contain *segment register*, *instruction pointer*, *address generation adder*, *bus control logic*, and an *instruction queue*.
- Use *instruction queue* to implement a *pipelined architecture* (prefetch up to 4 (6) bytes of instruction code for 8088 (8086) and then store and access the codes in FIFO order).
- See Ch9 for the detail discussion on instruction set and segment registers.

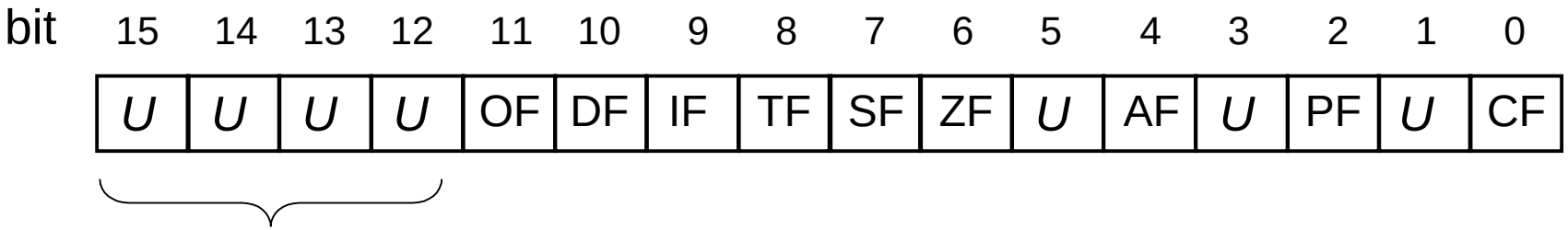
Execution Unit (EU)

- Responsible for decoding and executing instruction.
- Contains: *arithmetic logic* unit (ALU), status and control flags, general purpose registers, and temporary-operand register.
- EU access the instruction from output end of the instruction queue and data from general-purpose register.
- It reads one instruction at a time, decodes them, generates operand address if necessary, passes them to BIU and request to perform the read/write cycle to memory or I/O, and performs the operation specified by the instruction on operand.
- During execution, EU may test the status and control flags and update these flags based on the results of execution.

Flag Registers

- The flags indicate the condition of the microprocessor as well as controlling its operations.
- A flag register is a flip-flop which indicates some conditions produced by the execution of an instruction or controls certain operations of the EU. A 16-bit flag register in the EU contains nine active flags.
- *conditional flags:* Six flags are *conditional flags*. They are set or reset by the EU on the basis of the results of some arithmetic operation.
- *control flags* : The three remaining flags in the flags register are used to control certain operations of processor. They are called the *control flags*.

Flag Registers



Carry Flag (CF)- set by carry out of MSB.
Parity Flag (PF)- set if result has even parity.
Auxiliary carry Flag (AF)- for BCD
Zero Flag (ZF)- set if results = 0
Sign Flag (SF) = MSB of result
TF- single step trap flag
IF- interrupt enable flag
DF- string direction flag
Overflow Flag (OF)- overflow flag

Conditional Flags

- **carry flag (CF)-** indicates a carry after addition or a borrow after subtraction, also indicates error conditions.
- **parity flag (PF)-** is a logic "0" for odd parity and a logic "1" for even parity.
- **auxiliary carry flag (AF)-** important for BCD addition and subtraction; holds a carry (borrow) after addition (subtraction) between bits position 3 and 4. Only used for DAA and DAS instructions to adjust the value of AL after a BCD addition (subtraction).
- **zero flag (ZF)-** indicates that the result of an arithmetic or logic operation is zero.
- **sign flag (SF)-** indicates arithmetic sign of the result after an arithmetic operation.
- **overflow flag (OF)-** a condition that occurs when signed numbers are added or subtracted. An overflow indicates that the result has exceeded the capacity of the machine.

Control Flags

- The control flags are deliberately set or reset with specific instructions YOU put in your program. The three control flags are:
  - **trap flag (TF)** - used for single stepping through a program;
  - **interrupt flag (IF)** - used to allow or prohibit the interruption of a program;
  - **direction flag (DF)** - used with string instructions.

- No specific instruction to set TF. See example 11-1 in Brey's for more details.

General-Purpose Registers

- EU has eight 8-bit *general-purpose registers*, labeled AH, AL, BH, BL, CH, CL, DH, DL. These registers can be used individually for temporary storage of 8-bit data.
- Register pairs AH-AL, BH-BL, CH-CL, and DH-DL can be used together to form register AX, BX, CX, and DX and can be used to store 16-bit data words.
- The AL register is also called the *accumulator*. It has some features that the other general-purpose registers do not have.
- The advantage of using internal registers is that it can be accessed more quickly than from external memory. No memory reference or memory cycle is needed to get the data.