

Optical Heart Rate Detection Sensor

General Description

The PAHEI-2GEI-2G is a high performance and low power CMOS-process optical sensor with Green LED and DSP integrated serving as a Heart Rate Detection (HRD) sensor. It is based on optical technology which measures the variation of human blood movement in the vessel.

Key Features

- Heart rate detection function (HRD)
- Ultra-low power consumption, power saving mode during time of no touch movement
 - LPT sleep1
 - LPT sleep2
- Flexible sleep rate control
- Flexible communication interface
 - I²C
 - 4-wire SPI
 - 2-wire SPI
- I²C interface up to 1 Mbit/s
- SPI interface up to 1 Mbit/s
- Hardware reset support
- Hardware power down support
- Integrated chip-on-board LED with wavelength of 525nm

Key Sensor Performance

Parameter	Value
Max. frame rate	3000 fps
	VDDM: 3.0~3.6V
	VDDIO: 1.62~3.6V
Supply voltage	
Supply voltage	Note: suggest customer could
	consider 3.3V to avoid voltage
	drop issue.
	1.5 mA at Normal mode
	160 uA at Sleep1 mode
	40 uA at Sleep2 mode
Power consumption	15uA at power down mode
	Note: including LED current, w/o I/O
	toggling, package only
Operating temperature	-20 to +60 °C
(at junction)	
Package	Land Grid Array. Size 3.0 x 4.7 mm
r wertage	with 16 pins

Applications

- Healthcare on wearable device
- Photoplethysmogram waveform

Ordering Information

	Part Number	Packing	Description
ſ	PAH8001EI-2G	16-Pin LGA	CMOS HRD optical sensor



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Block Diagram

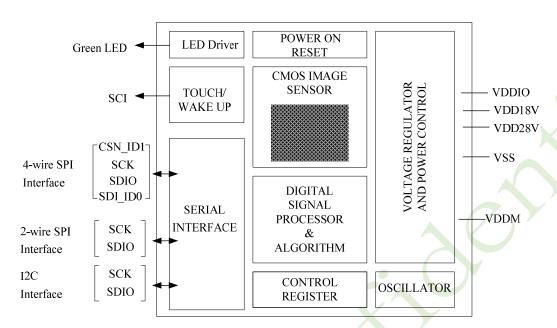


Figure 1. Functional Block Diagram



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Pin Configuration

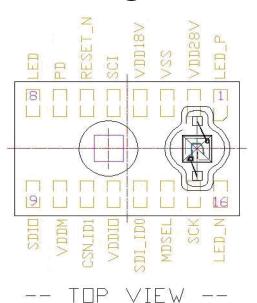


Figure 2. Pin Configuration

Pin No.	Name	Туре	Description
1	LED P		LED Anode
1	LED_P		Provide VDDM supply voltage
2	VDD28V	PWR	Analog circuit power regulator output Must connect 0.1uF capacitor to GND
3	VSS		GND
4	VDD18V	PWR	Analog and digital circuit power regulator output Must connect 0.1uF capacitor to GND
5	SCI	OUT	Touch on/off INT (Active high)
6	RESET_N	IN	Hardware control to enter reset mode Level High: leave reset mode Level Low: enter reset mode Set to high when not used
7	PD	IN	PD: Hardware control to enter power down mode Build-in 1M ohm pull-down resistor Level High: enter power down mode Level Low: leave power down mode Set to low when not used
8	LED		LED driver connection Must connect to LED N
9	SDIO	IN/OUT	4-wire SPI: data output pin 2-wire SPI: data in-out pin I2C: data in-out pin
10	VDDM	PWR	Power supply (3.0v~3.6v) for internal power regulator
11	CSN_ID1	IN	4-wire SPI: chip select, active low I2C: address set ID1(Tri state IO)
12	VDDIO	PWR	I/O power supply. VDDIO: 1.62V~3.6V
13	SDI_ID0	IN	4-wire SPI: data input pin I2C: address set ID0(Tri state IO)
14	MDSEL	IN	Tri state IO For select 2-wire SPI/ 4-wire SPI/ I2C mode I2C: Pull down 4-wire SPI: Floating 2-wire SPI: Pull high(Tied to VDDIO)
15	SCK	IN	2-wire SPI/ 4-wire SPI/ I2C: clock pin
16	LED_N		LED Cathode Must connect to LED



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Package Outline Dimension and Recommend Layout PCB

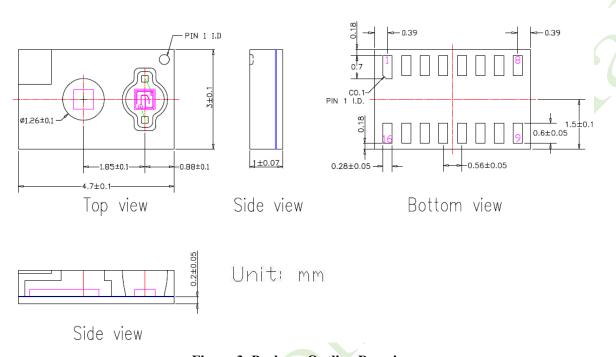


Figure 3. Package Outline Drawing

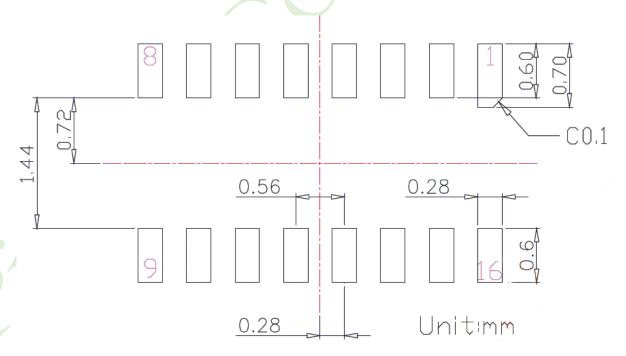


Figure 4. Recommend Layout PCB



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Reference Application Circuit

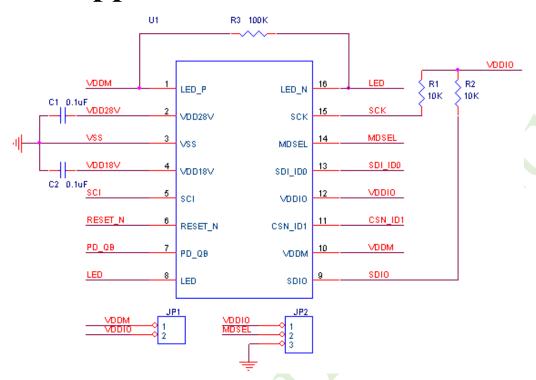


Figure 5. Application Circuit

Design Notes:

- 1. VDDM & VDDIO: 3.0V~3.6V (3.3V System) --> JP1 Short
- 2. VDDM: 3.0V~3.6V, VDDIO: 1.62V~1.98V (1.8V System) --> JP1 Open
- 3. R1, R2 10K for I2C Only
- 4. VDD28V, VDD18V must be connected 0.1uF capacitor to GND
- 5. SCI can connect to MCU HW INT as Touch INT for power saving (Active high)
- 6. VDDM and VDDIO power noise need to under 100mV
- 7. MDSEL of JP2 tied to VDDIO for 2SPI, floating for 4SPI, and tied to GND for I2C
- 8. ID0 and ID1 can directly bond to VDDIO or GND based on your I2C ID selection
- 9. LED pin must be pulled high 100K resistor to VDDM for internal circuit voltage reference

PCB Layout Guide

- 1. 0.1uF Capacitors of VDD18V and VDD28V must be closed to 8001.
- 2. If SDI ID0 and CSN ID1 (I2C ID selection) are floating, please don't close to any clock trace.
- 3. Trace width of VDDM/VDDIO/VDD28V/VDD18V/LED P/LED N/LED must be at least 8 mil.



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Absolute Maximum Ratings, T = 25°C

Description	Symbol	Min.	Max.	Unit
DC Supply Voltage	V _{DDM} _MAX	-0.4	VDDM + 0.3	V
I/O Voltage	V _{DDIO} _MAX	-0.4	VDDIO + 0.3	V
I/O Pin Input High Voltage (All I/O pin)	V_{DDIO} In	-0.4	VDDIO + 0.3	V
ESD, human body model	ESD _{HBM}	-	2	KV

^{*}Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

Recommended Operating Condition

Description	Symbol		Min.	Typ.	Max.	Unit
Operation Temperature	Тот		-20	25	60	°C
Power Supply Voltage	$V_{ m DDM}$		3.0	3.3	3.6	V
IO Supply Voltage	V _{DDIO}		1.62	3.3	3.6	V
Supply Noise (Peak to peak within 10K – 80 MHz)	$ m V_{Npp}$		-	-	100	mV
Carial Clash Eraguanay	SCK	SPI	-	-	1000	KHz
Serial Clock Frequency	SCK	I ² C	-	400	1000	КПХ

Note: For power supply voltage, suggest customer could consider 3.3V to avoid voltage drop issue and increase human skin coverage.

Thermal Information

Description	Symbol	Min.	Тур.	Max.	Unit
Storage Temperature	T _{STG}	-40	-	85	°C
Lead-free Temperature, Surface-mount Process	Tsol	-	245	-	°C

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AC Operating Condition

Electrical Characteristics are defined under recommended operating conditions. Typical values at 25 °C, VDDIO =

3.3V for 3.3V application and VDDIO = 1.8 V for 1.8V application.

Symbol	Parameter	Min.	Тур.	Max.	Unit	Notes
tpdr	PD Pulse Register	-	-	1.9	ms	2 frames time maximum after setting PD_enh bit in the Configuration register
$t_{ m PU}$	Power Up from V _{DD} ↑	10	-	38	ms	From V _{DD} ↑ to valid touch signals.
T_{HOLD}	SDIO Read Hold Time	-	3	-	us	Minimum hold time for valid data.
$t_{ m delay}$	Address and data delay time	2.75			us	Refer to Serial Interface section
tresync	Serial Interface RESYNC.	1	-	-	us	Refer to Serial Interface section
tsiwtt	Serial Interface Watchdog Timer Timeout	1	1 18 96	-	ms	2/4 wire SPI: Refer to Serial Interface section 1 ms for normal mode, 18 ms for sleep1 and 96 ms for sleep2 mode
tWAKE1	Waking from Sleep1 Mode	10	18	27	ms	@Slp1_freq 18 ms
tWAKE2	Waking from Sleep2 Mode	10	96	144	ms	@Slp2_freq 96 ms
tswkint	Sensor Wakeup Interrupt Time	-	310	-	us	
tr, tf	Rise and Fall Times: SDIO	-	30	-	ns	$C_L = 30 \text{ pF}$

DC Electrical Characteristics

Electrical Characteristics are defined under recommended operating conditions. Typical working temperature is 25 °C. VDDIO=1.8~3.3V+/-5%.

Symbol	Parameter	Min.	Тур). I	Max.	Unit)	Notes
Type: Po	wer							
I_{DDHRD}	Supply Current for Chip at HRD (Normal)	1.05			3.0	mA	No	including LED current, w/o SPI interface I/O toggle
I _{DDS1}	Supply Current for Chip (Sleep1)	-	120)	240	uA	No	including LED current, w/o SPI interface I/O toggle
I _{DDS2}	Supply Current for Chip (Sleep2)	-	30		60	uA	No	including LED current, w/o SPI interface I/O toggle
Iddpd	Supply Current for Chip (Power Down)	-	15		45	uA		
I _{LEDHRD}	Supply Current for LED at HRD (Normal)	5	0.43	5	1.8	mA	@L	ED_Step = 5, depend on human factor
I _{LEDS1}	Supply Current for LED (Sleep1)	-	40		160	uA	@L	ED_Step = 5, Slp1_freq 18 ms, depend on human factor
ILEDS2	Supply Current for LED (Sleep2)	-	10		40	uA	@L	ED_Step = 5, Slp2_freq 96 ms, depend on human factor
I _{INRUSH}	Inrush Current	-	-		60	mA	VD	DM/VDDIO/VDD18V/VDD 28V with 0.1uF
Type: IO								
V_{IH}	Input Voltage HIGH	0.7VD	DIO	-	VDD	10+0.4	V	
17	Innet Veltore LOW	-0.4	4	-	0.	48	V	$@VDDIO \ge 1.7V$
V_{IL}	Input Voltage LOW	-0.4	4	-	0.	0.44		$@VDDIO \ge 1.62V$
VoH	Output Voltage HIGH	VDDIC	0-0.4	-	VDDIO+0.4		V	@I OH = 2mA
Vol	Output Voltage LOW	-0.4	4	-	0.4 V $@I_{OL} = 2mA$			
Type: LF	ED							
ILED	Sink current	4.5	5	9.0	13	13.5 mA @LED Step = 5		
VLED-	LED cathode voltage	0.6	ó		VDDI	10+0.3	V	At LED register setting of 9.0mA



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Serial Interface Communication

The synchronous serial port is used to set and read parameters in the sensor.

1. Two-Wire SPI Interface (For PAH8001EI-2G)

SCK: The serial clock line. It is always generated by the host micro-controller.

SDIO: The serial data line used for write and read data.

1.1. Transmission Protocol

The transmission protocol is a two-wire link, half duplex protocol between the micro-controller and sensor. All data changes on SDIO are initiated by the falling edge on SCK. The host micro-controller always initiates communication; the sensor never initiates data transfers.

The transmission protocol consists of the two operation modes:

- Write Operation.
- Read Operation.

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has a bit7 as its MSB to indicate data direction. The second byte contains the data. Timing between two bytes is no more than T_{SIWIT} .

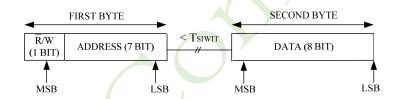


Figure 6. Two-wire SPI Transmission protocol

1.2. Write/Read Operation

Write Operation

A write operation, which means that data is going from the micro-controller to the sensor, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The transfer is synchronized by SCK. The micro-controller changes SDIO on falling edges of SCK. The sensor reads SDIO on rising edges of SCK.

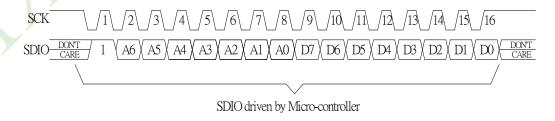


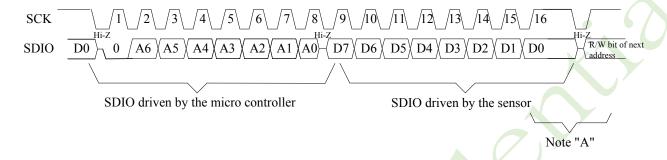
Figure 7. Two-wire SPI Write operation



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Read Operation

A read operation, which means that data is going from the sensor to the micro controller, is always initiated by the micro controller and consists of two bytes. The first byte contains the address, is written by the controller, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the sensor. The transfer is synchronized by SCK. SDIO is changed on falling edges of SCK and read on every rising edge of SCK. The controller must go to a high Z state after the last address data bit.



Note "A" 1. The sensor sends data to the micro controller.

2. The sensor releases and set SDIO to Hi-Z as the falling edge of the SCLK



Note "B" 1. The Host controller sends address to the sensor.

2. The Host controller releases and set SDIO to Hi-Z after the last address bit.

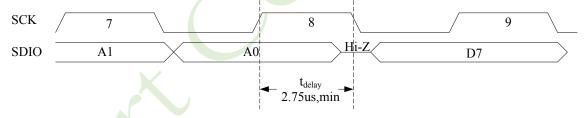


Figure 8. Two-wire SPI Read Operation



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2. Four-Wire SPI Interface (For PAH8001EI-2G)

CSN_ID1 : Chip select line, active low(Generally named SPI_CS). SCK : Serial clock line, generated by the host controller.

CSN_ID0: Serial data line, used to write data to sensor(Generally named MOSI). **SDIO**: Serial data line, used to read data from sensor(Generally named MISO).

2.1. Transmission Protocol

The transmission protocol is a 4-wire link, half duplex protocol between the micro-controller and the sensor. All data changes on SDI_ID0/SDIO are latched at SCK rising edge. The host controller always initiates communication and the sensor never initiates data transfers.

The transmission protocol consists of the two operation modes:

- Write Operation.
- Read Operation.

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has a bit 7 as its MSB to indicate data direction. The second byte contains the data.

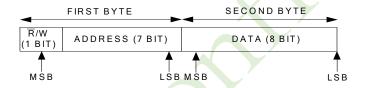


Figure 9. Four-wire SPI Transmission protocol

2.2. Write/Read Operation

Write Operation

A write operation, which means that data is going from the host controller to the sensor, is always initiated by the controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The transfer is synchronized by SCK. The controller changes SDI ID0 at SCK falling edges. The sensor reads SDI ID0at SCK rising edges.

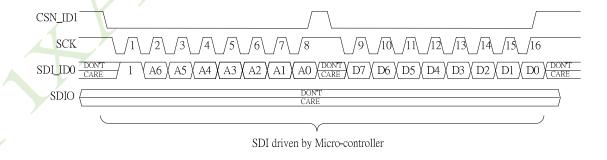


Figure 10. Four-wire SPI Write operation



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Read Operation

A read operation, which means that data is going from the sensor to the controller, is always initiated by the HOST controller and consists of two bytes. The first byte contains the address, is written by the controller, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the sensor. The transfer is synchronized by SCK.

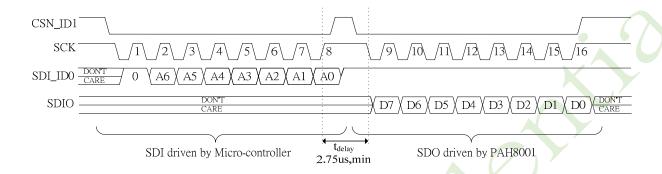


Figure 11. Four-wire SPI Read Operation

2.3. Timing Spec

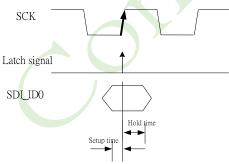


Figure 12. SPI Timing Spec

Symbol	Parameter	Min	Max	Unit
Setup time	Serial Host Write data bus setup time	1/8T		ns
Hold time	Serial Host Write data bus hold time	1/4T		ns

Note: $T = SPI \ clock \ (SCK)$



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3. I²CTM Interface (For PAH8001EI-2G)

SCK : Serial clock line, generated by the host controller(Generally named SCL).
SDIO : Serial data line, used to read data from sensor(Generally named SDA).

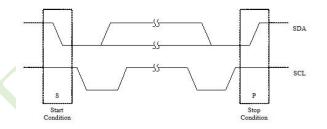
PAH8001EI-2G supports I2C bus transfer protocol and acts as slave device. The 7-bits selectable slave address is depending on SDI ID0 and CSN ID1 input pin state and supports receiving / transmitting speed as maximum 1MHz.

Table 1. I2C Slave Address

SDI_ID0	CSN_ID1	7-bit slave address (hex)
Low	Low	33
Low	High	37
Low	Floating	3b
High	Low	53
High	High	57
High	Floating	5b
Floating	Low	63
Floating	High	67
Floating	Floating	6b

3.1. Bus Overview

- Only two wires SDIO (serial data) and SCK (serial clock) carry information between the devices connected to the I2C bus. Normally both SDIO and SCK lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiate a transfer (start condition), generates clock signals, and terminates a transfer (stop condition).
- Start and stop condition: A high to low transition of the SDIO line while SCK is high defines a start condition. A low to high transition of the SDIO line while SCK is high defines a stop condition. Please refer to Figure 12.
- Valid data: The data on the SDIO line must be stable during the high period of the SCK clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 13.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge: The receiving device should pull down the SDIO line during high period of the SCK clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.





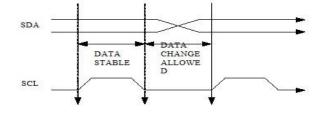


Figure 14. Valid Data



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3.2. Data Transfer Format

Master transmits data to slave (Write Cycle)

S: Start.

A: Acknowledge by salve.

P: Stop.

RW: The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 - Read cycle, RW = 0 - Read cycle.

SUBADDRESS: The address values of PAH8001EI-2G internal control registers.

During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDIO line. After slave (PAH8001EI-2G) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDIO line. Again follow the PAH8001EI-2G acknowledgment, the master places the 8 bits data on SDIO line and transmit to PAH8001EI-2G control register (address was assigned by 2nd byte). After PAH8001EI-2G issue acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAH8001EI-2G sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAH8001EI-2G can be programming via this way.

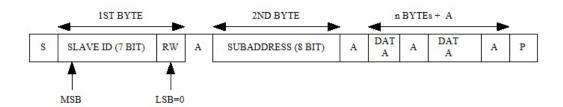


Figure 15. I²C Write cycle



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Slave transmits data to master (read cycle)

The sub-address was taken from previous write cycle.

The sub-address is automatically increment after each byte read.

Am: Acknowledge by master.

Note there is no acknowledgment from master after last byte read.

During read cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDIO line. After issue acknowledgment, 8 bits DATA was also placed on SDIO line by PAH8001EI-2G. The 8 bits data was read from PAH8001EI-2G internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAH8001EI-2G place the next 8 bits data (address is increment automatically) on SDIO line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDIO line high. The slave (PAH8001EI-2G) must releases SDIO line to master to generate STOP condition.

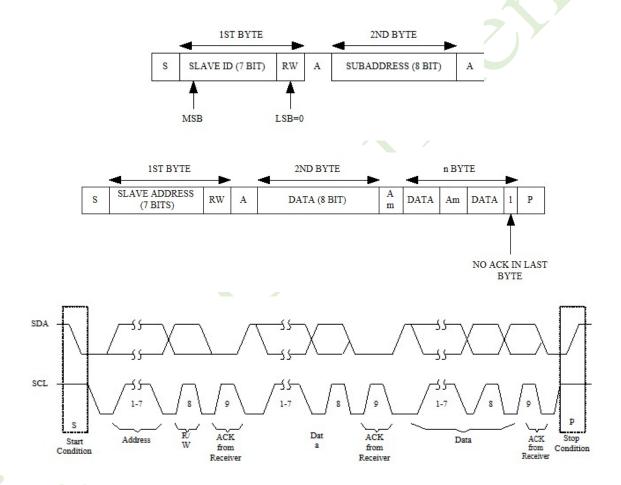


Figure 16. I²C Read cycle



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3.3. Bus Timing Specification

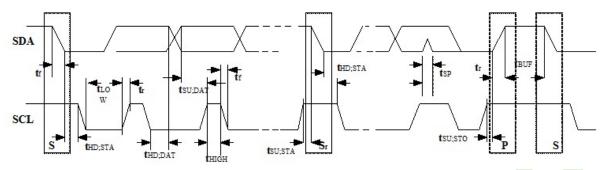


Figure 17. I²C bus timing

Parameter		Standar	d Mode	T India
Parameter	Symbol	Min.	Max	Unit
SCK clock frequency.	f_{scl}	10	1000	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	t _{HD:STA}	4.0	-	μs
Low period of the SCK clock.	t_{LOW}	4.7	-	μs
High period of the SCK clock.	thigh	0.75	-	μs
Set-up time for a repeated START condition.	tsu;sta	4.7	•	μs
Data hold time. For I2C-bus device.	thd;dat	0	3.45	μs
Data set-up time.	tsu;dat	250	1	ns
Rise time of both SDIO and SCK signals.	$t_{\rm r}$	30	N.D.	ns (notel)
Fall time of both SDIO and SCK signals.	ťŕ	30	N.D.	ns (notel)
Set-up time for STOP condition.	tsu;sto	4.0	-	μs
Bus free time between a STOP and START.	t _{BUF}	4.7	1	μs
Capacitive load for each bus line.	Cb	1	15	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V _{nH}	0.2 VDD	-	V

Note: It depends on the "high" period time of SCK.

4. Error Detection

- 1. The controller can verify success of write operations by issuing a read command to the same address and comparing written data to read data.
- 2. The controller can verify the synchronization of the serial port by periodically reading the product ID register (0x00) to check the data (0x30).



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5. Re-Synchronous Serial Interface

If the controller and the sensor get out of synchronization, then the data either written or read from the registers will be incorrect. In such case, one way to solve this mis-match is to toggle the SCK line from high to low for least t_{RESYNC}, and then MUST toggle it from low to high to wait at least t_{SIWTT} to reach re-synchronous the serial port. This method is called by "watchdog timer timeout". The sensor will reset the serial port without resetting the registers and be prepared for the beginning of a new transmission.

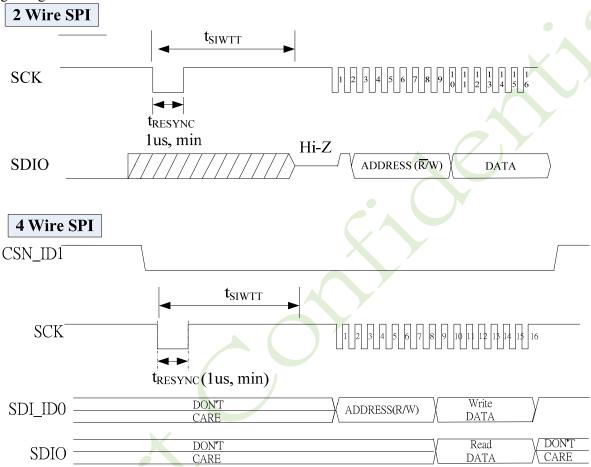


Figure 18. Re-synchronous Serial Interface Using Watchdog Timer Timeout

Note that this function is disabled when the sensor is in the power down mode. If the user uses this function during the power down mode, it will get out of synchronization. The sensor and the HOST controller also might get out of synchronization due to following conditions.

- Power On Problem The problem occurs if the sensor powers up before the HOST controller sets the SCK and SDI_ID0 lines to be output. The sensor and the controller might get out of synchronization due to power on problem. The way to solve this issue is to use "watchdog timer timeout".
- ESD Events The sensor and the HOST controller might get out of synchronization due to ESD events. "watchdog timer timeout" is one way to recover.



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6. Power Down Mode

Software Power Down

The sensor can be placed in a power-down mode by setting **PD_enh** bit in the **Configuration** register via a serial port write operation. After setting the **Configuration** register, wait at most 2 frames times. To get the chip out of the power down mode, clear **PD_enh** bit in the **Configuration** register via a serial port write operation. In the power down mode, the serial interface watchdog timer (see Section 4.4) is not available. But, the serial interface still can read/write normally. For an accurate report after leave the power down mode, wait about 3ms before the HOST controller is able to issue any write/read operation to the sensor.

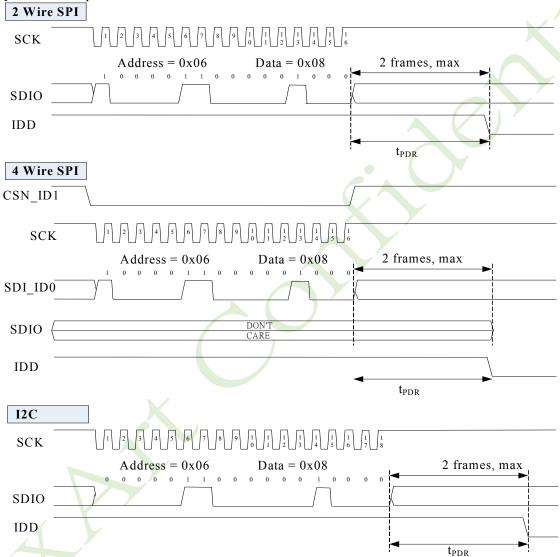


Figure 19. Power-down Configuration Register Writing Operation

Hardware Power Down

The sensor can be placed in a power-down mode by setting **PD** pin at **High-level**. After setting the pin, wait at most 2 frames times. Give it a Low-level to exit power down status. In the power down mode, the serial interface watchdog timer (see Section 4.4) is not available. But, the serial interface still can read/write normally. For an accurate report after leave the power down mode, wait about 3ms before the HOST controller is able to issue any write/read operation to the sensor.

Optical Heart Rate Detection Sensor

Operation Guide

1. Sleep Mode Timer

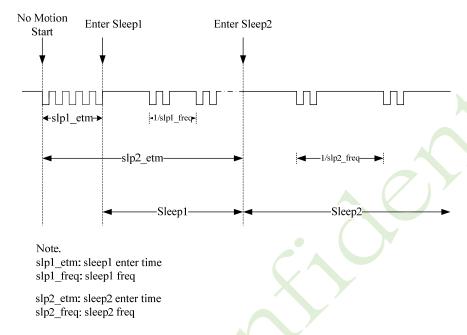


Figure 20. Sleep Mode Timer diagram

2. Touch INT Function (HW SCI Pin)

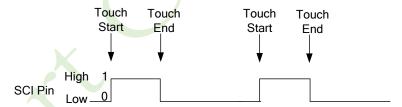


Figure 21. Touch Timer diagram

3. Auto Exposure (AE) Function

AE Enable (Default): If frame average is under 100 or over 200, sensor will control LED exposure time (10us~160us) automatically to let frame average into the range.

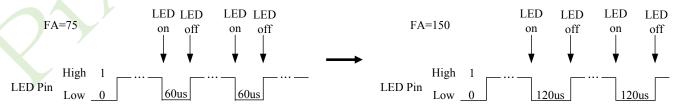


Figure 22. AE Function

AE Disable: Sensor will be fixed LED exposure time (60us) no matter frame average.



Optical Heart Rate Detection Sensor

4. Heart Rate Detection

Heart rate detection is an optical measurement technique that uses a light source and a detector to detect cardio-vascular pulse wave that propagates through the body. The detected signal (pulse wave) called photoplethysmography and its acronym in some literature, is (PPG/PTG). The PPG signal reflects the blood movement in the vessel, which goes from the heart to the fingertips through the blood vessels in a wave-like motion. Therefore, we can use this PPG signal to calculate heart rate.

This optical based technology could offer significant benefits to healthcare, e.g. noninvasive, accurate and simple-to-use.

Applications

- Heart Rate for general healthcare (Perfusion Index : Typ.1%)
- Photoplethysmogram Waveform

Heart Rate Detection Performance

Platform	PAH8001EI-2G					
Heart rate measurement range	30 to 210 beats per minute (bpm)					
Heart rate tolerance	±3 bpm @ Room temperature for steady state ±5 bpm @ Room temperature for motion state					
Response time	8 sec @ HR 72/bpm					

Heart Rate Detection Block Diagram

4.1 System Design for App level

- ➤ Processor to access PPG data from 8001 sensor, then pass it to App level
- APP level apply PixArt provided algorithm library to get heart rate data and waveform

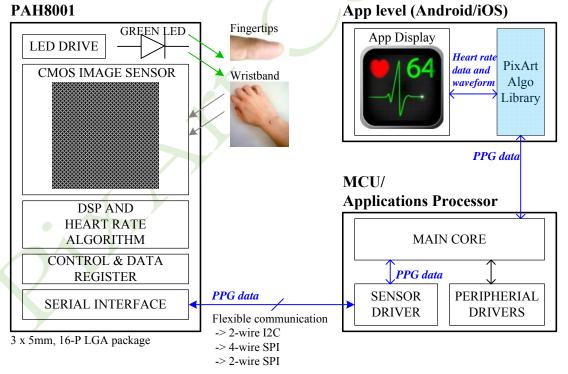


Figure 23. System Design for App level



Optical Heart Rate Detection Sensor

4.2 System Design for Firmware level

- > Processor to access PPG data from 8001 sensor
- > Perform heart rate calculation by PixArt algorithm library, then send result to destiny

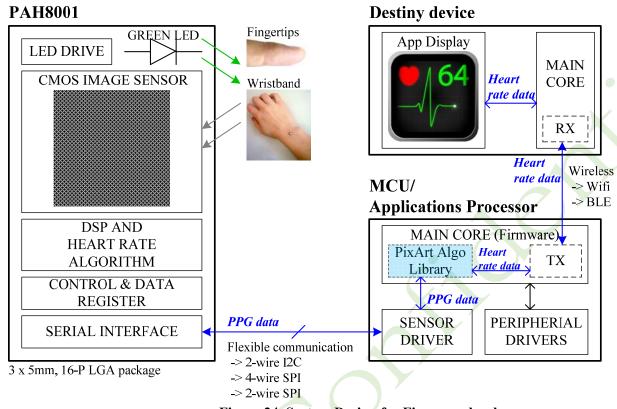


Figure 24. System Design for Firmware level

Note:

PAH8001 provides heart rate measurements. However, it is not a medical device.

To use the heart rate detection sensor on your wrist, finger or palm, you must:

Fasten the sensor snugly makes tight contact with your skin and maintain stable (no motion) while measuring to acquire accurate heart rate. If the sensor does not contact the skin well or have extreme motion while measuring that the heart rate will not be measured correctly.

Sensor's performance is optimized with greater blood flow. On cold days or users have poor circulation (ex: cold hands, fingers and cold feet) the sensor performance (heart rate accuracy) can be impacted because of lower blood flow in the measuring position.



Optical Heart Rate Detection Sensor

Register Table

The optical heart rate detection sensor can be programmed through registers and heart rate relational data can be read from registers. All registers not listed are reserved, and should never be written by firmware. Note that the user should write address 0x09 with 0x5A if he/she would like to modify the value of register. Besides, the user should write address 0x7F with 0x01 if he/she would like to modify the value of Bank1 register and write address 0x7F with 0x00 to return to Bank0.

				Bank0
Address	Name	R/W	Default	Data Type
0x00	Product_ID1	R	0x30	Eight bits[11:4] number with the product identifier
0x01	Product_ID2	R	0xDx	Four bits[3:0] number with the product identifier Reserved[3:0] number is reserved for future use
0x05	Operation_Mode	R/W	0xB8	Bit field
0x06	Configuration	R/W	0x02	Bit field
0x09	Write_Protect	R/W	0x00	Bit field
0x0A	Sleep1 Setting	R/W	0x21	Bit field
0x0B	Enter_Time	R/W	0x37	Bit field
0x0C	Sleep2 Setting	R/W	0x71	Bit field
0x20	AE_EnH	R/W	0x0F	Bit field
0x32	Exposure Time L	R	-	Bit field
0x33	Exposure_Time_H	R	-	Bit field
0x4D	Touch_Resolution	R/W	0x1A	Bit field
0x59	Touch Detection	R	-	Bit field

				Bank1
Address	Name	R/W	Default	Data Type
0x07	SCI_Touch_EnH	R/W	0x08	Bit field
0x1A	HR_Data_Algo_A	R	- /	Eight bits unsigned integer
0x1B	Frame_Average	R	-	Eight bits unsigned integer
0x1C	HR_Data_Algo_C	R		Eight bits unsigned integer
0x23	Touch_TH	R/W	0x28	Bit field
0x25	Touch_TH_S_L	R/W	0x00	Bit field
0x26	Touch_TH_S_H	R/W	0x02	Bit field
0x38	LED_Step	R/W	0xF2	Bit field
0x64	HR_Data_A	R	-	Eight bits unsigned integer
0x65	HR_Data_B	R	-	Eight bits unsigned integer
0x66	HR_Data_C	R	-	Eight bits unsigned integer
0x67	HR_Data_D	R	-	Eight bits unsigned integer
0x68	HR_Data_Ready	R	-	Eight bits unsigned integer



Optical Heart Rate Detection Sensor

Register Function Description

	Bank0										
0x00	Product_ID1 (Read)										
Bit	7	7 6 5 4 3 2 1 0									
Field				PID[1	1:4]						
Usage											

0x01	Product_ID2 (Read)									
Bit	7	6	5	4	3	2	1	0		
Field		PID[[3:0]		VID[3:0]					
Usage	The value in this register can't be changed. PID[3:0] can be used to verify that the serial communications link is OK. VID[3:0] is a value between 0x0 and 0xF, it represents the chip version.									

	Operation_Mode (Read/Write)											
Bit 7 6 5	4	3	2	1	0							
Field 1 0 1	Slp_enh	Slp2_enh	Slp2For	Slp1For	Wakeup							
Usage Operation_Mode register allows the user to chan optional values. Operation_Mode[4:0] "0xxxx" = Disable sleep mode "10xxx" = Enable sleep1 mode¹ "11xxx" = Enable sleep2 mode² "11100" = Force entering sleep2³ "1x010" = Force entering sleep1³ "1x001" = Force wakeup from sleep mode³ Notes: 1. Enable sleep mode, but disable automatic ensleep1 mode. After 1000 ms (typical) not mode until touch detected or wakeup bit asser 2. Enable sleep mode full function. In this case, 3 (typical) not moving during normal mode, the wakeup bit asserted. After 6 sec (typical) not moving during sleep detected or force wakeup to normal mode. No	Operation_Mode[4:0] "0xxxx" = Disable sleep mode "10xxx" = Enable sleep1 mode¹ "11xxx" = Enable sleep2 mode² "11100" = Force entering sleep2³ "1x010" = Force entering sleep1³ "1x001" = Force wakeup from sleep mode³ Notes: 1. Enable sleep mode, but disable automatic entering sleep2 mode. In this case, only 2 modes are available, normal mode and sleep1 mode. After 1000 ms (typical) not moving during normal mode, the sensor will enter sleep1 mode, and keep on sleep1 mode until touch detected or wakeup bit asserted. Note that the entering time depends on the setting of <i>Enter_Time</i> register. 2. Enable sleep mode full function. In this case, 3 modes are available, normal mode, sleep1 mode and sleep2 mode. After 1000 ms (typical) not moving during normal mode, the sensor will enter sleep1 mode and sleep2 mode until touch detected or wakeup bit asserted. After 6 sec (typical) not moving during sleep1 mode, the sensor will enter sleep2 mode, and keep on sleep2 mode until touch detected or force wakeup to normal mode. Note that the entering time depends on the setting of <i>Enter_Time</i> register. 3. Only ONE of these three bits, Slp2For/Slp1For/wakeup, can be set to 1 at a single register write, others MUST be 0. After											
	4. To force entering normal mode, clear <i>Slp_enh/Slp2_enh</i> bit when the sensor is in normal mode; otherwise, in sleep mode, clear											
Slp_enh/Slp2_enh bit, and then assert Wakeu	p bit.											
Notes Field Name Description Dit [7:5] MUST always be 101												
Bit [7:5] MUST always be 101 Sleep mode enable/disable												
Slp_enh Sleep mode enable/disable 0 = Disable												
1 = Enable (Default)												
Automatic enter sleep2 mod	a anabla/digabla											
Slp2 enh 0 = Disable	c chable/ulsable											
1 = Enable (Default)												
Slp2For Force entering sleep2 mode.	Set "1" to enter	leen? and then i	it will be reset to	"0"								
Slp1For Force entering sleep1 mode.												
Wakeup Manual wake up from sleep												



Optical Heart Rate Detection Sensor

0x06			C	onfiguration	(Read/Write)					
Bit	7	6	5	4	3	2	1	0		
Field	Reset	0	0	0	PD_enh	0	1	0		
Usage	The <i>Configuration</i> register allows the user to change the configuration of the sensor. Shown below are the bits, their default values, and optional values.									
Notes	Field Name	Descri	ption							
	Reset			n mode (Defau t"1" will be ful	ilt) I chip reset, then t	he bit will be se	et to "0".			
	Bit [6:4]	MUST	always be 000		•			6/7		
		VA								
	Bit [2:0]	MUST	always be 010)						

0x09				Write_Protect	(Read/Write)						
Bit	7	6	5	4	3	2	1	0			
Field	WP[7:0]										
Usage	Write protect for the register bank $0.00A \sim 0.000$ and $0.00A \sim 0.000$ bank $0.000 \sim 0.000$.										
Notes	Field Name	Descri	Description								
				sable for the addre							
	WP[7:0]		$0x00 = \text{Enable (Default)}$, register bank $0x0A \sim 0x7F$ and bank $10x00 \sim 0x7F$ are read only.								
	$0x5A = Disable$, register bank $0x0A \sim 0x7F$ and bank $10x00 \sim 0x7F$ can be read/written.										

0_0 4	Sleep1 Setting (Read/Write)											
0x0A				Sieepi_Setting	g (Read/Write))						
Bit	7	6	5	4	3	2	1	0				
Field		Slp1_f	req[3:0]	A	0	0	0	1				
Usage	<i>Sleep1_Setting</i> register allows the user to set frequency time for the sleep1 mode.											
Notes	Field Name	Descr	Description									
		Setting	g frequency time	for the sleep1 me	ode.							
		A scal	e is 6ms. Relative	e to its value 0 ~	15, the frequency	y time is $6 \sim 96$ m	S.					
	Slp1_freq[3:0]	Defau	lt is 18ms. (slp1_	freq[3:0] = 0010)							
		If slp1	freq[3:0]=n, the	frequency time	is (n+1)*6 ms.							
		For ex	ample, $n=2$ and t	he frequency tim	e is 18ms.							

0x0B			Enter_Time (Read/Write)							
Bit	7	6 5	4	3	2	1	0				
Field		Slp1_etm[3:0]		Slp2_etm[3:0]							
Usage	Enter_Time register allows the user to set enter time for the sleep1 and sleep2 mode.										
Notes	Field Name	Description	Description								
	Slp1_etm[3:0]		Setting sleep1 enter time. A scale is 250ms. Relative to its value $0 \sim 15$, the frequency time is 250ms ~ 4000 ms. Default is 1000ms. (slp1 etm[3:0] = 0011)								
	Slp2_etm[3:0]	A scale is 750ms. Relati	Setting sleep2 enter time. A scale is 750ms. Relative to its value $0 \sim 15$, the frequency time is 750ms ~ 12000 ms. Default is 6000ms about 6 sec). (slp2 etm[3:0] = 0111)								

0x0C	Sleep2_Setting (Read/Write)									
Bit	7	6	5	4	3	2	1	0		
Field		Slp2_f	req[3:0]		0	0	0	1		
Usage	<i>Sleep2_Setting</i> register allows the user to set frequency time for the sleep2 mode.									
Notes	Field Name	Descr	ption							
		Setting	g frequency tim	e for the sleep2 mo	de.					
		A scal	e is 12ms. Rel	lative to its value	$0 \sim 15$, the freq	uency time is 12	$2 \text{ms} \sim 192 \text{ms}$. Do	efault is 96ms.		
	Slp2_freq[3:0]	(slp2_	freq[3:0] = 011	1)						
	If slp2_freq[3:0]=n, the frequency time is (n+1)*12 ms.									
		For ex	ample, n=7 and	the frequency time	e is 96ms.					



Optical Heart Rate Detection Sensor

0x20	AE_EnH (Read/Write)										
Bit	7	6	5	4	3	2	1	0			
Field	0	0	0 0 1 1 1 AE_Er								
Usage	To Enable/Disable Auto-Exposure (AE) function.										
Notes	Field Name		Description								
			Enable/Disable A	Auto-Exposure	(AE) function.						
	AE_EnH		1 = Enable (Defa	ault), LED expo	sure time (10us~	160us) is auto-ac	ljustment by se	nsor			
			0 = Disable, LEI	D exposure time	e is fixed 60us						

0x32		Exposure_Time_L (Read)									
Bit	7	6	5	4	3	2	1	0			
Field		Exposure_Time[7:0]									
0x33		Exposure_Time_H (Read)									
Bit	7	6	5	4	3	2	1	0			
Field			Reserved[5:0)]			Exposure	Time[9:8]			
Usage	To get exposure time of LED. If value is 32, exposure time is 10us. If value is 512, exposure time is 160us.										

0x4D			Toucl	n_Resolution	n (Read/Writ	te)					
Bit	7	6	5	4	3	2	1	0			
Field	0	0 0 1 Touch_Resolution[3:0]									
Usage	Set Touch_Resolution When Touch_Resoluti Touch_Resoluti Touch_Resoluti	ion = 9, touch in	formation *1/2 formation *1/4	2	Default is 10.						

0x59	Touch_Detection (Read)										
Bit	7	7 6 5 4 3 2 1 0									
Field	Touch_Flag		Reserved[6:0]								
Usage	Touch Flag is 1 meant touch on and is 0 meant touch off.										



Optical Heart Rate Detection Sensor

					Bank1						
0x07				SCI_T	Touch_EnH (F	Read/Write)					
Bit	7	6		5	4	3	2	1	0		
Field	0	0 SCI_Touch_EnH 0 0 1 0 0									
Usage	To Enable/	To Enable/Disable Touch Flag as SCI pin.									
Notes	Field Nam	Field Name Description									
	SCI_Touch	Touch as SCI pin enable/disable 0 = Disable (Default) 1 = Enable When touch, SCI pin is keeping high.									
	When no touch, SCI pin is keeping low.										

0x1A		HR_Data_Algo_A (Read)										
Bit	7	7 6 5 4 3 2 1 0										
Field		HR Data Algo A[7:0]										
Usage	To get heart rate data	get heart rate data for algorithm reference and the range is from 0 to 255.										

0x1B			F	rame_Avera	age (Read)					
Bit	7	6	5	4	3	2	1	0		
Field		Frame Average[7:0]								
Usage	To get current frame a	To get current frame average of brightness and the range is from 0 to 255.								

0x1C		HR_Data_Algo_C (Read)										
Bit	7	7 6 5 4 3 2 1 0										
Field		HR Data Algo C[7:0]										
Usage	To get heart rate data	To get heart rate data for algorithm reference and the range is from 0 to 255.										

0x23		Touch_TH (Read/Write)									
Bit	7	7 6 5 4 3 2 1 0									
Field		TOUCH TH[7:0]									
Usage	To Adjust Touch Thresh	To Adjust Touch Threshold to distinguish touch on and touch off.									

0x25	Touch_TH_S_L (Read/Write)										
Bit	7	7 6 5 4 3 2 1 0									
Field		TOUCH TH S[7:0]									
Usage	To Adjust Touch Threshold of Strong Light to distinguish touch on and touch off under strong light.										
0x26			Touch	TH_S_H (R	ead/Write)						
Bit	7	6	5	4	3	2	1	0			
Field		Reserved[3:0)]	TOUCH TH S[11:8]							
Usage	To Adjust Touch Threshold of Strong Light to distinguish touch on and touch off under strong light.										

0x38		LED_Step (Read/Write)									
Bit	7	6	5	4	3	2	1	0			
Field	1	1	1	LED_Step[4:0]							
Usage	Set LED Step to a	t LED Step to adjust LED current.									
Notes	Field Name	ield Name Description									
		LED	Current Step rang	ge from 0 to 31	.Typical one s	tep is 1.8mA+/-5	0%.				
	LED Step	Defa	alt value is 18 or 3	32.4mA.							
	LED_step	If LED_Step[4:0]=n, the LED Current is n*1.8 mA.									
		For example, n=18 and the LED Current is 32.4mA.									



Optical Heart Rate Detection Sensor

0x64	HR_Data_A (Read)									
Bit	7	7 6 5 4 3 2 1 0								
Field		HR Data A[7:0]								
Usage	To get heart rate data	To get heart rate data and the range is from 0 to 255.								

0x65		HR_Data_B (Read)										
Bit	7	7 6 5 4 3 2 1 0										
Field		HR Data B[7:0]										
Usage	To get heart rate data	get heart rate data and the range is from 0 to 255.										

0x66				HR_Data_0	C (Read)			
Bit	7	6	5	4	3	2	1	0
Field	HR Data C7:0]						7	
Usage	To get heart rate data	and the range is	from 0 to 255.					

0x67				HR_Data_I	D (Read)	. (7		
Bit	7	6	5	4	3	2	1	0
Field	HR Data D[7:0]							
Usage	To get heart rate data	and the range is	from 0 to 255.					

0x68	HR_Data_Ready (Read)									
Bit	7	6	5	4		3		2	1	0
Field	Reserved[7:4] HR Data Ready Status[3:0]									
Usage	To get heart rate data ready status									
Notes	tes Field Name Description									
	HR_Data_Ready_S	tatus If sta If sta If sta If sta	Check Heart Rate Data Ready Status. If status is 0, it means data is not ready. If status is 1, it means data is ready. If status is 2, it means loss one data. If status is 3, it means loss two data. Max status is 15, it means loss fourteen data.							

Note: The bit fields with specific value(s) are reserved for future use. It is very important to write the correct value into the corresponding fields. All reserved register values should not be modified to keep the sensor from abnormal status.



Optical Heart Rate Detection Sensor

Update History

Version	Update	Author	Date
V0.1	Creation, Preliminary 1st version	Leon Lin	Dec/06/2013
V0.4	Modify Current Consumption	Leon Lin	Jan/02/2014
V0.5	1. Modify Sensor Name to PAH8001EI-2G	Leon Lin	Jan/14/2014
	2. Modify Operating Temperature Range		
V0.6	1. Content Revised	Leon Lin	Apr/30/2014
V0.7	1. Suggest customer consider 3.3v to avoid voltage drop issue	Leon Lin	Jun/17/2014
	2. Modify Heart rate tolerance	\ \	
V0.8	Add AE register and explain AE function	Leon Lin	Jun/30/2014
V0.9	1. Modify package outline drawing and add recommend layout PCB	Leon Lin	Jul/11/2014
	2. Add exposure time register		