Design Of 4-bit CAM using 9t SRAM cell

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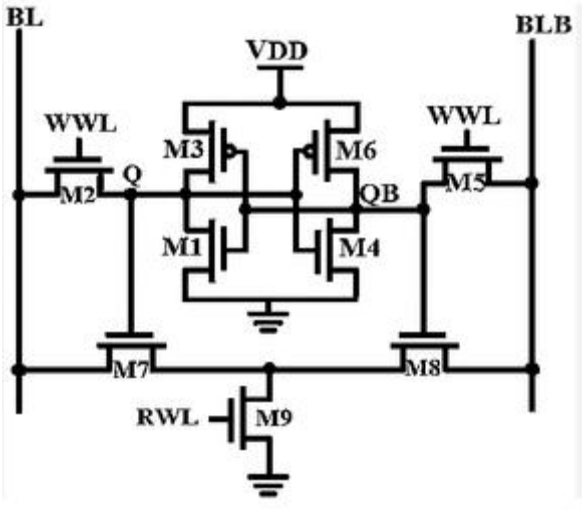
I. Abstract

The main goal of the project is to construct a 4-bit low power content addressable memory (CAM) using a compare-circuit and a 9T SRAM while decreasing size, power, and latency to the greatest extent possible.In this paper, we propose a design for a nine-transistor static RAM-based low-power, high-speed, 4-bit content-addressed memory. On a 22 nm technology, we created the suggested CAM architectures with the goals of lowering power, area, and delay.

II. Introduction

Static Random-Access Memory is a type of Random-Access Memory (RAM), which is a semiconductor device which stores the processor that a micro controller uses to store different variables used for different operations. SRAM uses its memory to store data bits as power is supplied, it allows a fast access to the stored data and is used in the cache memory. SRAM is shown in the figure below.



The benefit of the 9T SRAM cell is that it simultaneously improves data stability while reducing leakage power. As depicted in Fig. 1, a 9T SRAM cell completely isolates the data using bit lines. A separate read signal line is utilized for the read procedure (RWL). The two access

transistors are turned off when the read signal line (RWL) is made high and the write signal line (WWL) is made low (M5 & M2). The information kept in the storage nodes determines how the M7 and M8 transistors operate. Based on the data from the storage nodes, BL and BLB are discharged and charged.

SRAM memory cell consumes lower power during read and writes operations compared to 6T conventional circuit. The ability of the cell to write properly and to have sufficient read noise margin is very important for sub threshold region. we examine many of such necessities for successful operation. Also, a new 9T SRAM combining the advantages of these circuits is proposed in the paper. A nine transistors (9T) SRAM cell configuration is proposed in this paper, which is amenable to small feature sizes encountered in the deep sub-micron/Nano CMOS ranges. Compared with the 8T and 10T cells of [1] and [2], the 9T scheme offers significant advantages in terms of power consumption. The conventional six transistor (6T) SRAM cell shows poor stability at very small feature size with low power supply. During the read operation, voltage division between the access and driver transistors causes the read stability to be very low. Hence in this paper, a 9T SRAM cell is proposed for high read stability and low power consumption. The proposed cell utilizes single bit-line (BL) for write operation, resulting in reduction of dynamic power consumption. During read operation, the data storage nodes are completely isolated from the bit lines, thus ornamental the read static noise margin.

Hence in this paper, a 9T SRAM cell is proposedfor high read stability and low power consumption [5]. The proposed cell utilizes single bit-line (BL) for write operation, resulting in reduction of dynamic power consumption. During read operation, the data completely isolated from the bit line, thus enhancing the read static noise margin.

1. Operations Of SRAM

Read operation

SRAM uses a flip-flop circuit to store each data bit. The circuit delivers two stable states, which are read as 1 or 0. To support these states, the circuit requires six transistors, four to store the bit and two to control access to the cell.[1]

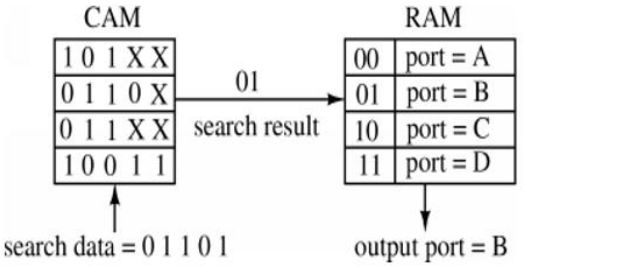
Write Operation

In the write operation, Sense/Write circuit allows to drive bit lines b and complement b',and then it provides accurate values on bit line b and b' as well as go to activate word line.

Content-addressable memory (CAM) is a data storage device that stores memory in cells. When any aspect of the memory is entered, the CAM compares the input with all the stored data. It is

high-speed technology. In CAM, memories are not arranged in chronological order and are not packed in isolated modules.[2]

It analyzes input search data versus a table of saved data, and returns the address of matching data as shown in the figure below.[3]



2. Operation Of CAM

CAM also has a comparison circuitry which is used to compare search data with the data contents stored in its memory simultaneously. This comparison circuitry in the CAM cell occupies extra area than usual memory cell. Hence there is more power dissipation but high speed due to parallel searching operation.[4]
Hence, a basic CAM cell has two functions :

1) Bit Storage like usual memory RAM. So this bit storage uses simple SRAM cell which contains two cross-coupled inverters forming positive feedback working as a D-latch.

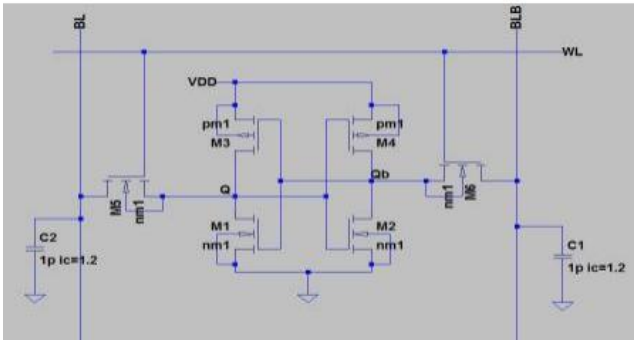
2) Bit Comparison which is equivalent to XNOR logic operation. It is unique in CAM. So, it has three modes of operation: read, write and compare.[4]

III.Implementation And Design

1. 6TSRAM

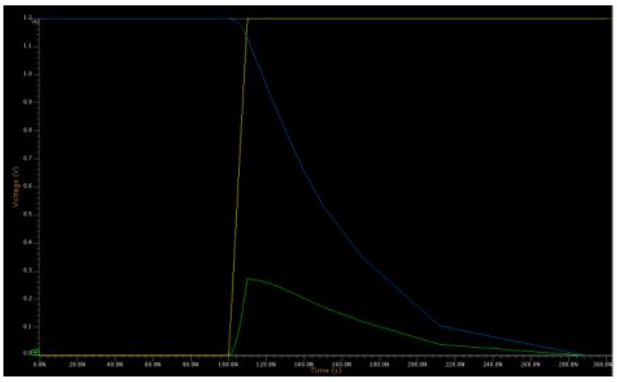
✧ Schematic Of 9T SRAM

The schematic for the SRAM was implemented using 6 transistors as shown in the following figure.

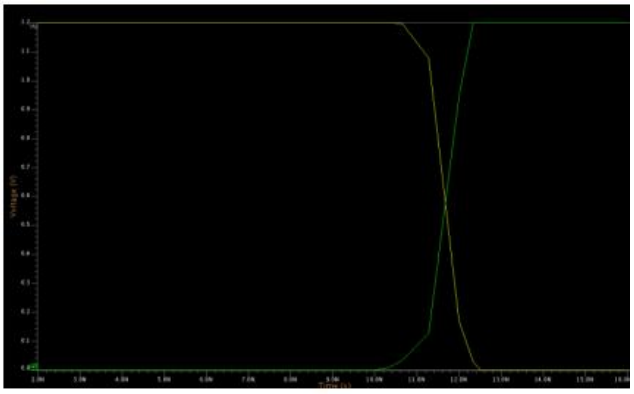


The schematic of basic cell structure it consists of six transistors where NMOS_5 and NMOS_6 is called the access transistor and NMOS_1 and NMOS_2 is called the driver transistor and PMOS_1 and PMOS_2 called the load transistor. Vdd supply is 1.2-volt

Word line is applied to the gates of both the access transistors. Substrate of P channel transistor is connected to the Vdd supply and substrate of N channel is connected to the ground terminal. To understand the working of basic cell we have to assume the previous state of cell. Basically by this circuit we can do only read operation. By taking the input voltage we can store the value SRAM cell. First we applied the input voltage to the inverter one. Then we got the output of inverter one that is input of the second inverter. After the pass transistor gets turn on by the word selection .The value is passing through the access transistor to the bit line and bit line bar. From the bit line and bit line bar, finally we got output. In this way the read operation gets performed.



Read

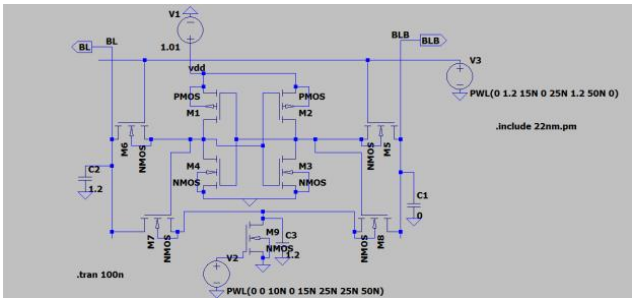


Write

2. 9TSRAM

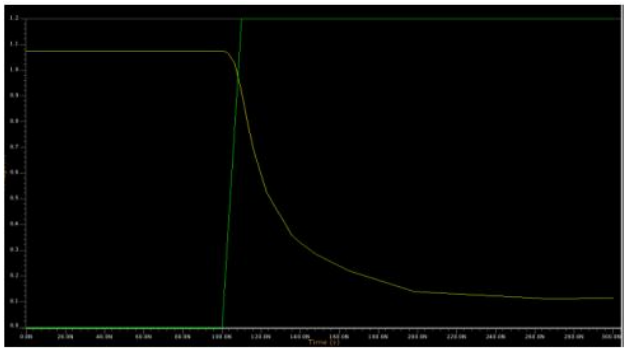
✧ Schematic Of 9T SRAM

The schematic for the SRAM was implemented using 9 transistors as shown in the following figure.

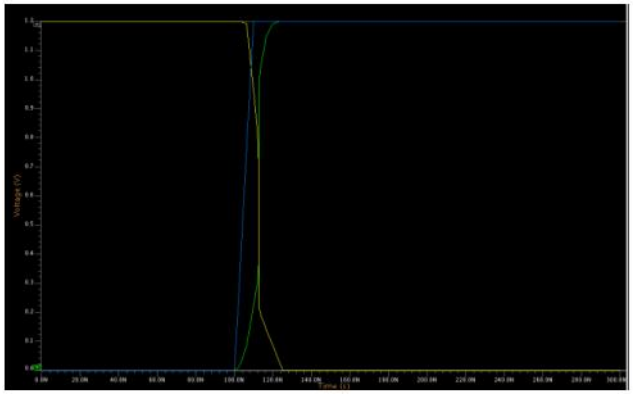


the read and write operations are separated by adding transistor stack to the conventional 6T cell, thus it has the area penalty but operates efficiently than the 6T SRAM cell at lower VDD

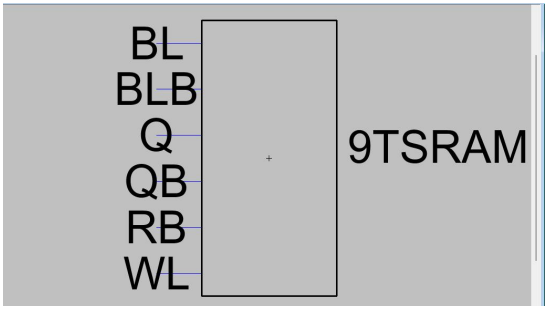
READ AND WRITE OPERATION OF 9T SRAM CELL The upper sub-circuit of the 9T memory cell is essentially a conventional 6T SRAM cell. The write operation is identical with the conventional cell. For write operation write signal WWL is set to 1 and read signal RWL is made 0. The lower circuit of the 9T memory cell is a differential read port. Prior to a read operation, both bitlines precharged to VDD . To start a read operation, the read signal RWL transitions from 0 to 1 and signal WWL goes to low. One of the bitlines is discharged depending on the data that is stored cell.



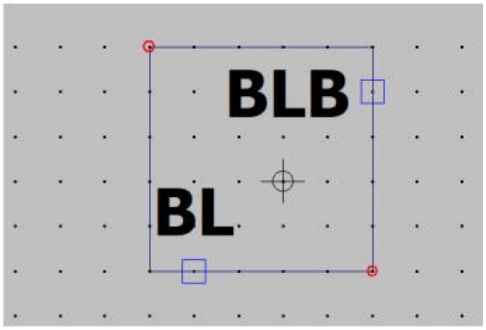
Read



✧ 9T SRAM icon



Make 9tsram cell to block



✧ layout of the 9T SRAM.

The following figure shows the layout of the 9T SRAM

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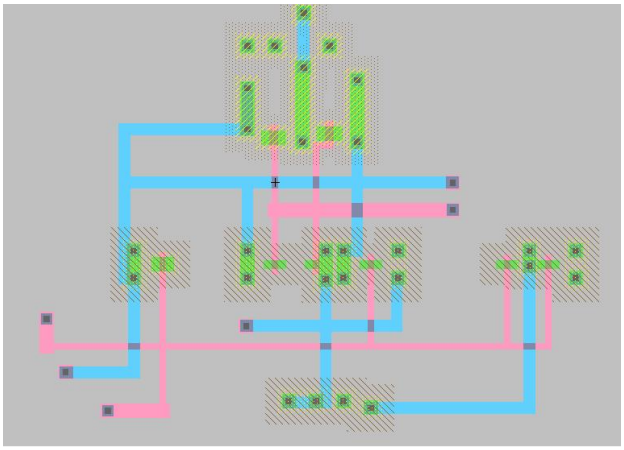
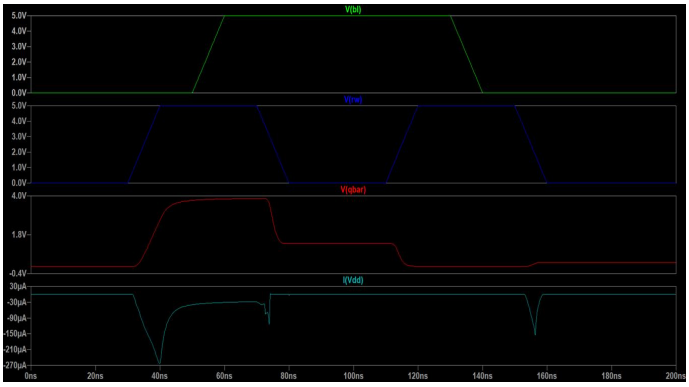


✧ Simulation Of 9T SRAM



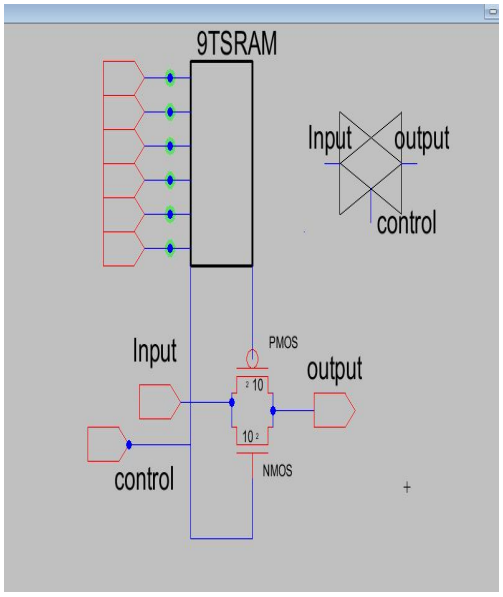
3. 1 Bit CAM

✧ Schematic Of 1 Bit CAM

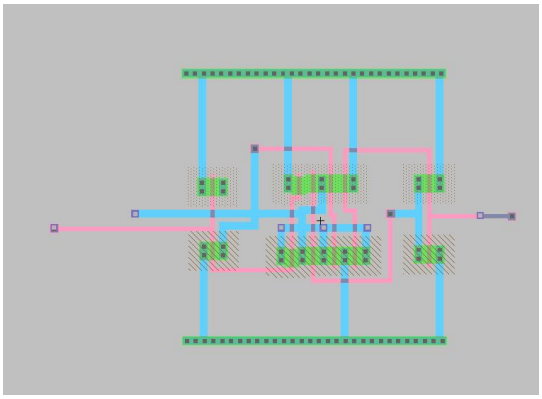
The SRAM schematic was used to build the schematic for the 1-bit CAM cel. The camIN input is compared to the data stored in the SRAM using the pass gates. Outputs of the SRAM Q and QB are the enable bits of the pass gates, and the camIN input and its negation are the values to be passed. Two inverters were used instead of having two camIN inputs, camIN and camOUT. Since (camIN)' is input of the pass gate that has Q as enable, (camIN)' is passed to the output match when Q is high, and camIN is input of the pass gate that has QB as enable, camIN is passed to the output when QB is high. so we need to implement all requirements.

- 9TSRAM was implemented in part 1
- Pass gate
- Inverter

✧ **Schematic Of PassGate**

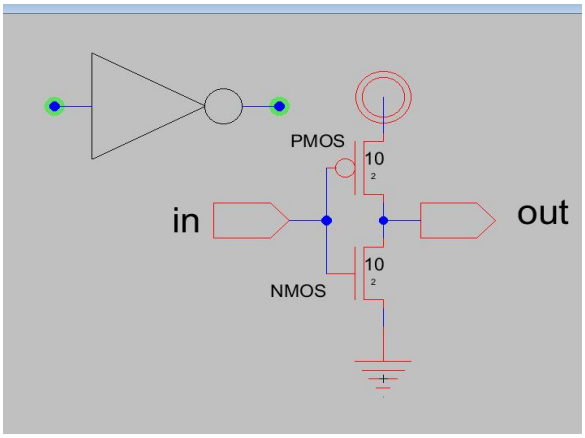


✧ **layout of the PassGate**

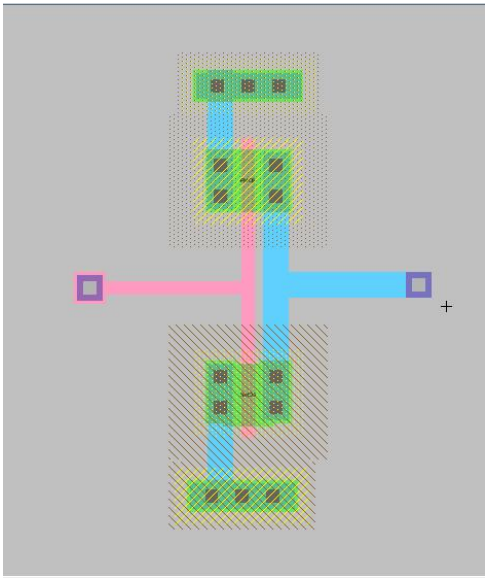


- Inverter

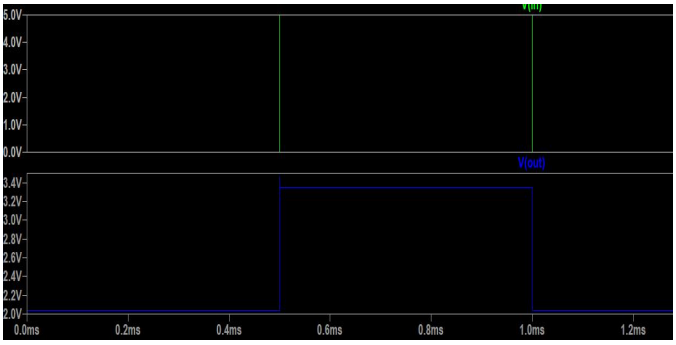
✧ **Schematic Of Inverter**



✧ **Layout Of Inverter**

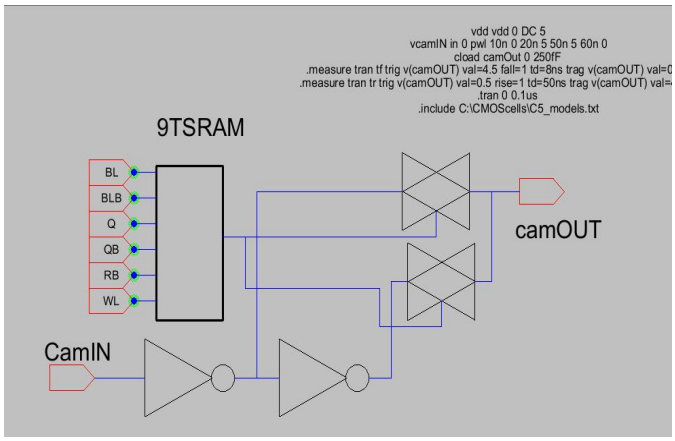


✧ **Simulation Of Inverter**

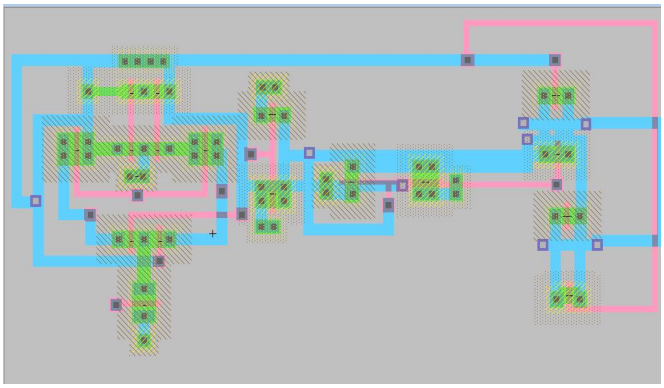


Finally the 1 bit CAM was implemented as shown in the following figure.

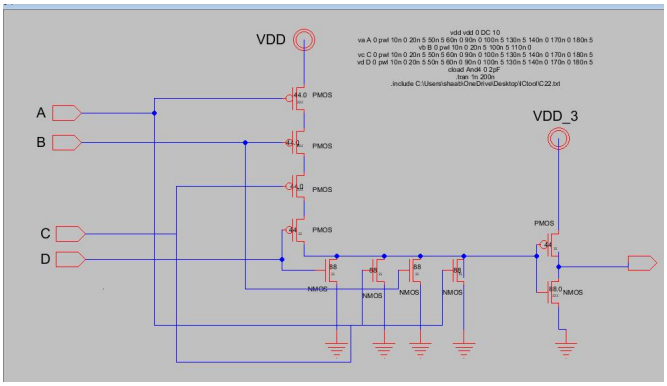
✧ **Schematic Of 1 Bit CAM**



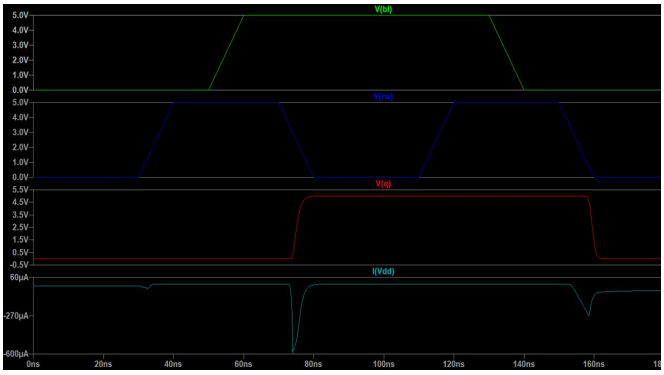
✧ Layout Of 1 Bit CAM



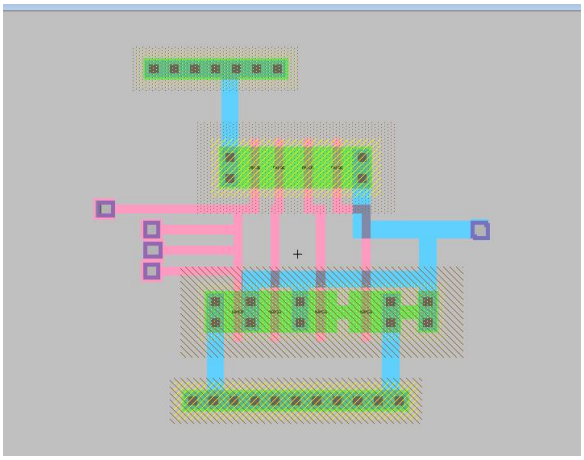
✧ Schematic Of 4 input OR Gate



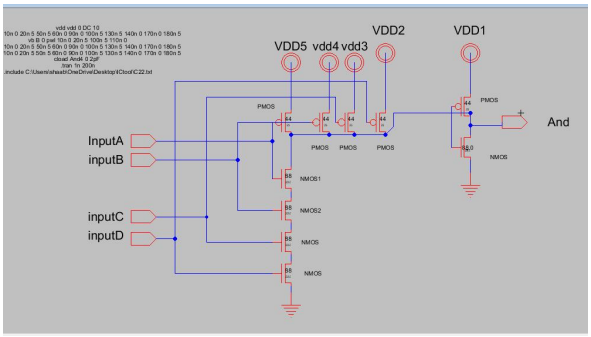
✧ Simulation Of 1 Bit CAM



✧ Layout Of 4 input OR Gate



✧ Schematic Of 4 input AND Gate

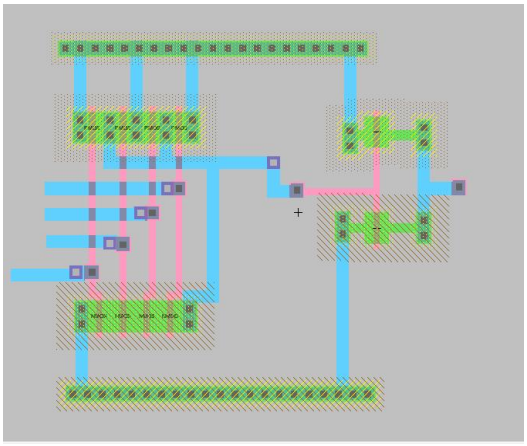


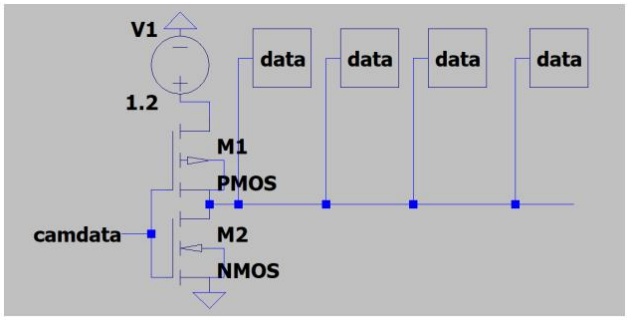
4. 4 Bit CAM

16 blocks of one-bit CAM cell were connected with 4 rows and 4 columns to form the 4-bit CAM cell. Row decoder was built to select one of the rows to write data on so 4-bit WBL and WBLB are shared between all columns and also 4-bit camdata are shared between them to compare between data stored in CAM and the camdata. The match output of each of the four 1-bit CAM cell in each row were ANDed to detect the match occurrence of the whole row, and the four ANDs of the four rows were ORed to generate one match output that represents a match occurrence in the whole design. The column decoder was built to read the data stored in a specific CAM cell of the 16 cells, the data stored in the CAM cell which is enabled by the row and the column decoder is shown in the RBL output of that cell. The following figure shows the schematic of the 4-bit CAM cell.so we need to implement all requirements.

- 1-bit CAM was implemented in part 3
- 4 input OR Gate
- 4 input AND Gate
- Inverter was implemented in part 2
- Decoder

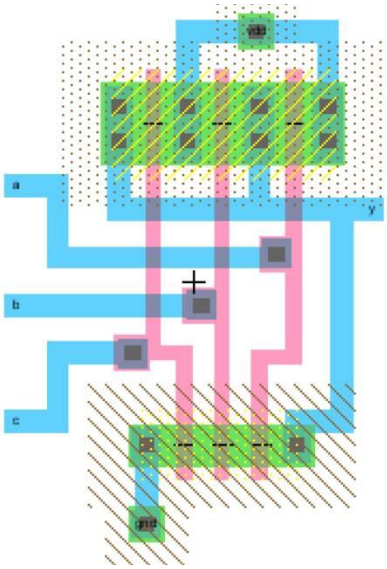
✧ Layout Of 4 input AND Gate



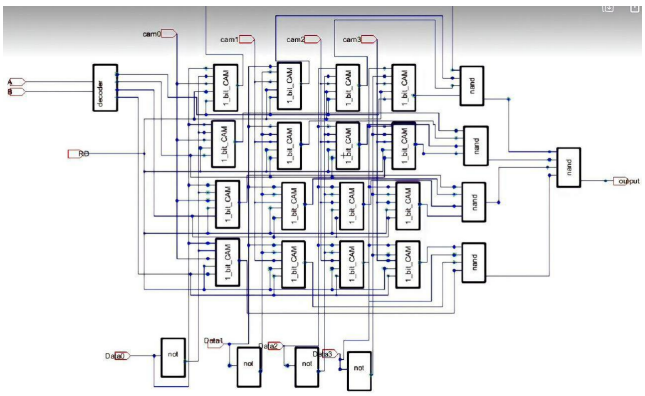


4 bit- cell cam system

✧ layout Of Decoder

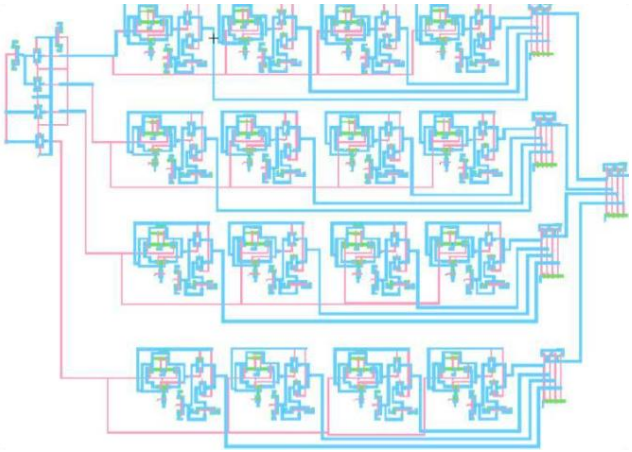


Finally the 4 bit CAM was implemented as shown in the following figure.



✧ Layout Of 4 Bit CAM

✧



Delay , Area and power :

We introduce a versatile auxiliary bit to reduce the search delay there by speed boosting with a little area and power overhead. Before that the existing CAM architecture must be familiarized since our proposed method is similar to existing architecture but with different operating principle. The pre-computation CAM uses additional bits to filter some mismatched CAM words before the actual comparison.

These extra bits are derived from the data bits and are used as the first comparison stage. For example, number of “1” in the stored words are counted and kept in the Counting bits segment. When a search operation starts, number of “1”s in the search word is counted and stored to the segment. These extra information are compared first and only those that have the same number of “1”s (e.g., the second and the fourth) are turned on in the second sensing stage for further comparison. This scheme reduces a significant amount of power required for data comparison, statistically. The main design idea is to use additional silicon area and search delay to reduce energy consumption. The previously mentioned pre-computation and all other existing de-signs shares one similar property.

About 9tsram a one sided schematic triggered based read and write operation form 9T static random access memory cell, it will consume low power and energy consumptions with high read and write stability. The proposed method of schmitt trigger based 9T SRAM memory cell which obtain high read stability in one sided schmitt triggered inverter with a single bit line structure, similarly the write ability will improve the power gating in schmitt trigger inverter with a write assist of control and trip voltage of schmitt trigger inverter. In this proposed work of this paper will designed this 9T SRAM memory cell single bit and 8-bit level which using 16nm and 22nm CMOS technology and proved the performance of area, delay and power

The 9t SRAM mentioned with XOR gate as the comparison circuitry are used to build a CAM cell, the XOR gate is used to check the matching between bits on the SRAM cell and cam data.

CONCLUSION

A high speed low power CAM with a parity bit was proposed. A CAM is a type of memory in which the contents are accessed by the words than memory locations. In the existing system design which is the pre-computation method we make use of the counting bit segment which is of 4 bit along with the input data and also with the words stored inside the cam memory this increases the number of steps in search operation by finding out the number of one's in the input bit and that stored in cam memory and this design methodology meets with Ion/Ioff problem this altogether results in increase in search speed delay and additional silicon area consumption. In the proposed method we are introducing a parity bit instead of the counting bit which will reduce the search speed delay hence the output is fetched at an interval of one clock cycle. Since content addressable memory has wide application in the communication field the proposed design of cam can create revolutionary changes. This design helps to improve the search speed of cam and improve its efficiency

References

[1]https://www.techtarget.com/whatis/definition/SRAM-static-random-access-memory#:~:text=SRAM%20uses%20a%20flip%2Dflop,control%20access%20to%20the%20cell.

[2]https://www.geeksforgeeks.org/what-is-content-addressable-memory/

[3]https://assignmentpoint.com/content-addressable-memory/

[4]https://www.ijsr.net/archive/v4i10/SUB159221.pdf

[5] https://www.ijert.org/design-of-efficient-low-power-9t-sram-cell

[6]https://www.scribd.com/document/255635237/Static-RAM#

[7] https://ritaj.birzeit.edu/bzu-msgs/attach/2205823/Low-power+Content+Addressable+Memory+Array+for+Mobile+Devices_Rev2.pdf

[8] https://ritaj.birzeit.edu/bzu-msgs/attach/2205824/design-of-efficient-low-power-9t-sram-cell-IJERTV2IS1448.pdf