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CECS 360

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21 Feb 2018

Assignment #1

Introduction:

This is a 32-bit counter program designed with Verilog. Switch 0 controls count up/down mode. The button up acts as a reset and when button down is pressed, it will increment/decrement the 32-bit counter. The 8 LEDs connected to the anodes and cathodes will display the counter value.

Modules:

AISO: obtains reset, handles metastability by passing through two registers, then outputs a clean reset signal which can be used for other modules.

db\_ticker: generates a single tick for every 1MHz.

debounce\_2: a modified moore finite state machine module with 8 states: 4 for low (0) output states and 4 for high (1) output states. Results in a clean square wave of low to high.

pulse\_maker: obtains a square wave from debounce and converts it into a single positive edge detect pulse.

counter: a 32-bit counter which increments/decrements itself upon a positive edge detect. Increments if up-high down-low (Switch 0) is high and decrements if low.

display\_controller: obtains counter value input and displays it onto the 8 seven-segment LED displays.

ticker: generates a single tick for every 100kHz

pixel\_controller: a modified moore finite state machine module with 8 states, each state for each seven-segment LED display. Shifts to the next display upon every tick.

ad\_mux: distributes 4-bit counter values per display.

hex\_to\_7\_segment\_decoder: decodes digital hex values into visible hex values which can be observed on the seven-segment displays.

reg\_1bit: 1-bit register.