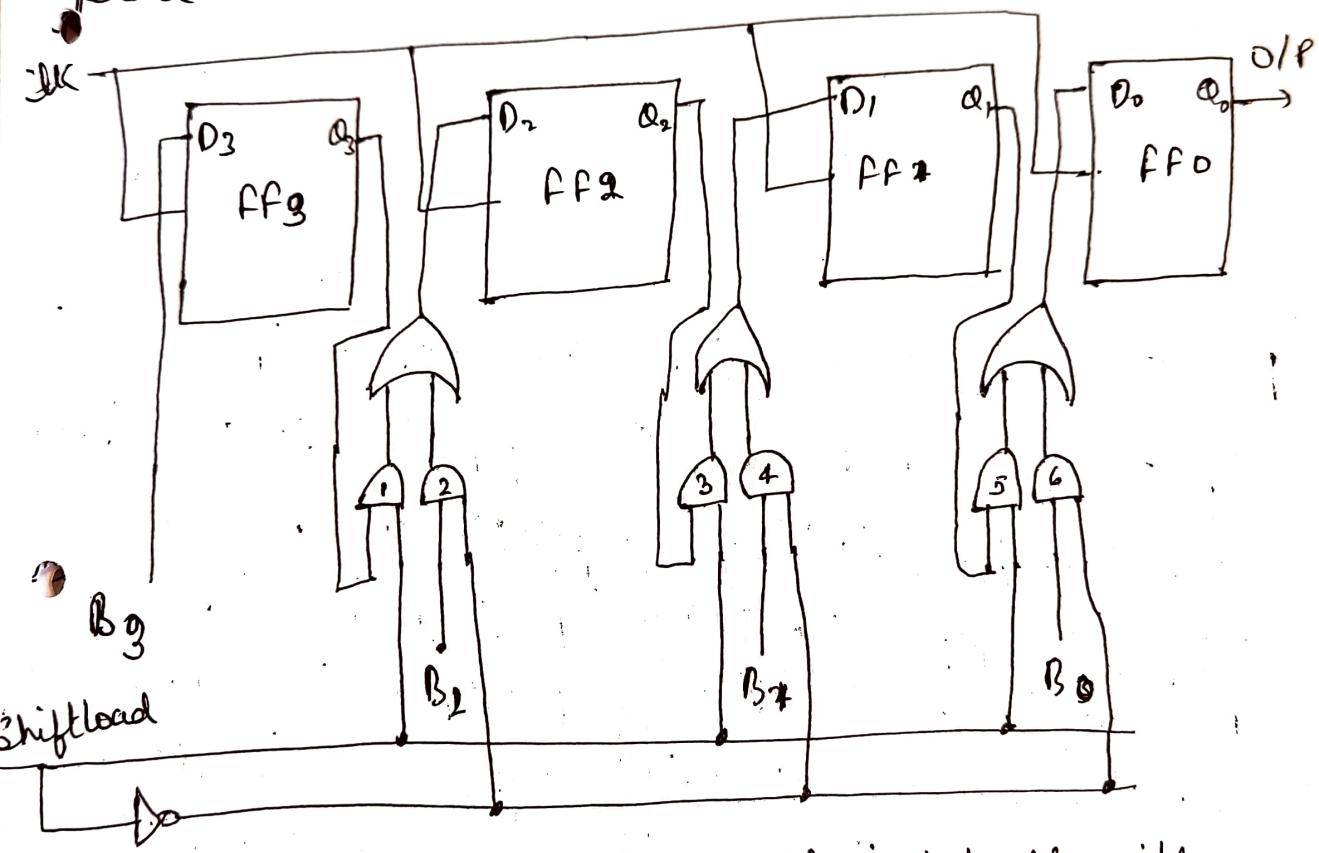
ft mode : ... memory cell which

When the shift/load bar line is ~~low~~ High (1), the ③ AND gates 2, 4 & 6 becomes inactive, Hence the Parallel loading of the data becomes impossible But the AND gate 1, 3, and 5 become active Therefore the shifting of data from left to right bit by bit on application of clock pulses. Then parallel in serial out operation takes place.



Now let suppose Control Signal is '0' then the data to be loaded and then data will become 1101

CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	1	1	0	1 → 1
2	0	1	1	0 → 0
3	0	0	1	1 → 1
4				
5	0	0	0	1 → 1
6				

1011

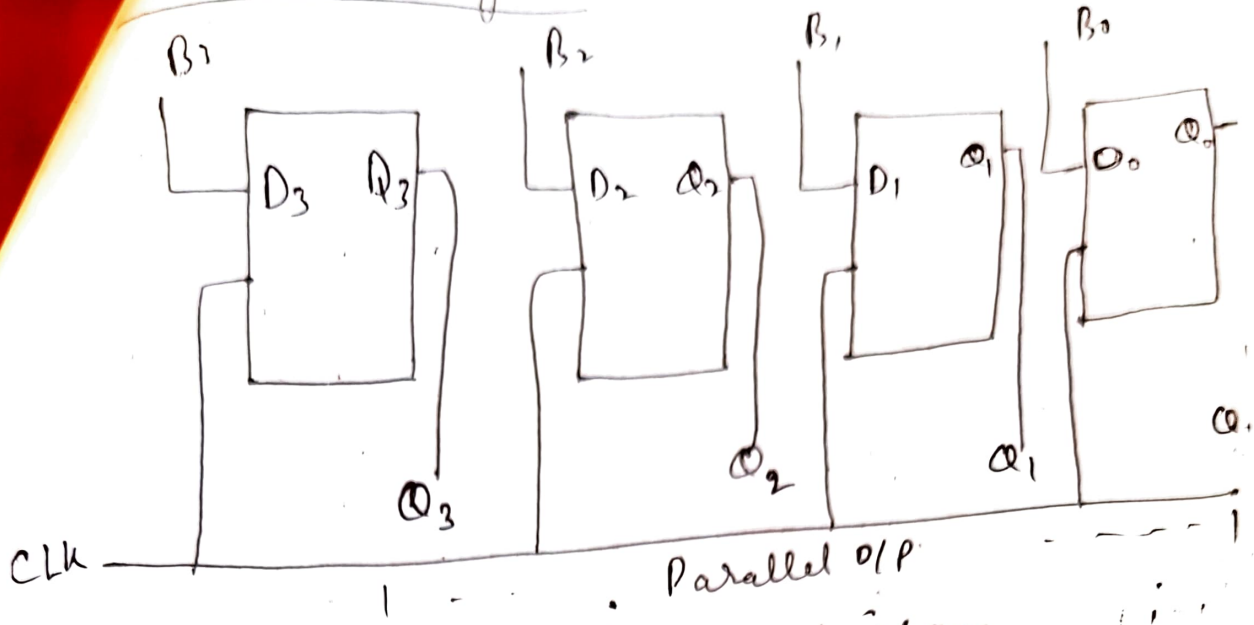
1101

1101 → Q_0

1101

PIPO : In this register the 4 bit binary input B_0, B_1, B_2, B_3 is applied to the data inputs D_0 D_1 D_2 D_3 respectively, as clock edge is applied, the input binary bits will be loaded into the flip flop simultaneously The loaded bits will appear simultaneously to the O/P side. only clock pulse is essential to load all ~~data~~ data bits

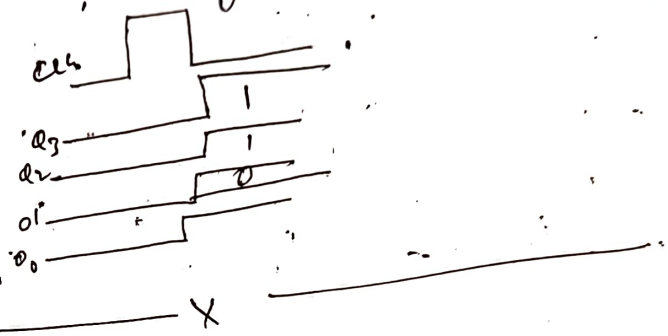
Block diagram



Truth Table

CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	1	1	0	1

Timing diagram



Bidirectional Shift Register :

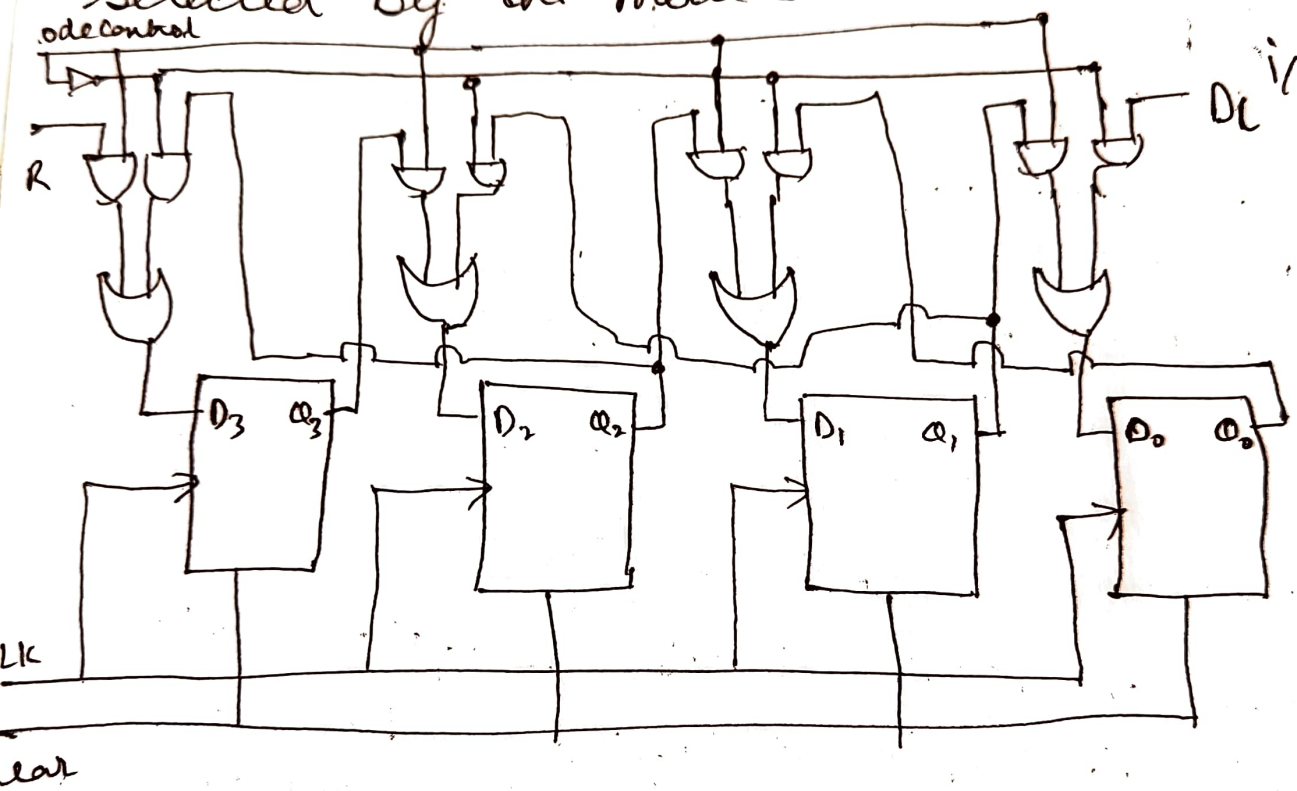
The register which is used shift the data on the right side or left side based on the selected mode is known as the bidirectional shift register.

If the selected mode is high (1), the data will be moved to the right side & If the selected mode is low (0), the data will be moved to the left side.

If we move binary number (base two) to the left side, it is to multiply the no. by 2. and if we shift right, no needs to divide by 2.

Timing

To execute these operations, we require a register to shift the data in any direction. This register can be implemented using D-flip flop and logic gates which allows the data bit to transfer from one stage to next stage to any side either right or left based on an I/P signal. Here, the direction of data shifting is selected by the mode control.



The bidirectional shift register mainly include two serial I/P like the data input with serial right shift (DR) and the data I/P with serial left (DL) with select (M) whenever the data need to shift right side the input is given to DR & for left input is given to DL.

ration of Bidirectional Shift Registers

with M = 1 shift right operation: ; If M=1 and then AND gates 1, 3, 5, and 7 are enabled whereas the remaining AND Gates 2, 4, 6 and 8 will be disabled. The data Dr is shifted to right bit by bit from FF-3 to FF-0 on applecation of Clock pulses. Thus with M=1, we get Serial right Shift operation.

② If M=0, 2, 4, 6, and 8 are enabled, The data DL Shifted by left bit by bit from FF 0 to FF 3.

UNIVERSAL Shift Register : A Shift register which can apply shift the data in both direction as well as load it parallely is known as a universal Shift register. The shift register is capable of performing the following operation

① Parallel loading ② left & Right Shifting

Q. A 4 bit serial in parallel out shift register is initially set to 1111. The data 1010 is applied to the i/p. After 3 clock pulses the o/p will be

		Store	
Initially	1010	1111	1111
1st	0101	0111	1 0111
2nd	10	1011	2 1011
3	1	0101	3 0101

Q.

1231 <5
1195

1111 → 1010

			1111
1st	→ 1010	→	0111
2nd.	→	→	1011
3rd	→		0101

Ques. Find 2's Complement +45.

2	45	
2	22	1
2	11	0
2	5	1
2	2	1
2	1	0
	0	1

2	45	
2	22	1
2	11	0
2	5	1
2	2	0
	1	1

⇒ 101101
1's Comp ⇒ 010010
+ 1
010011