Q1:

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library ieee;

use ieee.std\_logic\_1164.all;

entity myEntity is

port ( a, b, c, d : IN STD\_LOGIC;

Q : OUT STD\_LOGIC

);

end myEntity;

architecture behavioral of myEntity is

begin

process (a, b ,c, d)

begin

if ( a = '0' and b = '0' and c = '0' and d = '0') then Q <= '1'; *-- 0000*

elsif (a = '0' and b = '0' and c = '0' and d = '1') then Q <= '1'; *-- 0001*

elsif (a = '0' and b = '0' and c = '1' and d = '0') then Q <= '1'; *-- 0010*

elsif (a = '0' and b = '1' and c = '0' and d = '0') then Q <= '1'; *-- 0100*

elsif (a = '1' and b = '0' and c = '0' and d = '0') then Q <= '1'; *-- 1000*

else Q <= '0'; end if;

end process;

end architecture;

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LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY myEntity\_tb IS

END myEntity\_tb;

ARCHITECTURE testbench OF myEntity\_tb IS

component myEntity

port ( a, b, c, d : IN STD\_LOGIC;

Q : OUT STD\_LOGIC

);

end component;

signal a, b, c, d : STD\_LOGIC := '0';

signal Qout : STD\_LOGIC;

BEGIN

uut : myEntity port map (a, b, c, d, Qout);

sim\_proc : process

begin

*-- 0000*

a <= '0';

b <= '0';

c <= '0';

d <= '0';

wait for 10 ns;

*-- 0001*

a <= '0';

b <= '0';

c <= '0';

d <= '1';

wait for 10 ns;

*-- 0010*

a <= '0';

b <= '0';

c <= '1';

d <= '0';

wait for 10 ns;

*-- 0011*

a <= '0';

b <= '0';

c <= '1';

d <= '1';

wait for 10 ns;

*-- 0100*

a <= '0';

b <= '1';

c <= '0';

d <= '0';

wait for 10 ns;

*-- 0101*

a <= '0';

b <= '1';

c <= '0';

d <= '1';

wait for 10 ns;

*-- 0110*

a <= '0';

b <= '1';

c <= '1';

d <= '0';

wait for 10 ns;

*-- 0111*

a <= '0';

b <= '1';

c <= '1';

d <= '1';

wait for 10 ns;

*-- 1000*

a <= '1';

b <= '0';

c <= '0';

d <= '0';

wait for 10 ns;

*-- 1001*

a <= '1';

b <= '0';

c <= '0';

d <= '1';

wait for 10 ns;

*-- 1010*

a <= '1';

b <= '0';

c <= '1';

d <= '0';

wait for 10 ns;

*-- 1011*

a <= '1';

b <= '0';

c <= '1';

d <= '1';

wait for 10 ns;

*-- 1100*

a <= '1';

b <= '1';

c <= '0';

d <= '0';

wait for 10 ns;

*-- 1101*

a <= '1';

b <= '1';

c <= '0';

d <= '1';

wait for 10 ns;

*-- 1110*

a <= '1';

b <= '1';

c <= '1';

d <= '0';

wait for 10 ns;

*-- 1111*

a <= '1';

b <= '1';

c <= '1';

d <= '1';

wait for 10 ns;

end process;

END;

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | Q |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

Q2:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

ENTITY DoD IS

PORT ( dir : IN STD\_LOGIC\_VECTOR(3 DOWNTO 0);

leds : OUT STD\_LOGIC\_VECTOR(1 TO 7) );

END DoD ;

ARCHITECTURE Behavior OF DoD IS

BEGIN

PROCESS (dir)

BEGIN

CASE dir is

WHEN "0000" => leds <= "0001110" ;

WHEN "0001" => leds <= "1110111" ;

WHEN "0010" => leds <= "0111110" ;

WHEN "0011" => leds <= "1111110" ;

WHEN "0100" => leds <= "1100000" ;

WHEN "0101" => leds <= "0001100" ;

WHEN "0110" => leds <= "1000010" ;

WHEN "0111" => leds <= "0011000" ;

WHEN "1000" => leds <= "0001110" ;

WHEN "1001" => leds <= "1000010" ;

WHEN "1010" => leds <= "0111110" ;

WHEN "1011" => leds <= "1100000" ;

WHEN "1100" => leds <= "1110111" ;

WHEN "1101" => leds <= "0011000" ;

WHEN "1110" => leds <= "1111110" ;

WHEN "1111" => leds <= "0001100" ;

WHEN OTHERS => leds <= "-------" ;

END CASE ;

END PROCESS ;

END Behavior ;

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LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY DoD\_tb IS

END DoD\_tb;

ARCHITECTURE behavioral OF DoD\_tb IS

*-- Component Declaration for the Unit Under Test (UUT)*

COMPONENT DoD

PORT ( dir : IN STD\_LOGIC\_VECTOR(3 DOWNTO 0);

leds : OUT STD\_LOGIC\_VECTOR(1 TO 7)

);

END COMPONENT;

*--Inputs*

signal dir : std\_logic\_vector(3 DOWNTO 0) := "0000";

*--Outputs*

signal leds : std\_logic\_vector(1 TO 7);

BEGIN

*-- Instantiate the Unit Under Test (UUT)*

uut: DoD PORT MAP (

dir => dir,

leds => leds

);

*-- Stimulus process*

stim\_proc: process

begin

*-- hold reset state for 20 ns.*

wait for 20 ns;

*-- insert stimulus here*

*-- testing for version A (msb = 0)*

dir <= "0000";

wait for 10 ns;

dir <= "0001";

wait for 10 ns;

dir <= "0010";

wait for 10 ns;

dir <= "0011";

wait for 10 ns;

dir <= "0100";

wait for 10 ns;

dir <= "0101";

wait for 10 ns;

dir <= "0110";

wait for 10 ns;

dir <= "0111";

wait for 10 ns;

*-- testing for version B (msb = 1)*

dir <= "1000";

wait for 10 ns;

dir <= "1001";

wait for 10 ns;

dir <= "1010";

wait for 10 ns;

dir <= "1011";

wait for 10 ns;

dir <= "1100";

wait for 10 ns;

dir <= "1101";

wait for 10 ns;

dir <= "1110";

wait for 10 ns;

dir <= "1111";

wait for 10 ns;

end process;

END;

Graphical user interface, application

Description automatically generated

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| W | X | Y | Z | a | b | c | d | e | f | g |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

Q3:

library ieee;

use ieee.std\_logic\_1164.all;

entity Q3 is

port ( x , clk : IN STD\_LOGIC;

a, b, z : OUT STD\_LOGIC

);

end Q3;

architecture behavioral of Q3 is

signal qa, qb : std\_logic;

begin

process (clk)

begin

if falling\_edge(clk) then

*--ja = x’b and ka = x*

qa <= ((not x) and qb) and ((not qa) or (not x)) and qa;

*-- jb = x’ and kb = a’x*

qb <= (not x) and (((not qb) or qa) or (not x)) and qb;

end if;

end process;

a <= qa;

b <= qb;

z <= ((not x) and (not qa)) or (qb and x);

end behavioral;

Q4:

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library ieee;

use ieee.std\_logic\_1164.all;

entity q4 is

port ( clk, resetn : IN STD\_LOGIC;

z : OUT STD\_LOGIC

);

end q4;

architecture behaviour of q4 is

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*-- 8 > 4 > 2 > 0 > 1*

*-- 1000 > 0100 > 0010 > 0000 > 0001*

subtype state is std\_logic\_vector (3 downto 0);

signal y : state;

constant state0: state := "1000";

constant state1: state := "0100";

constant state2: state := "0010";

constant state3: state := "0000";

constant state4: state := "0001";

begin

process(resetn, clk)

begin

if resetn = '0' then

y <= state0;

elsif (rising\_edge(clk)) then

case y is

when state0 =>

y <= state1;

when state1 =>

y <= state2;

when state2 =>

y <= state3;

when state3 =>

y <= state4;

when state4 =>

y <= state0;

when others => y <= "----";

end case;

end if;

end process;

z <= '1' when y = state0 else '0';

end behaviour;

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library ieee;

use ieee.std\_logic\_1164.all;

entity Q4\_tb is

end Q4\_tb;

architecture behavior of Q4\_tb is

component Q4

port ( clk, resetn : IN STD\_LOGIC;

z : OUT STD\_LOGIC

);

end component;

signal clk : STD\_LOGIC := '0';

signal resetn : STD\_LOGIC := '0';

signal z : STD\_LOGIC;

constant Clock\_period : time := 20 ns;

begin

uut: Q4 port map (clk, resetn, z);

clk\_process: process

begin

clk <= '0';

wait for Clock\_period/2;

clk <= '1';

wait for Clock\_period/2;

end process;

sim\_proc: process

BEGIN

resetn <= '1';

wait for 10 ns;

end process;

end behavior;

Diagram

Description automatically generated