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Timepix3: a 65K channel hybrid pixel readout chip with simultaneous ToA/ToT and sparse readout

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ABSTRACT: The Timepix3, hybrid pixel detector (HPD) readout chip, a successor to the Timepix [1] chip, can record time-of-arrival (ToA) and time-over-threshold (ToT) simultaneously in each pixel. ToA information is recorded in a 14-bit register at 40 MHz and can be refined by a further 4 bits with a nominal resolution of 1.5625 ns (640 MHz). ToT is recorded in a 10-bit overflow controlled counter at 40 MHz. Pixels can be programmed to record 14 bits of integral ToT and 10 bits of event counting, both at 40 MHz. The chip is designed in 130 nm CMOS and contains 256 $\times$ 256 pixel channels (55 $\times$ 55 μm^2). The chip, which has more than 170 M transistors, has been conceived as a general-purpose readout chip for HPDs used in a wide range of applications. Common requirements of these applications are operation without a trigger signal, and sparse readout where only pixels containing event information are read out.

A new architecture has been designed for sparse readout and can achieve a throughput of up to 40 Mhits/s/cm^2. The flexible architecture offers readout schemes ranging from serial (one link) readout (40 Mbps) to faster parallel (up to 8 links) readout of 5.12 Gbps. In the ToA/ToT operation

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mode, readout is simultaneous with data acquisition thus keeping pixels sensitive at all times. The pixel matrix is formed by super pixel (SP) structures of 2×4 pixels. This optimizes resources by sharing the pixel readout logic which transports data from SPs to End-of-Column (EoC) using a 2-phase handshake protocol.

To reduce power consumption in applications with a low duty cycle, an on-chip power pulsing scheme has been implemented. The logic switches bias currents of the analog front-ends in a sequential manner, and all front-ends can be switched in 800 ns. The digital design uses a mixture of commercial and custom standard cell libraries and was verified using Open Verification Methodology (OVM) and commercial timing analysis tools. The analog front-end and a voltage-controlled oscillator for 1.5625 ns timing resolution have been designed using full custom techniques.

KEYWORDS: VLSI circuits; CMOS readout of gaseous detectors; Front-end electronics for detector readout

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1 Introduction

Timepix [1] was conceived as a timing measurement chip with an added functionality of measuring time-over-threshold (ToT). ToT functionality was found useful in many applications (for example [2, 3]), and Timepix3 extends the functionality of Timepix by allowing simultaneous time-of-arrival (ToA)/ToT measurement. It also aims to improve the timing resolution of Timepix by over a factor of 6. The pixel size has been retained at $55 \times 55\,\mu\text{m}^2$. The Timepix3 engineering run has been funded by Medipix3 collaboration, and it has been a multi-site project between the European Organization for Nuclear Science (CERN), Nikhef and the University of Bonn.

Although full scale (non-prototype) chips with capabilities of simultaneous ToA/ToT measurement do exist [4–6], their spatial or timing resolution are not satisfactory for all applications. For example, in [7] it is pointed out, that longitudinal resolution in gas-electron multiplier time-projection chambers (GEM-TPCs) could be improved by having better timing resolution in the readout chip. Timepix3 has been designed to address these issues by using pixels of $55 \times 55\,\mu\text{m}^2$, and as mentioned, by improving timing resolution. The timing improvement has been achieved by using voltage-controlled oscillators (VCOs) inside the pixel matrix [8, 9]. In some low duty cycle applications [10] power consumption needs to be reduced by additional means. An on-chip power pulsing functionality has been added into Timepix3 to support its deployment in these applications. Main usage of Timepix3 is seen to be in particle tracking applications where timing and spatial resolution are important. However, the chip can be programmed in event counting or photon counting mode and used in imaging applications with higher particle rates than 40 Mhits/cm^2/s. The choice of the sensor will depend on the particular application but the first assemblies with a bonded sensor will use silicon sensors. In GEM-TPCs Timepix3 will be used without any sensor on top. Other possible applications for Timepix3 are described in [11].

2 General chip description

The main features of Timepix3 architecture are summarized in table 1. In addition to the simultaneous ToA/ToT measurement, an on-chip zero suppression scheme has been implemented in which only pixels with event data are read out. This reduces the dead-time per pixel compared to Timepix

Table 1. Summary of Timepix3 features.

CMOS technology	130 nm, 8-metal stack
Pixels	256 × 256
Pixel size	55 × 55 μm^2
Acquisition modes	Charge and time Time only Event counting and integral charge
Zero suppressed readout	YES
Dead time per pixel	ToT Pulse time + 475 ns
Timing resolution	1.5625 ns (640 MHz)
On-chip power pulsing	YES
Output bandwidth	Up to 5.12 Gbps (8 × 640 Mbps)
I/O	SLVS, 8b/10b, 8 output links for data

with occupancies below 50%. The chip provides 8b/10b encoded output data stream which can be used for clock and data recovery (CDR). This removes the need for sending a clock signal with the output stream. The stream can be sent off the chip using 1 to 8 output links. These links are driven by scalable low-voltage signaling (SLVS) drivers with adjustable current. On-chip phase-locked loop (PLL) supports output data frequencies from 40 MHz to 320 MHz at double data rate (DDR). An external clock can also be provided to readout the chip at user-chosen frequencies. The chip can be connected to a readout system board using wire-bonding or using through-silicon vias (TSVs) and redistribution layer under the chip.

Figure 1 shows a motivation for a change of readout architecture from a frame-based readout to a packet based architecture. A break-even point, above which a full-frame readout becomes faster, occurs at occupancies greater or equal to 50 %. Below this point, it is advantageous to use a packet-based readout. Readout time can be calculated as follows:

$$T_{\text{readout}} = N_{\text{pixels}} * bits_{\text{pixel}}/BW \tag{2.1}$$

where N_{pixels} is the number of pixels being read out, $bits_{\text{pixel}}$ the number of bits per pixel and BW the total output bandwidth of the chip. For a frame-based readout N_{pixels} is equal to the number of pixels per chip while for a packet-based readout it is exactly the number of pixels hit. Bits per pixel is assumed to be 28 bits for the frame-based readout and 28 bits + 16 bits (due to address overhead in each packet) for the packet-based readout shown in figure 1.

Readout time is not the only reason for a packet-based architecture. Duty cycle of the chip is also an important consideration, and due to continuous readout and data buffering inside the pixel matrix, Timepix3 can achieve a duty cycle of 100 % if required if the total particle rate does not exceed 40 Mhits/cm^2/s. In practice this means that the shutter controlling data acquisition (DAQ) can be kept open indefinitely without having to close it for the duration of readout.

High-level simulations using SystemVerilog (SV) [12] hardware description language were performed using data from several Timepix test beam runs to verify the readout architecture. Simulations facilitated fast prototyping of different readout architecture solutions without having to

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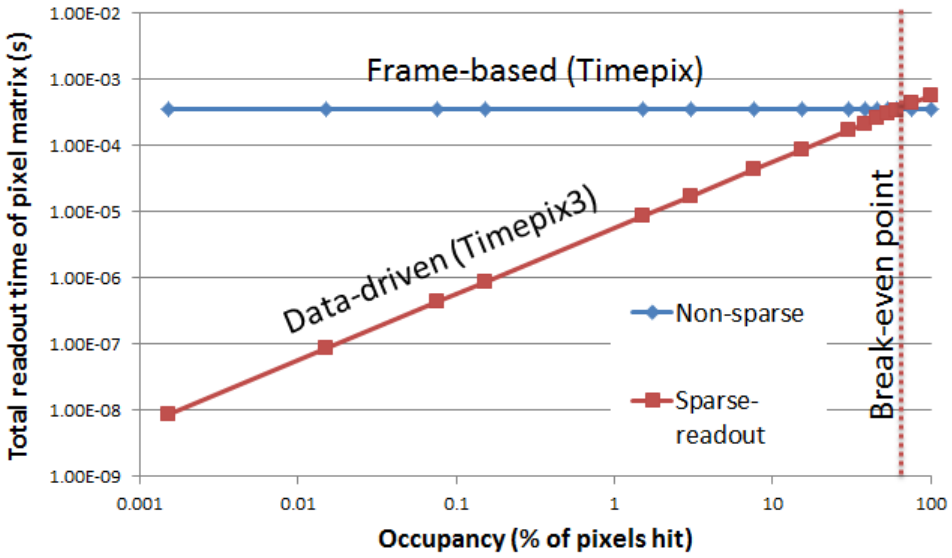

Figure 1. Readout times of a pixel matrix with a frame-based (non-sparse) and a packet-based (sparse) readouts.

debug multiple detailed circuit descriptions. By adopting these simulation methods, criticial limitations in some readout architecture options were uncovered early in the design process thus reducing the amount of implementation and functional verification work.

Figure 2 shows the three different packet formats of a pixel in Timepix3. Header information is included in each packet to distinguish event data packets from control packets. Address information consists of the position of a pixel in the pixel matrix. The next 14 bits contain either coarse time information or integral charge information. The coarse time information is generated by a 14-bit gray counter per double column, and distributed from bottom of the column to the top using two busses. One bus per physical pixel column was used because this required less horizontal routing to connect the busses to on-pixel memories. The following 10 bits consist either of charge information (ToT) or event count information. The event count information. in case of photons for example, is simply the number of photons counted by that pixel. A 4-bit event counter can be substituted for the four least significant bits (LSBs) (fine time) to detect pile-up hits in ToA/ToT and ToA-only modes or it can do photon counting, for example. Because each packet is tagged with an address of the pixel, no full frame needs to be decoded before obtaining information for an individual pixel. Each packet is a self-contained unit of information which is in contrast to Timepix, where a full frame readout is needed. Regardless of the operation mode of the pixel, the readout architecture processes each of the three different packet formats identically, simplifying the implementation of the logic.

The schematic of one pixel and the super pixel (SP) logic connected to it is shown in figure 3. The analog front-end contains a preamplifier with leakage current compensation feedback circuitry, a 4-bit digital-to-analog converter (DAC) for local threshold tuning and a discriminator. The digital front-end has synchronization logic to synchronize asynchronous hits to the on-pixel clock, and local clock gating is used to reduce the dynamic power consumption of inactive pixels. Each

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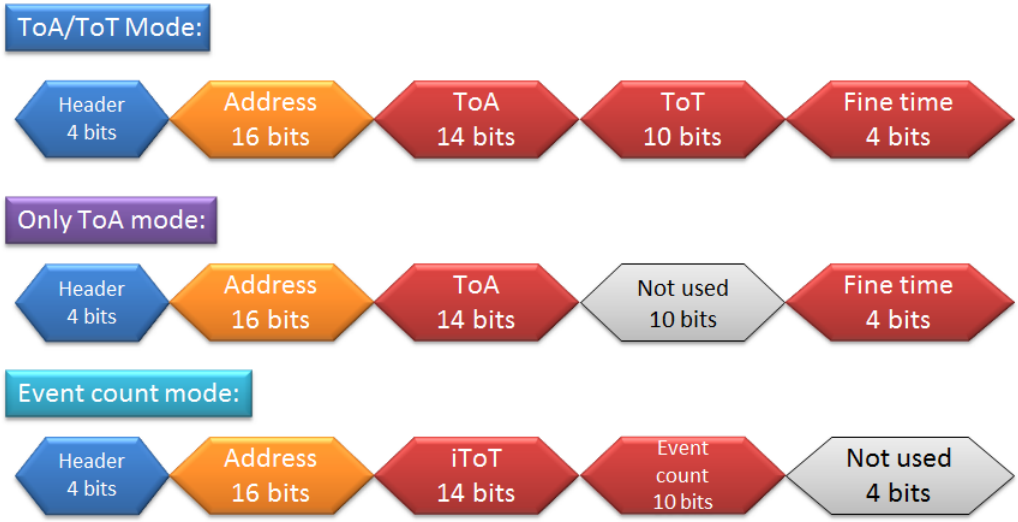

Figure 2. Packets in three different pixel operation modes.

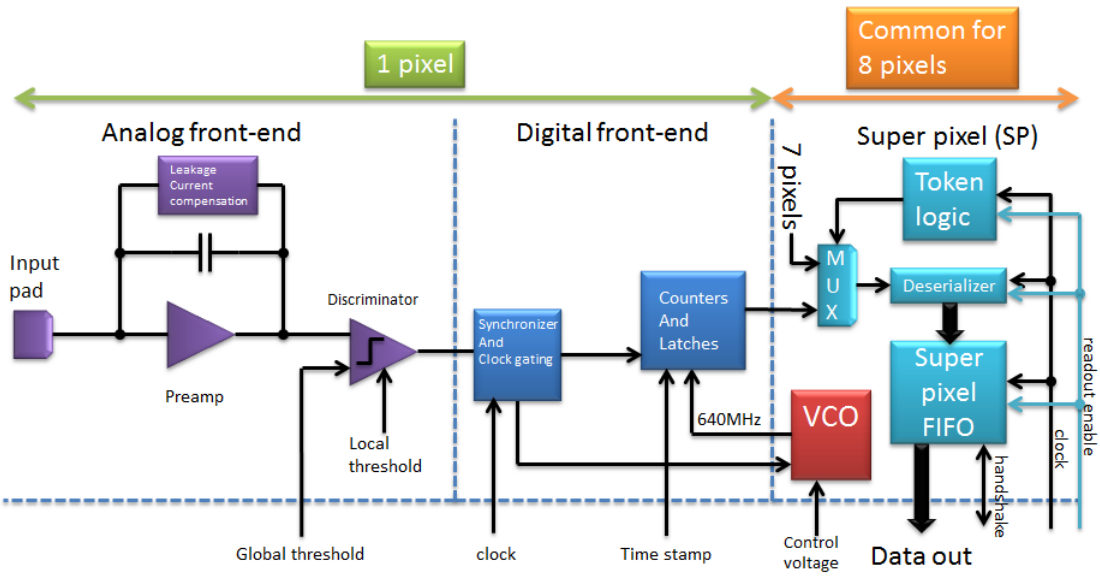

Figure 3. A schematic of one pixel and SP logic shared by 8 pixels.

pixel also has a 14-bit time stamp register, a 10-bit linear-feedback shift register (LFSR) for ToT measurement and logic to configure these counters as a 10-bit event counter and a 14-bit integral time-over-threshold (iToT) counter.

The operation principle of the pixel front-end programmed in simultaneous ToA/ToT mode is shown in figure 4. When the output of the amplifier exceeds the programmable threshold, the discriminator output rises and starts the 640 MHz clock. The clock is stopped by the rising edge of the 40 MHz clock. These clocks are asynchronous to each other and careful synchronization in the digital front-end is required to avoid counter upsets. The duration of ToT measurement is counted

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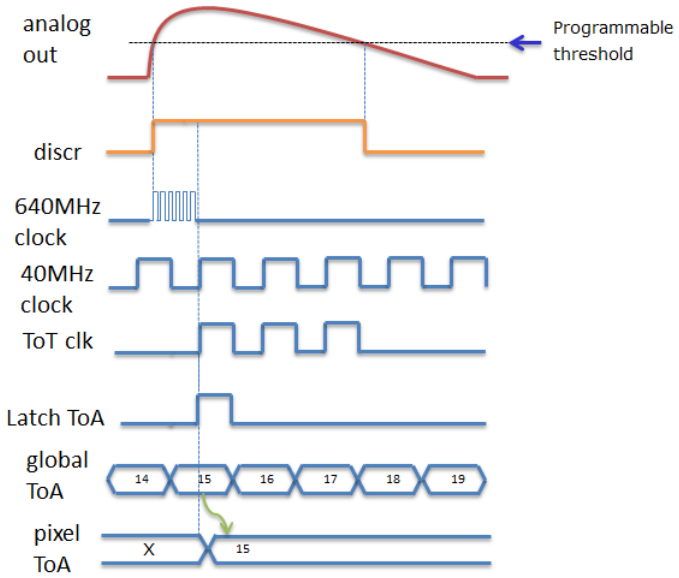

Figure 4. Operation principle of the Timepix3 pixel.

from this moment on. The coarse time stamp (ToA) is latched at the same time. As shown in figure 4, the time stamp counter (40 MHz) is distributed into pixels using a global (one per double column (DC)) bus instead of using a shutter signal as timing reference (as in [1]).

The SP logic is shared by 8 pixels, and can be accessed by only one pixel at time. This pixel is selected by the intra-SP token ring which receives a request signal from each pixel containing data. Data are shifted from a selected pixel into a deserializer in the SP, and written into a buffer for readout. The buffer has storage capacity for two events of data to reduce the dead-time of the digital pixel front-end. This allows continuous acquisition and readout with a relatively small dead-time of 475 ns per pixel (compared to 300 μs in Timepix). This dead time increases however when the chip is operating very close to its maximum hit rate and the data rate exceeds the available bandwidth.

Each SP accesses the column bus using token ring (round-robin) arbitration. This token arbitration is synchronous to the column clock and the token circulates from the top of the column to the bottom in 64 clock cycles. Data communication with End of Column (EoC) block is done using an asynchronous 2-phase handshake protocol (see [13]). Using this protocol, no absolute timing related to the clock signal is required. Data and handshake signals still require strict relative timing by ensuring the handshake signal (request) always arrives at the EoC after the data.

The chip also has two different readout modes. Shown in figure 3, the SP logic is controlled by a readout enable in these modes. In the first mode, the chip sends data off the chip as fast as possible without external command. This is called a data-driven mode, and readout enable is constantly high in the SP logic. In the second mode, data stays at the pixel level until an external readout command is provided. With this command, any number of columns from 1 to 128 can be read out in parallel. The columns which are not being read out have their clocks completely gated thus reducing power consumption. This readout mode is called a sequential readout mode.

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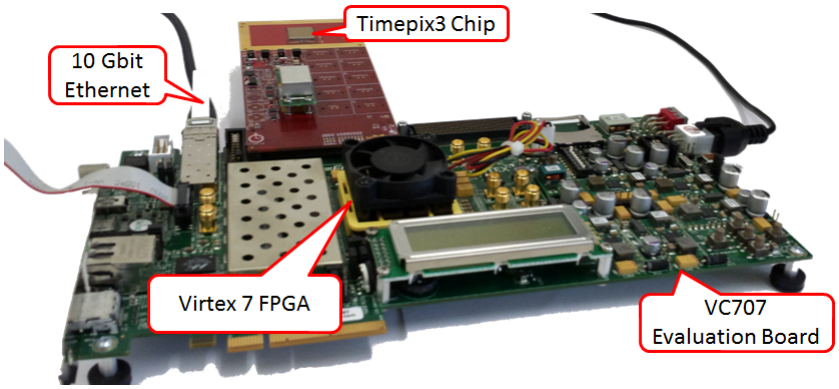

Figure 5. The test setup (Nikhef and CERN) for Timepix3 used to read out.

3 First measurements

The first batch of six Timepix3 wafers was received in August 2013. One wafer was diced and the testing of basic functionality of the chip started at the beginning of September 2013. The test setup for Timepix3 is shown in figure 5. The setup consists of a custom chipboard connected to an evaluation board. The system is controlled by a field-programmable gate array (FPGA) running a soft-core processor and data are sent to a desktop computer for offline analysis using 10 Gb Ethernet (10GbE).

The chip has been verified to be functional at room temperature, running at 40 MHz clock and from a power supply of 1.5 V. The pixel matrix configuration registers can be accessed via EoC logic and shift registers. All periphery registers are accessible via slow control logic and command decoder, and programmed register values are readable through the data links.

Both the analog- and the digital front-ends respond to on-chip generated test pulses as expected. Simultaneous ToA/ToT mode provides consistent charge and time information across the full matrix. First DAC scans have also been performed by configuring pixels to operate in event counting and integral charge mode. The mode has been observed to work as designed.

After compensating for clock and test pulse delays and injecting a test pulse simultaneously to all pixels, only two timing bins of 640 MHz were observed among all pixels. This is a clear indication that the VCO oscillation frequency across the full pixel matrix is very close to 640 MHz, and fine time stamping is performed correctly in the pixel logic. Compensation of top-down delays was done in software by using delay values obtained from hardware simulations. No left-to-right compensation for delays was done. Analog front-end is also fully functional and shows a noise performance $< 70\,e^-$ rms based on the first results (assuming a gain of 50 mV/k e^-). These figures have been obtained without a sensor bonded to the chip.

Measured minimum thresholds for pixels are shown in figure 6. Measured average noise in pixels is $60\,e^-$, and threshold dispersion after equalization is $35\,e^-$. From these numbers, the predicted minimum threshold is $400\,e^-$ (blue curve). Note that these values depend on the current settings of the preamplifier. The minimum threshold in the worst case (ToA/ToT, data-driven readout) is approximately $500\,e^-$. In figure 6 this indicates that when threshold is around $500\,e^-$ (red curve), one pixel starts to respond due to noise. When the threshold is decreased to $400\,e^-$,

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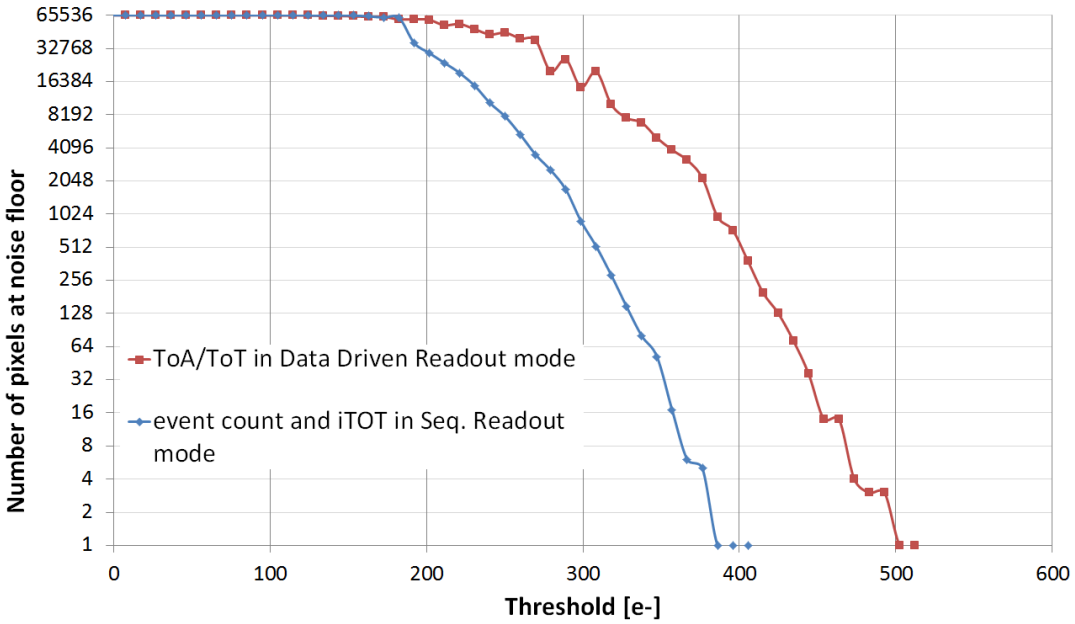

Figure 6. First threshold DAC scans of pixels in different operation/readout modes.

over 512 pixels are responding due to noise. There is a significant increase of about 100 e^- in the minimum threshold between different readout/operation modes. This is expected because in ToA/ToT mode time stamp counters (encoded in gray code) are constantly switching at 40 MHz. Also in data-driven mode the SP readout logic is active while in sequential readout mode the logic is completely idle.

Power consumption of the full chip has been measured to be less than the specified requirement of 1 W/cm^2. The measurements also show a throughput of 20 Mhits/s/cm^2 when running at 40 MHz clock. The periphery logic has been tested up to 80 MHz, and it is fully functional. All eight output links are also functioning at the maximum specified rate 640 Mbps.

4 Conclusions

The readout chip Timepix3 for hybrid pixel detectors (HPDs) has been successfully designed and implemented. Initial measurements match the simulated values very closely. Several new features for optimising the readout of a large number of integrated channels (65,536) have been demonstrated. The results shown demonstrate that the chip is working as expected in both the readout modes and in two different pixel operation modes.

The systematic characterisation of Timepix3 will continue and thorough investigation of full performance capabilities of the chip will be done later in 2013. Wafer probing and the qualification of the chips is also planned at the beginning of 2014.

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