IC Tester

Project Proposal and Feasibility Report submitted in partial fulfillment of the requirements for the Degree of Bachelor of Science of Engineering in

The Department of Electronic & Telecommunication Engineering University of Moratuwa

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Abstract

IC TESTER

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This report acknowledges a feasibility study of designing, prototyping, and testing an IC tester. The scope of this project basically covers development of a standalone computer software with GUI, digital design and implementation of digital IO driving unit, hardware design of electrical measuring instruments, power sources etc. Finally, the complete task is intended to be prototyped and basic tests like IDDQ test, continuity test, scan test, boundary scan and etc. will be implemented and demonstrated on digital ICs.

Current state-of-the-art in IC testing consists of very high-speed digital testing capabilities even up to 5Gbps, highly parallel testing capabilities along with automation in all possible areas. Teradyne, Advantest, LTX-Credence are some leading commercial vendors of Automatic Test Equipment (ATE). Price of an ATE tester from such a vendor is millions of dollars.

Ultimate motive of this project is to start IC testing in Sri Lanka. This first step of developing a locally made IC tester would create new business opportunities within the country. This report emphasizes that it is feasible to continue this project

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Acronyms and Abbreviations

IC	Integrated Circuit
VLSI	Very Large-Scale Integration
ATE	Automatic Test Equipment
DUT	Device Under Test
MCU	Microcontroller Unit
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
SPI	Serial Peripheral Interface
FPGA	Field Programmable Gate Array

1. INTRODUCTION

1.1 Introduction of IC Testing

Testing is a step followed in IC fabrication process to ensure the selected device has no manufacturing defects. In earlier times, IC designers only focused about the *speed*, *area* and *power* in optimization of the design. In contrast to that nowadays, *testability* has become the next factor which decides the quality of a design. According to the VLSI Realization Process the testing is placed as the process before delivering the chips to the customers.

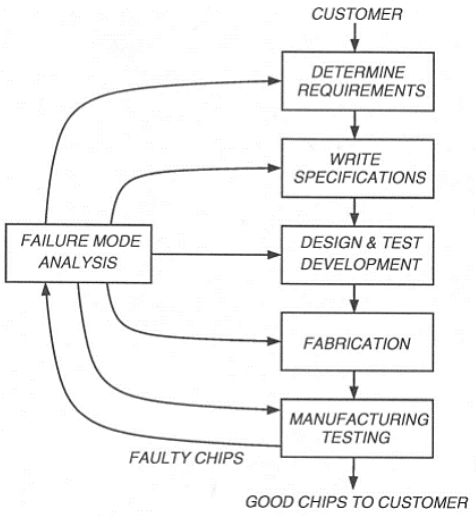

Figure 1-1 VLSI Realization Process

Generally, ICs are manufactured in large quantities on a single wafer by exposing to the processes such as photolithography. Before this wafer is cut into pieces in other words which is called as die preparation, to obtain individual circuits, all the individual circuits are tested for their functional defects which can be occurred by activities such as misalignment of films, faults with etching process, faults in materials and impurities. This process is known as *Wafer Testing*. Then, to prevent physical damage and corrosion, the dice are placed inside a supporting case. This process is named as *IC packaging*. Because there are mechanical and chemical processes involved in packaging, even after the wafer test is completed successfully, faults in IC can occur. For example, the bonding wires can be damaged or shorted in encapsulation, die can be misaligned and mutual

inductance and capacitance can appear. Therefore, it is essential to perform tests again before delivering good chips to the customers.

Both wafer testing and final testing after packaging are conducted by the machines called ATE. They can perform both *Parametric Tests* (such as output drive current test, leakage test etc.) and *Functional Tests* (check the proper functionality of chip nodes). High end testers consist of three components which are *test head, workstation,* and *mainframe*. Workstation can be identified as the user interface to the tester. A user can debug an IC through the software packages included in the workstation. Mainframe serves as the unit which includes parts such as measuring instruments, power supplies, digital driver unit etc. The test head contains more sensitive equipment which needs less distance to the DUT. Some of the ATE machines manufactured by commercial vendors are as follows

Figure 1-2 Teradyne UltraFLEXplus

Figure 1-3Teradyne J750Ex-HD Family

- 2.2Gbps digital performance
- 512 digital channels per instrument
- 256 Power supply channels

Price – Approximately $2 Million

- 400 Mbps digital performance
- 2048 multifunction pins
- Parallel IC testing capability

Price – starting from $99,000

1.2 The Problem Statement

IC manufacturers perform tests within their manufacturing plant or outsource the chips to other companies who carry out the procedure. Since the chips are tested by high end testers, similar to

the ATE machines mentioned above, it costs a considerable amount of money for the procedure. A company which facilitates the IC testing process can be considered as a successful business in the silicon industry.

Currently in Sri Lanka, ATE machines are not available to perform tests for ICs. It would be an immense opportunity for the electronic industry in the country as well as a door opening for job market if an IC tester can be manufactured in Sri Lanka.

1.3 Primary Objectives

Primary objectives of this project can be listed as follows.

1. Design and prototype a low cost scaled down hardware software solution for digital IC testing

   The IC tester is expected to **test the packaged digital ICs** and the design is **exclusive of automatic probers and handlers**. A user can program the IC tester with the user interface provided.
2. Demonstrate the functionality with basic tests for selected packages of digital ICs

   Tests such as continuity test, Iddq test and scan test are planned to be performed for multiple IC packages i.e. DIP14, DIP16, DIP28.
3. Taking the first step to develop a Sri Lanka made IC tester

   IC testers are not available in the current electronic industry in Sri Lanka. Manufacturing such a tester can be a good business opportunity for sub-contracting IC test process inside the country. The tester expected to develop in this project has compromised functionality of an industrial scale tester but, with improvements in future it can be brought out as an industrial scale IC tester.

1.4 Scope

There are mainly 5 areas where the scope of this project can be categorized.

1. Standalone cross platform computer software with GUI

   This software provides the interface between the tester hardware and the user. It is based on QT C++ framework, embedded SQLite Database Management System and a USB interface with the tester hardware.

2. Embedded firmware development

   Data transfer and signal control between the computer software package, digital driver unit and pin cards are handled by the STM32 MCUs. Protocols such as UART, USB and SPI are expected to be included in the firmware.

3. Digital design and logic driving unit

   This unit will be implemented as an FPGA design with Verilog. Up to 20Mbps data rate will be maintained in the 128 I/O ports. Maximum parallel capability will be 32 inputs and 32outputs at a time.

4. Hardware Designing and Prototyping

   Multiple programmable power supply units will be included with various voltage ranges, current limits, and resolution.

   Ex: 0-5V power supply with 1.5A current limit and 10mV resolution

   Programmable current source is expected to be designed for the tester. A voltmeter with milli Volt range and a current measuring unit capable of measuring up to nano Ampere range are included. Although the complete design will contain 16 pin cards, for the prototype 2 pin cards will be added including the programmable switching and routing circuitry and power and control circuitry.

5. Implementing basic tests on suitable ICs.

   Following tests are planned to establish in the tester. Continuity testing, Iddq testing, Scan testing, Boundary scan testing, Functional testing and Bypass Testing.

   DIP14, DIP16, DIP28/ DIP40, SOC16, QFP/ TQFP/ LQFP48 are the IC packages planned to be tested for demonstration.

1.6 Uniqueness and National Importance of the Project

The end prototype of this project will be an initiative step to design a Sri Lankan made IC tester. Since IC testing is not currently an industry in Sri Lanka, this will be a precious opportunity to start subcontracting in IC testing. In our scope the IC testing is expected to be performed for only

packaged ICs. By designing and developing automatic probes and arms and improving the capability this tester can elevate to wafer testing level.

One of the intentions of this project is to minimize the cost of the product. Powerful IC testers contain high end instruments such as power supplies, voltmeters purchased and placed off the shelf from such commercial instrument manufacturers. In our design to minimize the cost in our design, units such as power supplies and voltmeters are designed by us. Even though it will degrade the capability of the tester, still selected digital ICs with low complexity can be tested from our tester.

1.7 Potential Customers/beneficiaries

The long-term goal of this project is start IC testing in Sri Lanka. The end product of this project can be considered as the first leap of IC testing in the country and with the time being by adding sufficient amount of equipment and knowledge, a commercial IC testing service can be formed in Sri Lanka.

This IC tester can also be sold in the market as a commercial product specially for part suppliers who handle low quantity custom made ICs and low volumes of FPGA chips programmed with custom digital designs.
E.g. oscilloscope manufacturers, telecommunication equipment manufacturer.

Additionally, it is possible to market the product as a test bench for electronic research and development, repair and maintenance. Electronic sign engineers can be considered as an example for this customer base.

2. LITERATURE REVIEW

2.1 Generic Architecture of State-Of-The-Art IC Testers

Automated Test Equipment (ATE) are widely used in the semiconductor industry for manufacturing testing of ICs. Some popular commercial vendors of ATEs are *Teradyne*, *LTX-Credence*, *Advantest*, etc.

A high-performance tester with a fully upgraded configuration may cost around two million dollars in average. Targeting only s specific class of devices with designs for testability, a test system with a reduced configuration can be bought for a price as low as hundred thousand dollars. Probers and handlers which handles the automation of picking, placing and probing may cost about half a million dollars additionally.

2.1.1 Major Components of High-end ATE testers

- Test head
- Workstation
- Mainframe

Workstation is the computer providing a user interface to the tester. Test programs are written, executed and debugged from the workstation with the tools provided by ATE vendor. When tester is used in a production line, workers can control and monitor its day-to-day operations using the workstation.

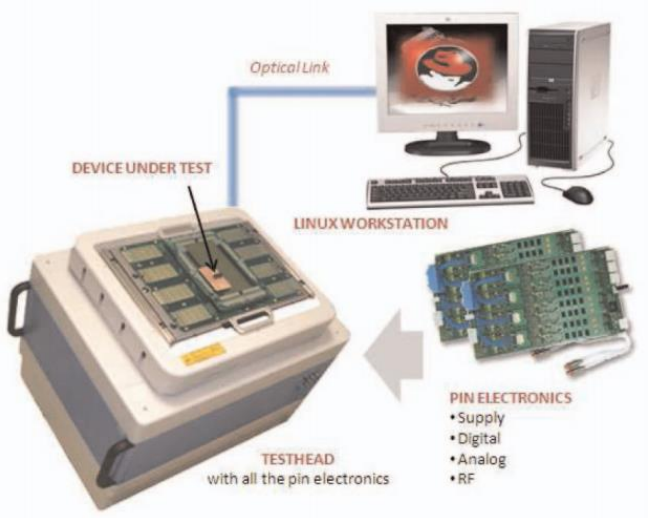

Figure 2-1 Major Components of an ATE tester

Mainframe consists of all the major internal hardware of the tester such as measuring instruments, power supplies, current sources, loads, switching and control circuitry, etc. It normally has separate subsystems for dc power, digital testing, analog testing, etc. It may also have a robotic manipulator for positioning of the test head. Normally a refrigeration system providing coolants to regulate the temperature is also there.

Test head contains highly sensitive test equipment that require close proximity to the device been tested. Mostly the measuring instruments that need to be right at the pins or pads of the device

under test (DUT) are there in test head. For example, digital I/O data streams with high speed require shorter electrical paths between the I/O pins of the DUT and the IO driving ports of the tester. That is why digital drivers of ATE testers are normally located in the test head.

2.1.2 DUT Interfacing

Device Interface Board (DIB) provides electrical connections between the ATE and the DUT. Depending on the ATE vendor's technology some other names are also commonly used for the DIB such as swap block, performance board, family board, etc. Shape and size may differ from DIB to DIB, but all of their main purpose is to provide a socketed electrical connection between the test instruments of the ATE and the pins or pads of the DUT.

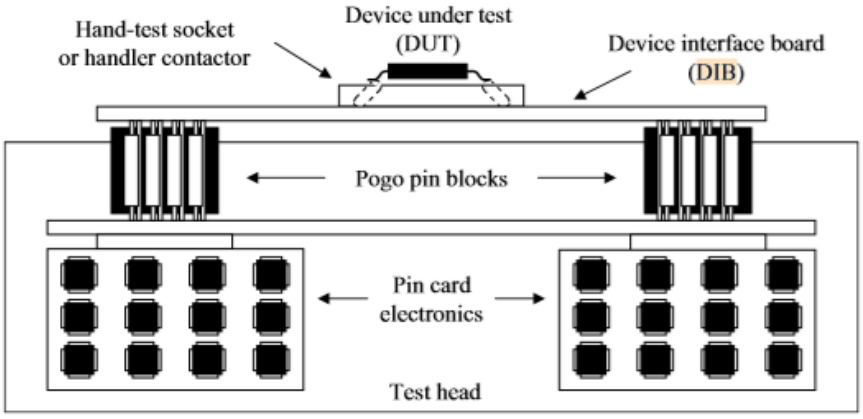

Figure 2-2 ATE test head to DUT interconnections

Following Alternative methods are also used in interfacing the ATE with the DUT.

- Wafer Probers
- Handlers (for packaged devices/ ICs)
- Focused Ion Beams
- Focused Temperature Systems, etc.

2.1.3 Tester Hardware Architecture

ATE comprised of following hardware units.

- General purpose voltage/current sources
- Voltage, current measuring instruments
- Switching matrices
- Digital pin cards

Figure 2-3 Hardware inside an ATE

- Arbitrary waveform generator and waveform digitizer
- Time measurement system
- RF subsystem
- Computing hardware

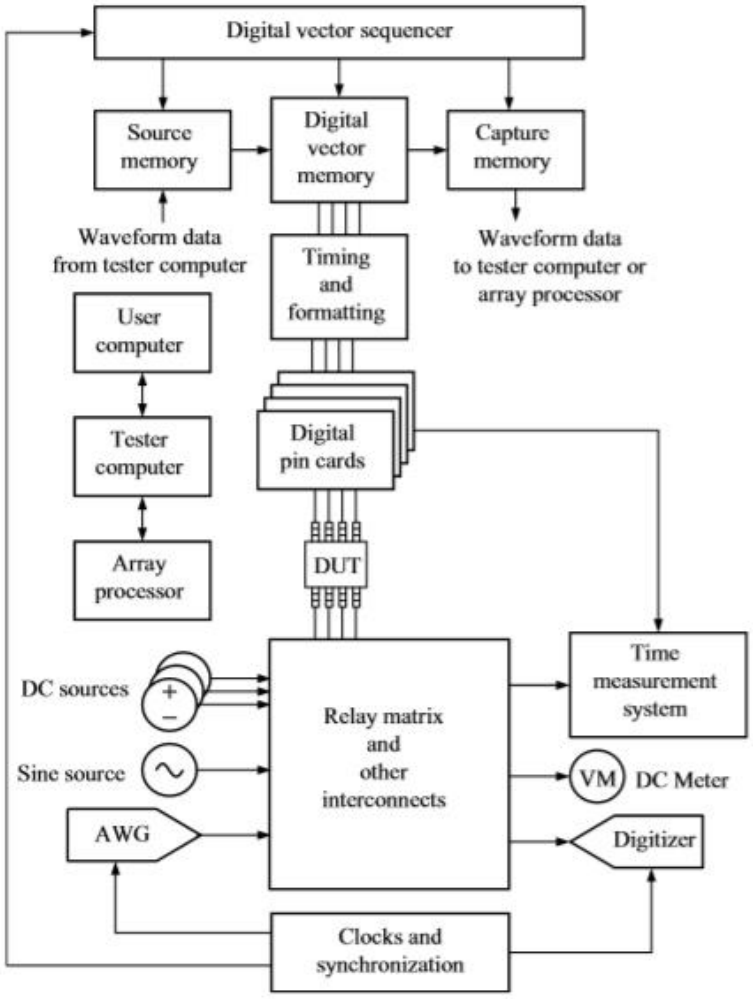

Figure 2-4 Generic ATE architecture

2.1.4 Test Flow

Following diagram shows a general flow chart of testing an IC which starts with continuity testing. The continuity check simply measures the voltage across the protection diodes of the DUT pins, by forcing a small current, in order to make sure that the DUT is well connected to the tester. Then one after another different functional tests, DC tests, AC tests, digital tests are performed to the IC

being tested. In each stage if a test is failed the IC is rejected. Both good and bad ICs are sorted in to bins.

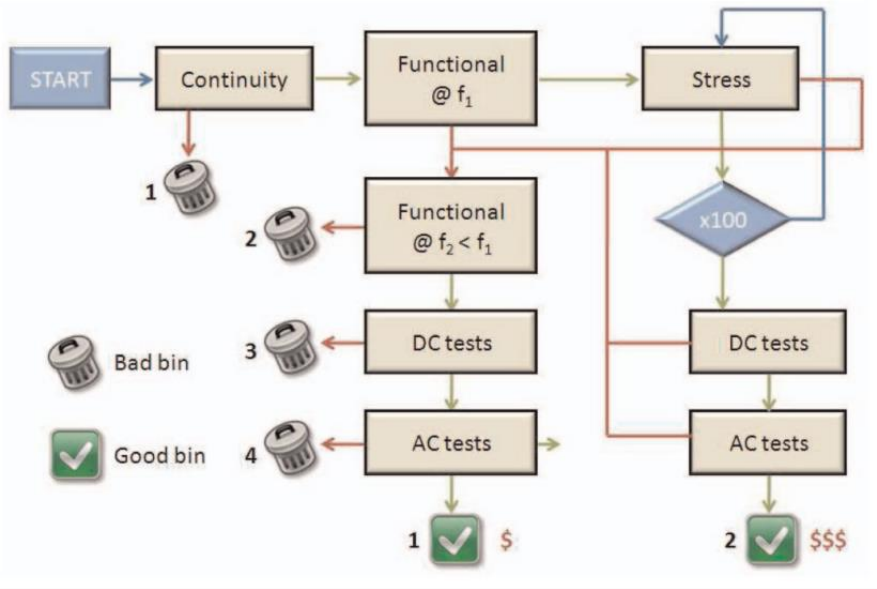

Figure 2-5 Example of Test Flow

2.2 Alternative Methodologies of Testing

Apart from high-end ATE testers used in manufacturing testing in IC fabrication, there are other methodologies which can be used to test ICs but with different purposes like below.

- Test equipment for manually performed electronic test and repair (mainly for PCBs, soldered components)
- Combinational logic level handheld IC testers and IC detectors

Figure 2-6 Probing soldered components for testing

Figure 2-7 PCB testing test equipment for R&D purposes

Following figure shows how testing R&D purposes is performed in an industrial environment.

A test module aimed at testing all digital ICs and PCBs from all logic families.

Multiplex matrix switch with a 16x16 switch matrix interface

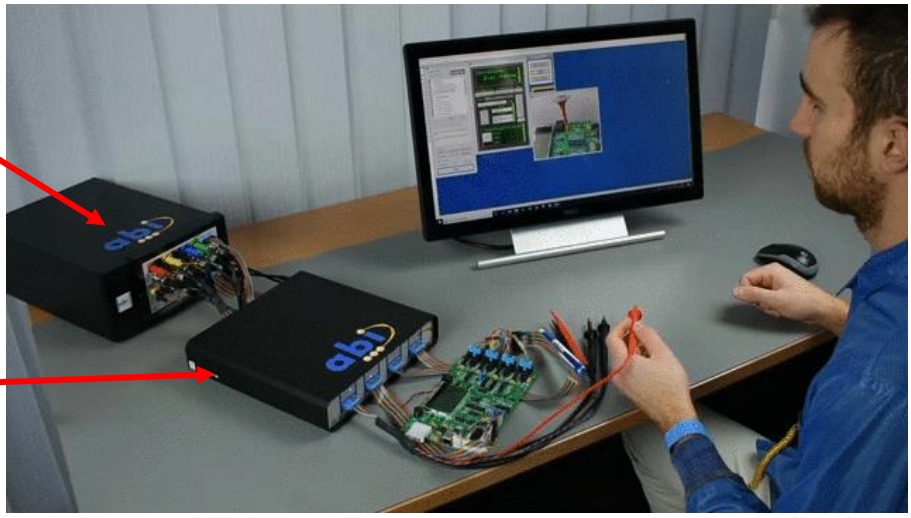

Figure 2-8 R&D Level Testing

Figure 2-10 A hand-held IC Tester

This picture shows LinearMaster Compact Professional by Abi Electronics which is a handheld IC tester which can do simple logic testing for ICs with up to 16 pins. It has a large embedded database to detecting unknown ICs as well.

Sentry Counterfeit IC Detector by Abi Electronics is a larger version of the previous one which has 256 test channels. Apart from identifying unknown ICs it can easily detect missing or incorrect dies, lack of bond wires, inaccurate pinouts and pin impedance variations. Simple pass or fail results are returned after testing.

Figure 2-9 A bench IC tester

3. METHODOLOGY

3.1 Project Architecture

3.1.1 Block Diagram

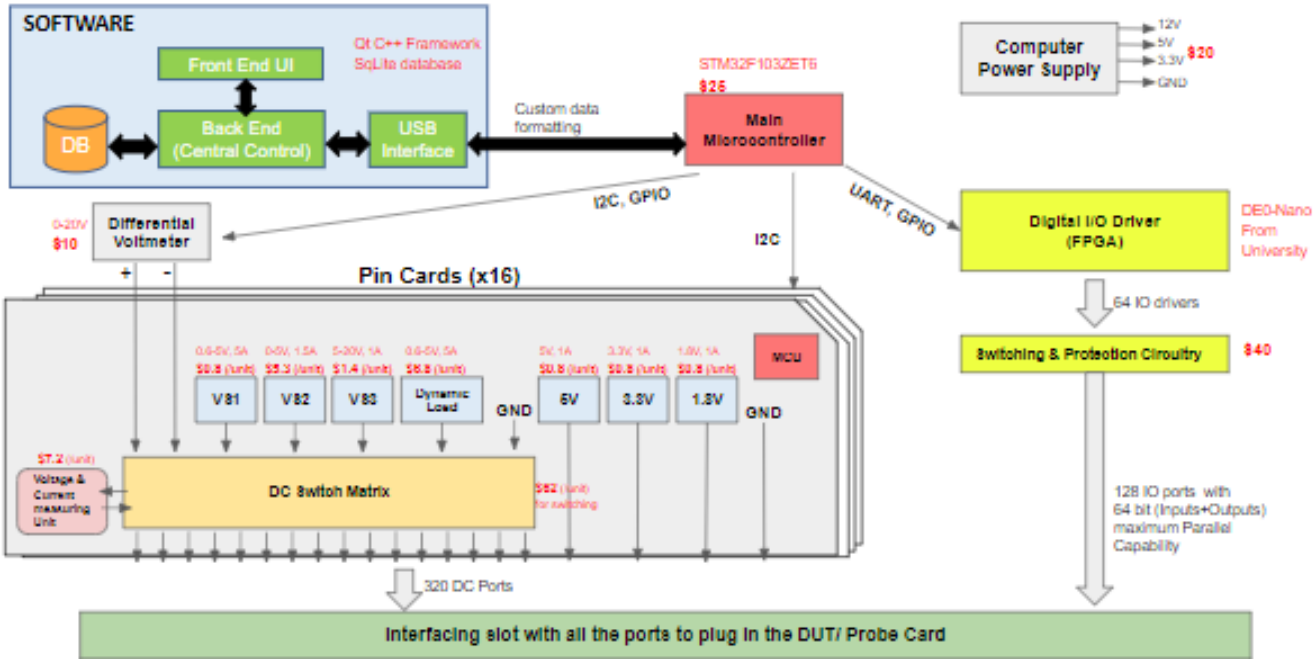

Figure 3-1 Block diagram of the project architecture

IC Tester Software is developed as a stand-alone desktop application using Qt framework with backend in C++ language. Moreover, this software is the top level of the control hierarchy of the IC tester. Front end UI is made as a Qt widget application. In the backend, the input data from the user interface which are recorded in the database are converted to a format comprehensible by the main microcontroller. SQLite is used as the DBMS for this desktop application. USB serial communication is used to communicate between the desktop application and the STM32 microcontroller.

Main Microcontroller (STM32F103VET6) is the main control unit inside IC tester hardware. It retrieves commands from the computer software via USB serial communication and then the received data packets are decoded in order to understand the commands. Then according to those commands, the main microcontroller delegates tasks to each individual hardware units of the whole tester.

Digital I/O Driver, protection and switching circuitry is the digital subsystem of the tester which mainly consists of 2 FPGAs, one for sourcing digital data to input pins of the DUT and the other for capturing digital data from output pins of the DUT. These two FPGAs have 32 digital drivers each which make the maximum parallel capability of the tester up to 32 bit. Furthermore, the FPGAs have the ability to change the clock speed as desired.

The interfacing I/O pins of the FPGA goes through protection and switching circuitry. A single I/O driver is connected to 2 digital I/O ports of the tester via relays, one with 3.3-5V logic conversion.

Pin cards used in the tester are pluggable based on the requirement where 16 such cards are used in total having 20 DC interfacing ports each. Hence the total number of ports of the IC Tester sums to 320 ports. Out of the 20 DC pins in each pin card, 16 pins are multipurpose because they are switchable through a DC switch matrix and the other 4 pins are directly connected to fixed voltage sources. Voltage and currents of each individual pin can be measured with the voltage and current measuring unit in each of the cards. All the relays, multiplexers and shift registers are controlled with a dedicated MCU in the pin card which also communicates with the main MCU of the IC Tester.

Differential voltmeter is common to all the 16 pin cards so that it can measure voltage between any 2 ports out of 320 ports in the IC tester.

3.1.2 Flow Chart

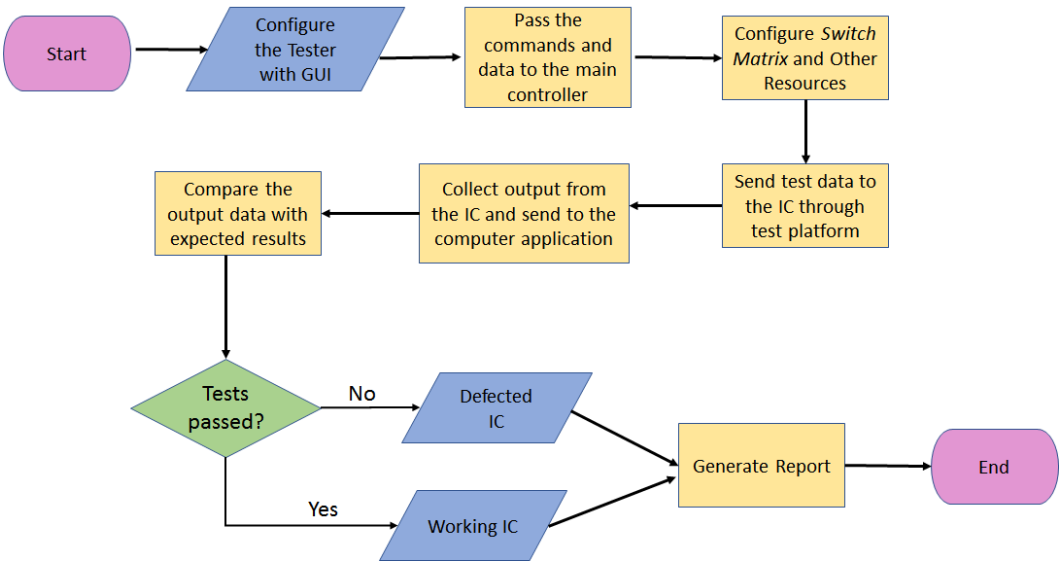

Figure 3-2 Flow chart of the project architecture

3.2 Evaluation of Alternative Methodologies

IC Tester Software framework alternatives

Being more hardware related and more of on-site testing, a standalone desktop application is more suited than a web or mobile application. Out of the following frameworks suitable for developing standalone applications, Qt was selected.

Alternative	Pros	Cons
Qt (C++)	Cross-platform C++ more supportive for hardware High community support Better GUI designer, being faster than other languages Good documentation	Complexity to the build process
.Net (C#)	Reliable and simple caching system Large community	Mainly used in windows Memory leaks Limited object-relational support
JavaFX (Java)	Cross-platform Open source Java being the most popular programming language in the world	Not quite mature enough Not very supportive for hardware related projects Comparatively low Performance

Table 1 Alternatives for desktop application frameworks

DBMS alternatives

Out of the following options, SQLite was selected being a serverless (embedded) database that runs as a part of the application.

Alternative	Pros	Cons
SQLite	Lightweight in setup, administration, and required resource Embedded, server-less database Best suited for standalone apps, specially Qt widget applications	Comparatively smaller library size
PostgreSQL, MySQL	The world's most advanced open source database Improved security	Requires a DB server Difficult to setup with Qt compared to SQLite

Table 2 Alternatives for Database Management Systems

Power supply units

In making power supplies in the IC tester, we decided to proceed with making our own power supplies due to the low cost and flexibility.

Alternative	Pros	Cons
Use industrial grade power supplies ($1200 per unit)	High precision and high reliability Wide range of operation Functionality can be monitored through a network	The range of operations exceed the limits of our design. The cost over number of configurable channels is too high.
Use power supply modules	Voltages and currents can be programed	The range of operations exceed the limits of our design. Low programmability
Designing our own Power supplies	Can be designed to match the desired requirements.	Can have design errors.

Table 3 Alternatives for power supply units

Digital I/O driver

Due to the cost effectiveness, we decided to implement our own design with FPGA.

Method	Advantages	Disadvantages
Use source and capture modules	High data rates (ex: 200 MHz) Widely programmable IO levels Built in pattern generators	The cost of a single module is too high (32 bidirectional channel, 2 logic voltage level modules with 10MHz clock - $1600)
Implement our own design with FPGA	Available in the university for initial testing	Limited embedded memory Protections methods are not available for pins (ESD, over voltage, over current)

Table 4 Alternatives for digital I/O drivers

3.3 Risk Analysis

Risks	How to overcome?
Limitation of affordable shipping methods due to Covid-19	Order components from the same supplier, together with the other groups to share shipping cost.
Inability to get together due to Covid-19	Using online collaboration platforms as much as possible. Ex: Zoom, Atom Teletype, EasyEDA, etc.
Hardware design faults lead to huge additional costs and time.	Every hardware design task is carried out with the collaboration of at least two members. Choosing components by carefully going through datasheets of number of suitable candidates. Going through thorough design verifications.

Risk of a selected component being out of stock	Keep alternative components selected. Choosing components which are available with 2 selected suppliers (Digi Key, LCSC)
Common resources with the university being unavailable due to other utilizations.	Communication with the relevant labs and do reservations based on requirement.

Table 5 Risk Analysis

3.4 Resource requirements and budget

Cost Categories	Total Cost (2 pin card)
Device power supply and wiring	$40
Programmable Power Supply units of the tester	$34
Hardware for switching & routing with a DC matrix	$123
Voltage & Current Measuring Instruments	$31
Hardware for Digital I/O System	$32
Passive Components	$20
Enclosure Cost	$30
PCB cost	$40
Shipping cost	$384
TOTAL	**$734**

Table 6 Total budget of the project

Since our project is very hardware intensive, electronic components were selected from two different suppliers (DIGI Key and LCSC) and the budget was prepared mainly with the quotations of those electronic components which are listed below.

Manufacturer	Man. Part No	Qty	Unit Price	Cost
On Semi	NTMFS4C022NT1G	17	$0.261	$4.437
Omron Electronics	G5NB-1A-E-DC12	142	$0.250	$35.500
TE Connectivity	1649222-1	36	$0.350	$12.600
Texas Instruments	ULN2003A	24	$0.120	$2.880
On Semi	74HC595	24	$0.114	$2.736
On Semi	MMBT2222ALT1G	17	$0.009	$0.153
ST Microelectronics	STM32F103C8T6	1	$2.000	$2.000
Texas Instruments	CD74HC4067SM96	3	$0.470	$1.410
				$61.716
Total for 2 pin cards				$123.43

Table 7 Budget for the major components for DC switching and routing

Manufacturer	Man. Part No	Qty	Unit Price	Cost
Omron Electronics	G5NB-1A-E-DC12	8	$0.250	$2.000
TE Connectivity	1649222-1	4	$0.350	$1.400
Maxim Integrated	MAX4239AUT	2	$1.000	$2.000
Texas Instruments	ADS1115	3	$3.170	$9.510
Texas Instruments	LMV321	2	$0.170	$0.340
Texas Instruments	ISO1541DR	2	$1.170	$2.340
Analog Devices	REF02CSZ-REEL7	2	$2.081	$4.162
Analog Devices	OP1177	4	$1.547	$6.118
Texas Instruments	TPL0102	2	$1.760	$3.520
				$31.390

Table 8 Budget of the major components for measuring instruments and dynamic loads

Manufacturer	Man. Part No	Qty	Unit Price	Cost
Texas Instruments	TPS56528DDAR	2	0.59	1.18
Analog Devices	LT3081	2	5.32	10.64
Texas Instruments	TPS54202	2	0.39	0.78
Texas Instruments	TPS7A7001DDAR	6	0.77	4.62
Texas Instruments	TPL0102-100RUCR	10	1.417	14.17
SXN	HSMS0650-3R3M	2	0.21	0.42
TDK	RLF7030T-6R8M2R8	2	1.009	2.018
				$33.828

Table 9 Budget of the major components for power sources

3.5 Task Delegation

Preliminary tasks | Digital design and implementation | Hardware design | Software and firmware development | Testing and prototyping

Task	Nalith	Yasara	Thilina	Lahiru
Literature review and exploring possible methods				
Designing programmable power supply units				
Designing voltage and current measuring instruments				
Designing a programmable dynamic load				
Design of hardware for switching and routing in the tester				
Hardware design of Digital I/O subsystem				
PCB design				
Front end software development (standalone GUI)				
Backend software development and database management				
Communication Interface between the PC and Tester				
Firmware development				
Digital design of digital I/O subsystem on a FPGA				
Hardware prototyping with wiring, soldering, etc.				
Electronic testing & debugging of prototypes				
Software & firmware testing of prototypes				
Documentation				

Table 10 Task delegation among the group members

There are 4 major categories of work in the project and all 4 members take part in tasks from all those 4 categories, for better efficiency and productivity. But major contributions of the members can be summarized as, Nalith and Yasara more focused on firmware development, software switching and control while Thilina and Lahiru contributing more for hardware and digital design.

3.6 Timeline

Task	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Literature review and exploring possible methods											
Designing programmable power supply units											
Designing voltage and current measuring instruments											
Designing a programmable dynamic load											
Design of hardware for switching and routing in the tester											
Hardware design of Digital I/O subsystem											
PCB design											
Front end software development (standalone GUI)											
Backend software development and database management											
Communication Interface between the PC and Tester											
Firmware development											
Digital design of digital I/O subsystem on a FPGA											
Hardware prototyping with wiring, soldering, etc.											
Electronic testing & debugging of prototypes											
Software & firmware testing of prototypes											
Documentation											

Table 11 Timeline

3.7 Initial Results

Software

- ✓ USB communication tested and working.
- ✓ DBMS handling tested and working.
- ✓ UI design that is currently being developed is shown in below diagram.

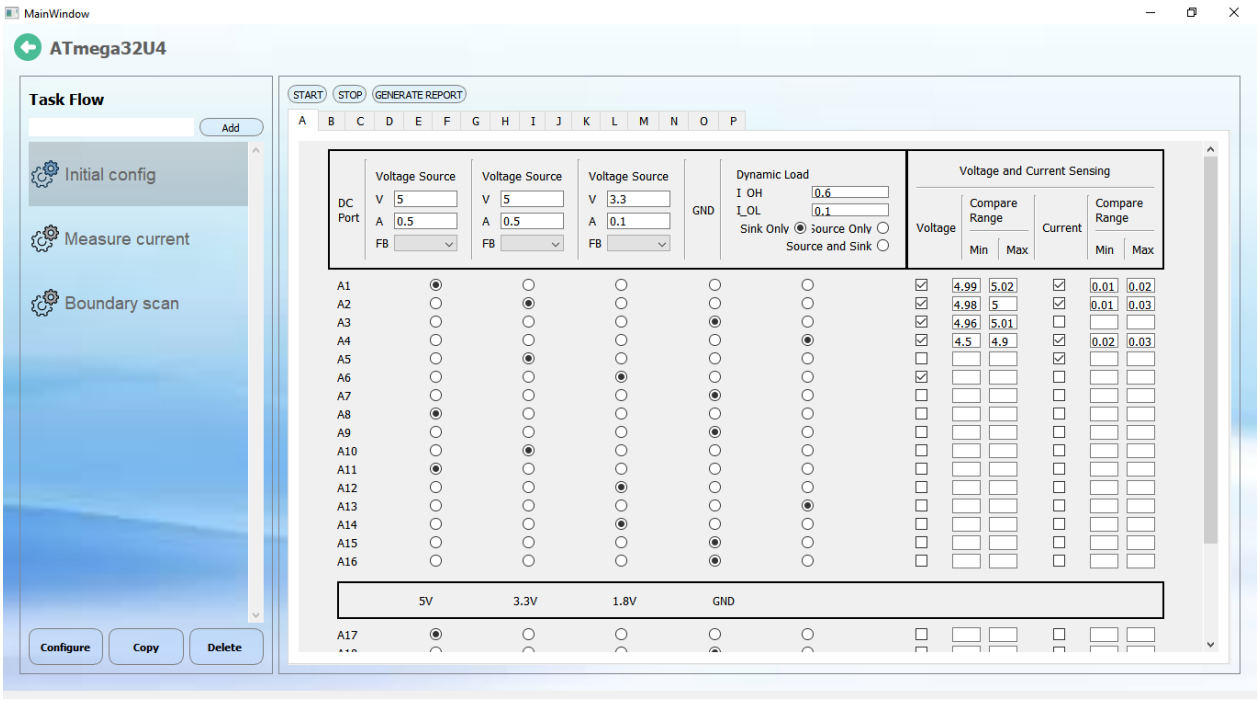

Figure 3-3 IC Tester software user interface

Hardware

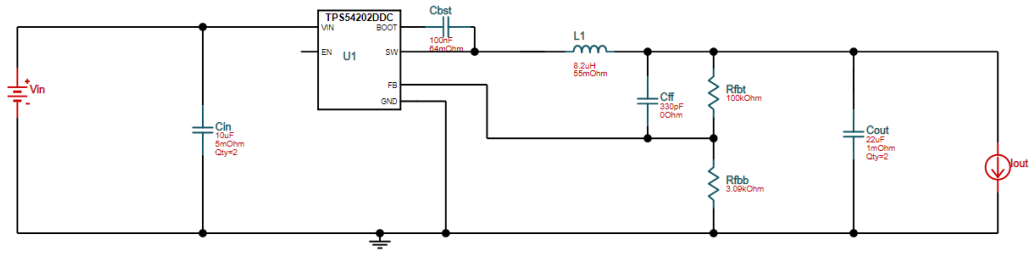

Figure 3-4 5V-20V, 1A power supply design with TPS54202 step down converter

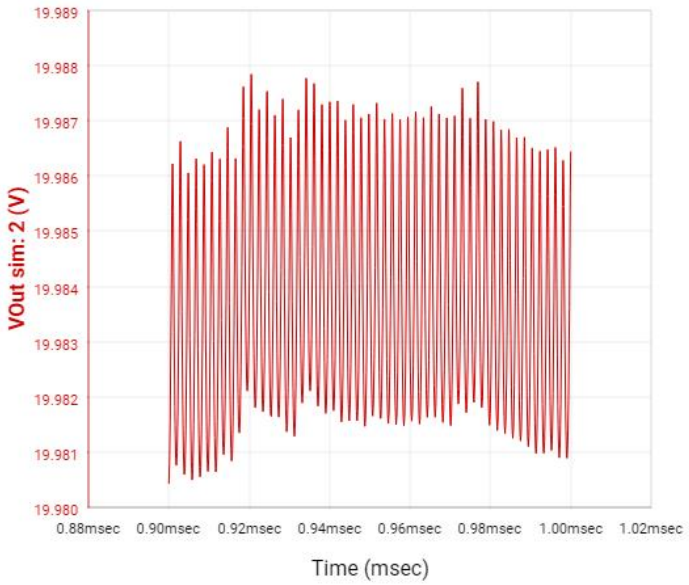

Figure 3-5 Steady state simulation results for power supply design with TPS54202 step down converter

4. DISCUSSION AND CONCLUTION

4.1 Main findings of the literature survey

The Literature survey was mainly carried out in three stages. On the first stage, we analyzed the production cycle of Integrated Circuits (ICs) and the importance of IC testing during the production. It was reviled that the testing is done in two production stages which are after the wafer (die) is produced and after the IC is packaged. Through these tests, ICs with manufacturing defects are identified. Further, functional ICs are categorized into several grades based on their performance. Since our scope only extends to testing packaged ICs, we mainly focused on identifying the manufacturing faults that occur during the packaging stage such as die misalignments, shorted or missing bonding wires and mutual inductance between bonding wires. Further, we analyzed the electrical tests that we can carry out to identify such defective ICs and also selected the types testes and determined complexity of each test that we are going to implement in our design within the scope of the project.

On the second stage of the literature survey, we were mainly focused on the hardware architecture of a generic IC tester. On the top level, an IC tester is a collection of discrete hardware units which functions as a power source or a data sourcing/capturing device or measuring device. These individual units are controlled by a central processing device to perform the tests which are pre-programmed by the user. It was identified that every IC tester regardless of its performance and capabilities, must contain at least one hardware unit of these three categories. The number of individual hardware units, the capabilities of each unit and the processing capability of the tester defines the types of tests and the complexity of each test that it can perform. With that knowledge, we calculated the resource requirements to implement the tests which we selected in stage one and then determined the number of hardware units and the specifications of each unit.

On the third stage of the literature survey, we reviewed and analyzed the existing IC testers available in the market. It was identified that there are three different kinds of testers available in the market targeting different sectors. IC testers for IC suppliers are the most expensive and most complex type of testers. They are produced in very small quantities and they are highly customizable. The second kind of testers is aimed at the research and development sector. They

are less expensive, less complex but more user friendly. Apart from testing ICs, they can be used as test benches to test electronic products and assembled PCBs. The third kind of testers is aimed at electronic repairing sector. They are the least complex testers and they perform very basic tests on a limited range of ICs. These testers are mostly used in electronic repair shops.

Since our project is focused on testing packaged ICs for manufacturing faults, we further looked into the hardware design of such IC testers. It was reviled that all of those testers use industrial-grade rack-mounted powers supplies and multimeters from reputed third party manufactures for its power and measuring units while using their own technology to design data source/capture devices. It was further noticed that the usage of such third-party modules largely increases the overall cost of the IC tester. With that knowledge, we thoroughly analyzed the available solutions, technologies and methods to implement the required hardware resources that we selected in stage two. After analyzing all the alternatives, it was found that to meet the specifications of each hardware unit while maintaining the coverall production cost at a minimum, it is required design and prototype all hardware units by ourselves.

4.2 Feasibility of the Project

4.2.1 Technical Feasibility of the Project

The technologies we are going to use in the project are neither very new nor cutting-edge. In terms of software development, it is required to develop a GUI for the IC tester, implement the communication between the computer and the embedded controller and program the embedded controller. We planning to achieve these tasks using the QT framework and C++ which are widely used for similar tasks and has great community support. In terms of hardware development, we are mostly working in the low and mid-frequency analogue electronic domain. We have already learned all the required fundamental knowledge from the course modules. It is required to develop several PCBs, assemble and test them. We are planning to use the student versions of Altium designer which is available at the university to design the PCBs and to use the soldering stations in the electronic workshop to assemble the PCBs. For testing and calibration of the PCBs, the equipment available in the university laboratories such as oscilloscope and bench multimeter is sufficient. Considering the above facts, we can consider that the project is technically feasible.

4.2.2 Financial Feasibility of the Project

The project is not sponsored by and external party and it is fully funded by the contribution of the four members of the group. We initially plan to contribute Rs. 35,000 per head. The roughly estimated budget for the project considering many worst-case scenarios totals to $1893 for the full design. But the design is modular and scalable since it has many repairing hardware components. The full design of the tester has 16 pin cards which result in 256 test channels. However, it was found that, for the demonstration purposes, only two pin cards which offer 32 test channels is sufficient. It would bring down the project cost to $730 which is within our initial budget. It is noticeable that about ⅓ of the total project cost comes from the shipping charges for PCB and electronic components. However, we are looking forward to combining PCB and component orders with other groups where we can share shipping charges which ultimately reduce the project cost. We are also looking forward to utilize university resources as much as possible to bring down the total project cost.

4.2.3 Social Feasibility of the Project

The ultimate goal of this project is to take the first step forward to design a low-cost IC tester which is to be fully assembled in Sri Lanka and subcontract IC testing for international electronic component suppliers. This is a very low quantity product. The users of this IC testers would be a small fraction of the society who are will be owning, operating or repairing these testers. Apart from those who particularly have an interest in IC testing, there will not be any significant effect on the general public caused by launching this product. Therefore, it can be considered that the project is socially feasible.

4.3 Impact of the Project

4.3.1 Local Impact of the Project

IC testing is an essential and unavoidable step in IC manufacturing. Therefore, it has a growing market. But IC testing is currently centered around the developing countries. The main obstacle which prevents a developing country like Sri Lanka entering the IC testing industry is mainly due

to the high cost of the IC testers which extends beyond a million dollars per single machine. The main objective of this project is to develop a low-cost IC tester which can be afforded by Sri Lankan companies and start subcontracting IC testing for electronic component suppliers. This will expose Sri Lanka to a new market segment in the electronic industry while creating tons of new job opportunities. These IC testers will require electronic test engineers to develop tests and program the testers. In the long run, it will be possible to introduce new engineering field which focused on electronic testing.

4.3.2 Global Impact of the Project

The introduction of a Low - cost IC tester from Sri Lanka which can be used to test ICs after manufacturing will urge other countries to develop similar products. With many countries entering into the IC testing market will be able to provide significant competition to the current IC testing market which is centered around the developed countries. Testing cost takes about 30 to 40% of the IC's market value. With the integration of low-cost testers, it is possible to decrease testing cost which will ultimately reduce selling prices of ICs making them more affordable.

4.4 Conclusion

Looking at the discussion of feasibility and significance, it is evident that the project is feasible within the selected scope. All the technologies which will be used in the project are wildly used and proven to work. The project can highly utilize the resources available in the university. Although the project is not backed by any third party, the estimated cost of the project considering many worst cases does not exceed the available budget. Further, At the end of the feasibility presentation, the ENTC staff, a group of highly experienced and reputed academics agrees that the project is feasible in all aspects and complex enough as a final year project. Being the first step to exposing Sri Lanka to the IC testing industry which will result in many new job opportunities, this project has a large local and global impact. Therefore, we arrive at our conclusion which is, design and prototyping a Low-Cost IC Tester is a highly feasible and a globally and locally significant project to be chosen and carried out as a final year project of the Department of Electronic and telecommunication engineering.

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