

AUTOMATED TEST EQUIPMENT FOR DIGITAL INTEGRATED CIRCUITS



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Declaration

This declaration is made on August 12, 2021.

Declaration by Project Group

We declare that the dissertation entitled Automated Test Equipment (ATE) for digital ICs (i.e., IC Tester) and the work presented in it are our own. We confirm that:

- this work was done wholly or mainly in candidature for a B.Sc. Engineering degree at this university,
- where any part of this dissertation has previously been submitted for a degree or any other qualification at this university or any other institute, has been clearly stated,
- where we have consulted the published work of others, is always clearly attributed,
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- with the exception of such quotations, this dissertation is entirely our own work,
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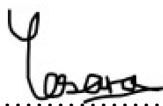
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Abstract

AUTOMATED TEST EQUIPMENT (ATE) FOR DIGITAL ICS

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Keywords: Digital Integrated Circuit (IC) Testing, ATE, Field Programmable Gate Array (FPGA), Electrical Measuring Instruments, Programmable Power Supply, Graphical User Interface (GUI)

This report acknowledges the evaluation of the results of a final year undergraduate project. The objective of the project is designing, prototyping, and testing an Automated Test Equipment (ATE) for digital Integrated Circuit (IC) testing. In fulfillment of the original scope, all the tasks of the project have been completed and they consist of developing a standalone IC Tester software with a Graphical User Interface (GUI), developing firmware and communication interfaces, digital design on Field Programmable Gate Arrays (FPGA), designing and prototyping of hardware for the main control unit, programmable power supply units, electrical measuring instruments, switch matrix units and finally, testing some digital ICs with the complete assembly of all the hardware components.

This report summarizes individual results obtained by evaluating the performance of each of the hardware components and the computer software. With the final assembly of the tester, a few digital logic ICs were tested with basic tests such as quiescent supply current (IDQ) testing, continuity testing, and digital input-output (I/O) testing. With the favourable results obtained from the project, the conclusion is that the development of this test equipment can be continued further for industrial IC testing in Sri Lanka.

Dedication

To our families, friends, supervisors, and all others that supported us in this work.

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Acronyms and Abbreviations

PCB	-Printed Circuit Board
FPGA	-Field Programmable Gate Array
IC	-Integrated Circuit
VLSI	-Very Large-Scale Integration
ATE	-Automated Test Equipment
DUT	-Device Under Test
RF	-Radio Frequency
DIB	-Device Interface Board
GUI	-Graphical User Interface
USB	-Universal Serial Bus
UART	-Universal Asynchronous Receiver Transmitter
SPI	-Serial Peripheral Interface
FYP	-Final Year Project
DBMS	-Database Management System
CDC	-Communication Device Class
MOSFET	-Metal Oxide Semiconductor Field Effect Transistor
PLL	-Phase-Locked Loop
I2C	-Inter-Integrated Circuit
GPIO	-General Purpose Input Output
ADC	-Analog to Digital Converter
DAC	-Digital to Analog Converter
MCU	-Microcontroller Unit
SDK	-Software Development Kit
JTAG	-Joint Test Action Group
API	-Application Programming Interface

Chapter 1

INTRODUCTION

1.1 Introduction of IC Testing

Testing is a step followed in Integrated Circuit (IC) fabrication process to ensure the selected device has no manufacturing defects. In earlier times, IC designers only focused on the *speed*, *area*, and *power* in optimizing the design. In contrast to that today, *testability* has become the next factor that decides the quality of a design. According to the Very Large-Scale Integration (VLSI) Realization Process, the testing is placed as the process before delivering the chips to the customers. [1]

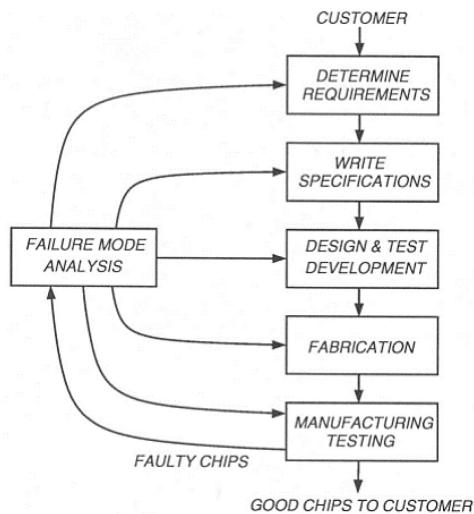


Figure 1.1 VLSI Realization Process

Generally, ICs are manufactured in large quantities on a single wafer by exposing them to the processes such as photolithography. Before this wafer is cut into pieces, in the die preparation process, to obtain individual circuits, all the individual circuits are tested for their functional defects, which can occur by activities such as misalignment of films, faults with the etching process, faults in materials, and impurities. This process is known as *Wafer Testing*. Then, to prevent physical damage and corrosion, the dice are placed inside a supporting case. This process is named *IC packaging*. Due to the fact, there are mechanical and chemical processes involved in packaging, even after the wafer test is completed successfully, faults in IC can occur. For example, the bonding wires can be damaged or

shorted in encapsulation, die can be misaligned, and mutual inductance and capacitance can appear. Therefore, it is essential to perform tests again before delivering good chips to the customers.

ATE machines conduct both wafer testing and final testing after packaging machines. They can perform both *Parametric Tests* (such as output drive current test, leakage test, etc.) and *Functional Tests* (check the proper functionality of chip nodes). High-end testers consist of three components which are *test head*, *workstation*, and *mainframe*. The workstation can be identified as the user interface to the tester. A user can debug an IC through the software packages included in the workstation. The mainframe serves as the unit, including measuring instruments, power supplies, digital driver unit, etc. The test head contains more sensitive equipment which needs less distance to the Device Under Test (DUT). According to a popular vendor's website [2], Some of the ATE machines manufactured by commercial vendors are as follows.



Figure 1.3 Teradyne UltraFLEXplus



Figure 1.2 Teradyne J750Ex-HD Family

- 2.2Gbps digital performance
- 512 digital channels per instrument
- 256 Power supply channels

Price – Approximately \$2 Million

- 400 Mbps digital performance
- 2048 multifunction pins
- Parallel IC testing capability

Price – starting from \$99,000

1.2 Problem Statement

IC manufacturers perform tests within their manufacturing plant or outsource the chips to other companies who carry out the procedure. Since the chips are tested by high-end testers, similar to the ATE machines mentioned above, it costs a considerable amount of money for the procedure. A company that facilitates the IC testing process can be considered a successful business in the silicon industry [3].

Currently, in Sri Lanka, ATE machines are not available to perform tests for ICs. It would be an immense opportunity for the electronic industry in the country as well as a door opening for the job market if an IC tester can be manufactured in Sri Lanka.

1.3 Literature Review

Automated Test Equipment (ATE) is widely used in the semiconductor industry for manufacturing testing of ICs. Some popular commercial vendors of ATEs are Teradyne, LTXCredence, Advantest, etc.

A high-performance tester with a fully upgraded configuration may cost around two million dollars on average. Targeting only a specific class of devices with designs for testability, a test system with a reduced configuration can be bought for a price as low as a hundred thousand dollars. Probers and handlers which handle the automation of picking, placing, and probing may cost about half a million dollars additionally. According to a book regarding fundamentals of mixed-signal IC testing [4], major Components of High-end ATE testers found in the industry can be stated as follows.

- **Workstation** – workstation is the computer providing a user interface to the tester. Test programs are written, executed, and debugged from the workstation with the tools provided by ATE vendor.
- **Mainframe** – consists of all the major internal hardware of the tester such as measuring instruments, power supplies, current sources, loads, switching and control circuitry, etc. It usually has separate subsystems for dc power, digital testing, analog testing, etc.
- **Test head** - contains highly sensitive test equipment that requires close proximity to the device been tested.

When considering the tester hardware architecture, an ATE comprises of following hardware units.

- General-purpose voltage/current sources
- Voltage, current measuring instruments
- Switching matrices
- Digital pin cards
- Arbitrary waveform generator and waveform digitizer
- Time measurement system
- RF subsystem

Generally, DUT interfacing is done by a Device Interface Board (DIB) which provides a socketed electrical connection between the test instruments of the ATE and the pins or pads of the DUT.

The diagram shown below represents a general flow chart of testing an IC, which is the commonly followed process in the industry. It starts with continuity testing, which measures the voltage across the DUT pins' protection diodes by forcing a small current to make sure that the DUT is well connected to the tester. Then one after another, different functional tests, DC tests, AC tests, digital tests are performed to the IC being tested. In each stage, if a test is failed the IC is rejected. Both good and bad ICs are sorted into bins.

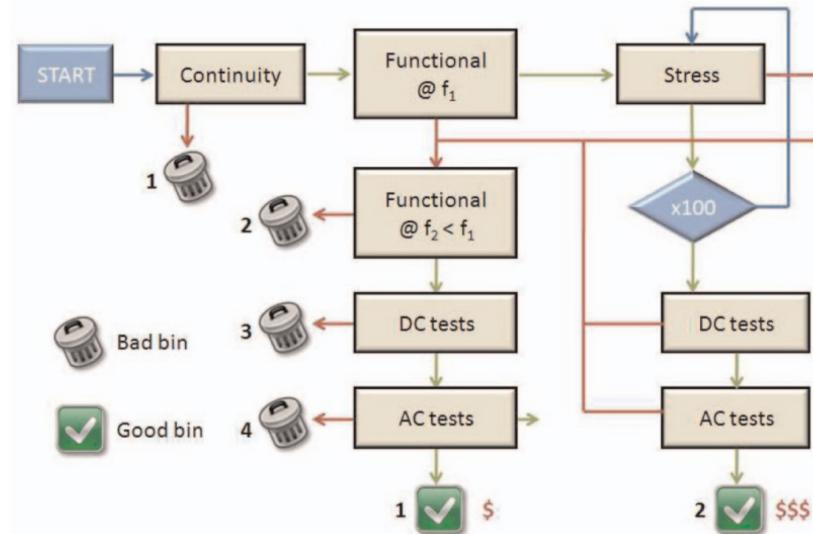


Figure 1.4 Example of Test Flow

1.4 Proposed Solution

We proposed a low-cost, scaled-down hardware-software solution for digital IC testing known by the name Automated Test Equipment (ATE) or IC Tester. Its design is **exclusive of automatic probers and handlers** and has the functionality of **testing packaged digital ICs**. A user can program the IC tester with the user interface provided.

It was also expected to demonstrate the functionality of the IC tester with basic tests for selected packages of digital ICs. As per the learnings from the digital IC design module [3], tests such as continuity test, Iddq test, and scan test were planned to be performed for multiple IC packages i.e., DIP14, DIP16, DIP28.

Moreover, our proposed solution can be stated as an attempt in taking the first step to developing an IC Tester in Sri Lanka. IC testers are not available in the current electronic industry in Sri Lanka. Manufacturing such a tester can be a good business opportunity for sub-contracting IC test processes inside the country. The tester developed in this project has compromised the functionality of an industrial-scale tester. However, it can be brought out as an industrial scale IC tester with improvements in the future.

1.5 Scope and Expected Deliverables

There are mainly 5 areas where the scope of this project can be categorized.

1. Standalone cross-platform computer software with GUI

This software provides the interface between the tester hardware and the user. It is based on QT C++ framework, embedded SQLite Database Management System and a USB interface with the tester hardware.

2. Embedded firmware development

The STM32 MCUs handle data transfer and signal control between the computer software package, digital driver unit, and pin cards. Protocols such as UART, USB, and SPI are expected to be included in the firmware.

3. Digital design and logic driving unit.

This unit will be implemented as an FPGA design with Verilog. Up to 100Mbps data rate will be maintained in 48 I/O ports. The maximum parallel capability will be 48 inputs/outputs at a time.

4. Hardware Designing and Prototyping

Multiple programmable power supply units will be included with various voltage ranges, current limits, and resolution. Ex: 0-5V power supply with 1.5A current limit and 10mV resolution.

A programmable current source is expected to be designed for the tester. A voltmeter with a millivolt (mV) range and a current measuring unit capable of measuring up to nano ampere (nA) range are included. Although the complete design will contain 16 pin cards, 2 pin cards will be added for the prototype, including the programmable switching and routing circuitry and power and control circuitry.

5. Implementing basic tests on suitable ICs.

General tests such as continuity testing, Iddq testing, scan testing, boundary scan testing, functional testing, and bypass testing are expected to be implemented in the final assembly of the IC tester. DIP14, DIP16, DIP28/DIP40, SOC16, QFP/ TQFP/ LQFP48 are the IC packages planned to be tested for demonstration.

1.6 Method of Investigation

The basic idea of our project is not to develop a completely novel solution but to develop a product to reach the industry-level standards in terms of quality and features at a lower cost. Our FYP group researched industry-level IC testers referred to related research papers books and, brainstormed all the information gathered. With the help of acquired knowledge, we developed a top-level hierarchy for the project.

This project can be subdivided into three key areas of investigation as follows. The solution space of each area was thoroughly explored by considering multiple options, assessing, and benchmarking them.

Investigations were carried out under the following three key areas.

- Hardware development
 - Literature review on the hardware architecture to find out the best prices in the industry.
 - Designing and simulating several different power supply circuits.
 - Referring to popular multimeter designs on the internet such as the designs in EEVBlog by Dave Johns.
 - Comparing and selecting electronic components while reading their datasheets thoroughly.
- Software development
 - Background research on the available software frameworks suitable for hardware interfacing.
 - Determining an appropriate Database Management System (DBMS).
 - Designing a user-friendly graphical user interface.
 - Brainstorming and deciding on features in the GUI for test configurations.
- Communication interfaces
 - Comparing the possible options for communication and improving the communication bit rate between the hardware and software GUI.
 - Testing dual-way USB serial communication using sample circuit setups.

1.7 Principal Results of Investigation

After an extensive analysis of each option in each key area, the project's overall design was finalized. The principal results of the investigations are shown as follows.

- Three power supply designs were finalized, one using the OPA548 power Op-Amp and the other two being switching converters. Reference designs for the power supplies were generated from Texas Instruments' WEBENCH power designer.
- The ammeter four measuring ranges were finalized by referring to the ‘μCurrent’ device by Dave Johns. The design for the programmable load was finalized modifying the design of the well-known circuit ‘Howland current pump’.

- There are small relays with fast switching times that can handle up to 5A, available in the market. These relays were decided to be used for switching purposes in the ATE. But since the on-resistance of those relays are around 20 Ohms, and since it is favourable to provide a ground connection to the DUT with a much lower resistance, we were able to choose a high-power Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) with a very low on-resistance around 1 Ohm for switching the ground connections in the IC tester.
- Universal Serial Bus (USB) Communication Device Class (CDC) libraries provided by the STM32 community were found to be easily applicable and suitable for communication with the computer with a high data rate.
- Most of the electronic components such as microcontrollers, digital-to-analog converters, analog-to-digital converters, clock generators, clock buffers, analog multiplexers, shift registers, transistors, MOSFETs, etc., were finalized after thorough reading through lots of datasheets.
- Being more hardware-related and more of on-site testing, a standalone desktop application was decided to be more suited than a web or mobile application. After evaluating the frameworks such as JavaFX, Qt, and .Net which are suitable for developing standalone applications, Qt was selected as the framework and C++ as the language with the reasons being cross-platform, C++ being more supportive for hardware, high community support, better GUI designer, C++ being faster than other languages and Good documentation.
- SQLite was selected as the DBMS after comparing the appropriate database libraries such as MongoDB, PostgreSQL, MySQL, etc., for the reason that its lightweight in setup, administration, and required resources, embedded and server-less database, best suited for standalone apps and especially Qt widget applications as stated in the book written on SQLite [5].

Chapter 2

METHOD

2.1 System Block Diagram

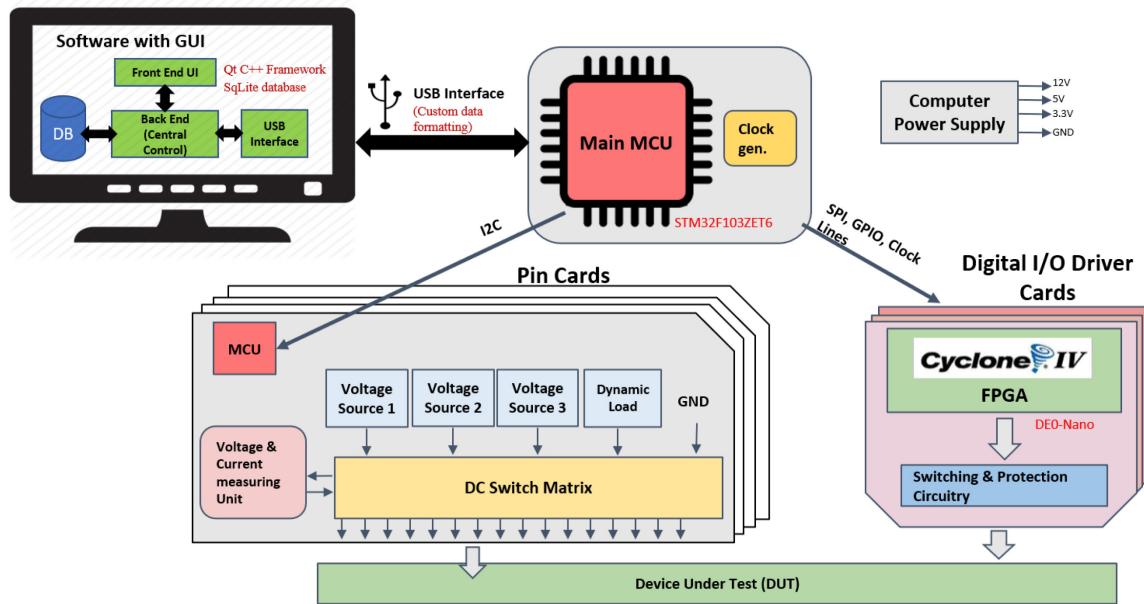


Figure 2.1 System block diagram

The block diagram of the project architecture is shown above and according to that, there are four major segments of the IC tester. Those are the software with a GUI, the main control board with the clock generating Phase Locked Loop (PLL), pin cards for electrical testing, and the digital I/O driver cards for digital testing. Each of these sub-areas is discussed in detail in the later sections of this chapter.

2.2 Main Microcontroller Unit

This unit acts as the communication handling device between the IC tester software, Pin Cards, and Digital IO Driver units. The heart of this unit is a STM32F103ZET6 Microcontroller. A large number of GPIO pins and support for different communication protocols such as I2C, SPI, and USB CDC make it convenient to connect with the outer world. The functionalities of the Main Microcontroller can be listed as follows.

1. Receiving commands for Pin Cards and Digital IO Drivers and sending back the results to the Software.
2. Generating clock signals for Digital IO Drivers
3. Configuring inputs and outputs of digital IO drivers and the logic levels.

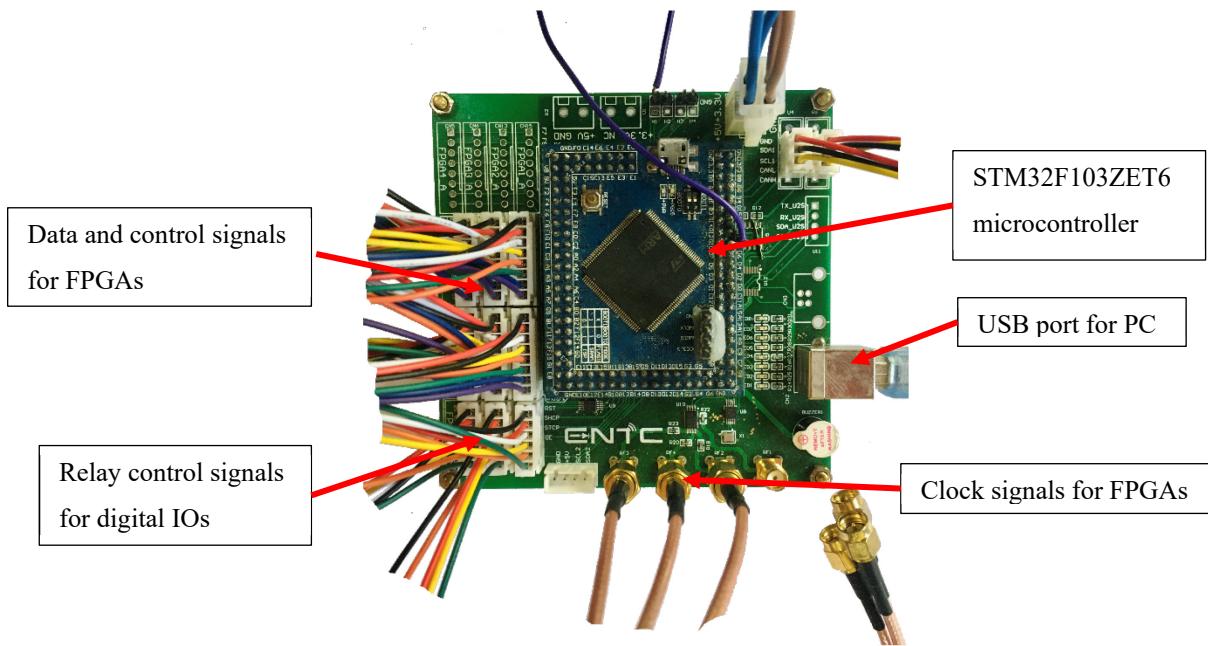


Figure 2.2: Main Microcontroller PCB

IC tester software is connected to the USB port of the computer where it is installed. The other end of the USB bus lies in the Main Microcontroller USB port. They communicate with each other using USB CDC. The data packets such as configuring power supplies, sending the switch matrix configuration composed by the software are decoded from the main microcontroller and sent to the relevant devices. The results from the devices, such as voltage and current measurements and digital outputs of DUT, are sent from the microcontroller to software with the support of USB CDC.

Digital IO Driver unit is a combination of DE0 nano FPGAs. The input clocks for those FPGA devices are generated with the help of the main microcontroller. I2C programmable Si5351A digital IC can be configured with the main microcontroller to generate clocks with variable frequency. The generated clock output is connected to CDCLVC110 clock buffer, which buffers the input to 4 outputs with minimum clock skew.

The 16 digital pins of each FPGA are connected to the logic level shifters. Their logic level voltages are programmed by the main microcontroller. Apart from that, the connectivity of DUT and FPGA is controlled with a relay matrix programmed by the main microcontroller. It also configures the digital IOs of FPGA as inputs or outputs.

2.3 Pin Card Electronics for Electrical Testing

Pin Card is a logical terminology for a set of resources that facilitates functionality for electrical testing for DUT. This includes mainly 3 PCBs.

1. PCB with Pin Card Microcontroller and Power Supply Units
2. PCB with Pin Card Measuring Instruments
3. PCB with Pin Card Switch Matrix

They work together, execute the commands from the Software and send back the electrical testing results.

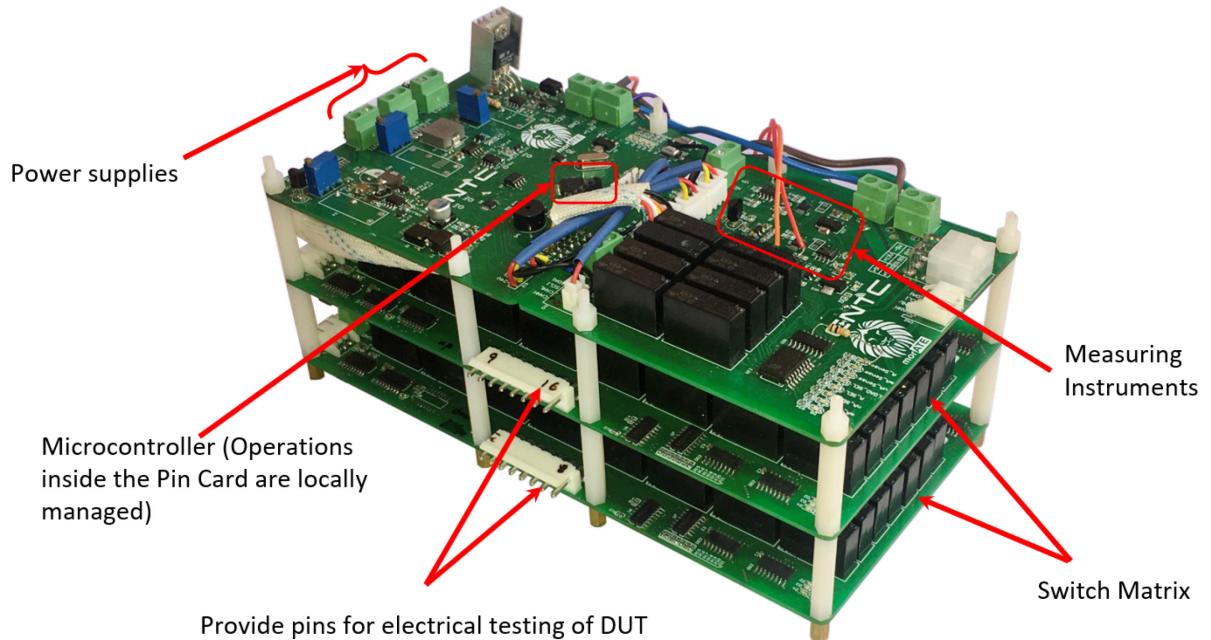


Figure 2.3 A photo of an assembled pin card

2.3.1 PCB with Pin Card Microcontroller and Power Supply Units

The microcontroller which handles the local operations inside a pin card is located in this PCB. It is an STM32F103c8t6 microcontroller. The functions of the microcontroller can be elaborated as follows.

- Configuring the DACs for setting voltages and current limits in power supplies.
- Sending the byte sequence to the shift registers to control the relay matrix.
- Configuring ADCs to measure currents and voltages from DUT.
- Configuring DAC to set the value for Dynamic Load.
- Communicating with the main microcontroller

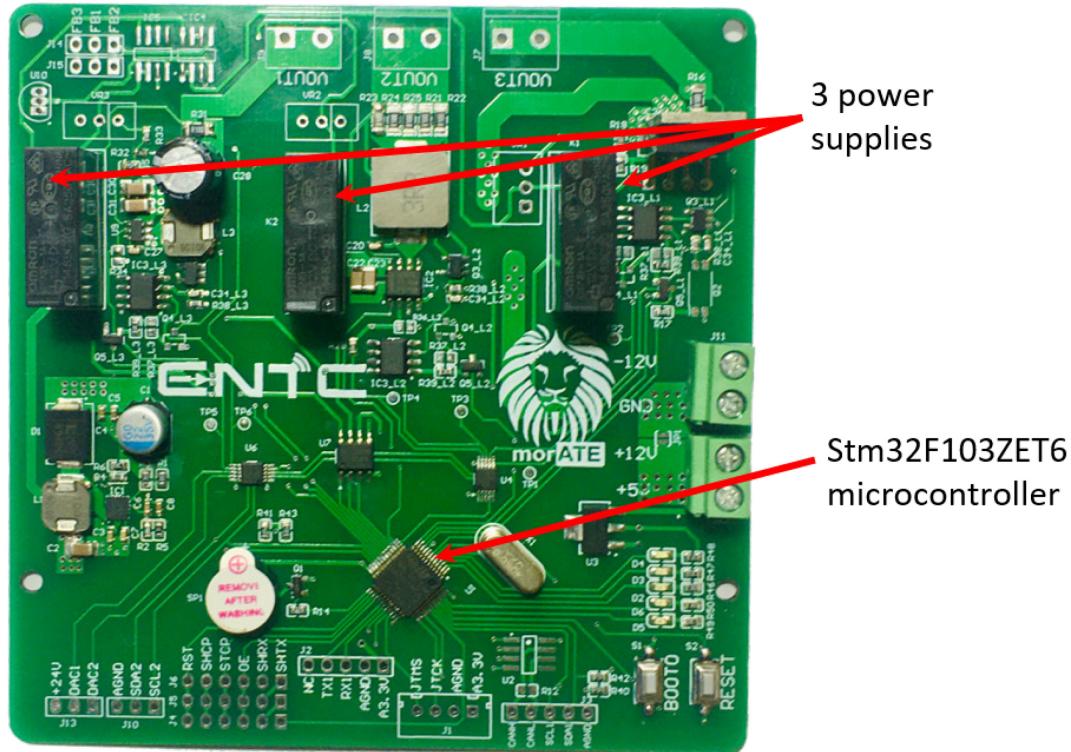


Figure 2.4 PCB with pin card microcontroller and power supply units

There are 3 power supplies in this segment. The first power supply is designed with an operational amplifier, which can work in the range between 0-5V and source up to 1A current. The second power supply is a buck converter which works in the 0.8V-5V range

and can source up to 5A current. The last power supply can source high voltages such as 5-15V and output 1A current.

The voltages of these power supplies are controlled by 12-bit I2C programmable DACs. The configuration registers of the DAC are set by the microcontroller. Apart from that, the output currents of the power supplies are monitored by current measuring ICs. The measured values are compared with the values set by the user, and an interrupt is generated for the microcontroller to take further measures (inform the software that current limits are triggered and switch off the respective power supply).

2.3.2 PCB with Pin Card Measuring Instruments

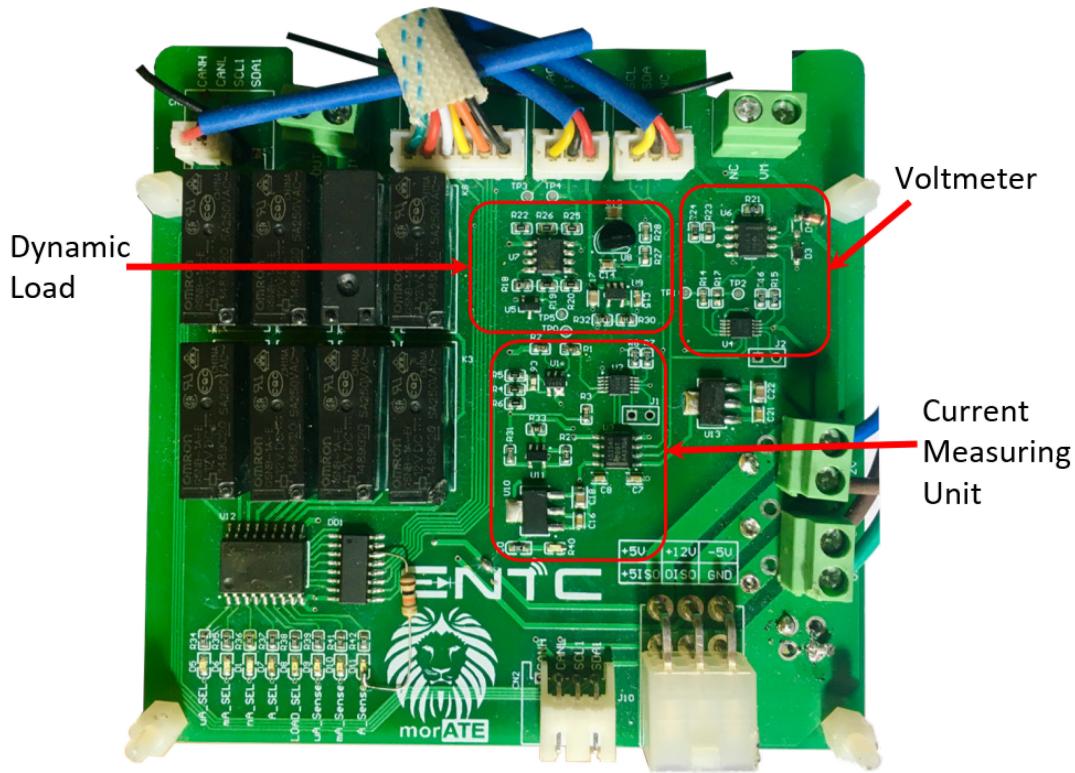


Figure 2.5 PCB with pin card measuring instruments

This PCB consists of a voltmeter, ammeter, and a programmable current source/sink. The voltmeter is designed to measure voltages from 0 to 20V and the input of the voltmeter is buffered by a precision Op-Amp voltage follower. The buffered voltage is then divided by 5 by a precision resistor network. The divided voltage is sampled by a 16-bit Analog to digital convertor to obtain the voltage measuring results.

The ammeter is designed to measure the bi-directional current flow through any pin of the pin card. The ammeter has four ranges, and they are selected by a set of relays. The current is measured by reading the voltage drop across a current sensing resistor and the voltage drop across the resistor (burden voltage) is kept below 10mV to reduce the error. The small voltage drop is then amplified by a precision Op-Amp amplifier with a gain of 100. The amplified voltage is sampled with a 16-bit ADC to get the final current measurement. The Ammeter is designed to measure the current in the high side of the system to remove the effect on the ground potential which occurs with low side current sensing. Since the voltage on an output pin can go as high as 15V, the ammeter is powered by a separate isolated power supply that does not share a common ground connection with the rest of the system.

The programmable load is used to perform the push-pull test on the DUT. The programmable load is a modified version of the well-known “Howland current pump” and it can source or sink currents up to 2.5mA. The sink/source current is programmable via an external voltage which is generated by a DAC. The circuit consists of matching resistors with 0.1% accuracy which maps 1mV of the external voltage to 1uA of current.

2.3.3 PCB with Pin Card Switch Matrix

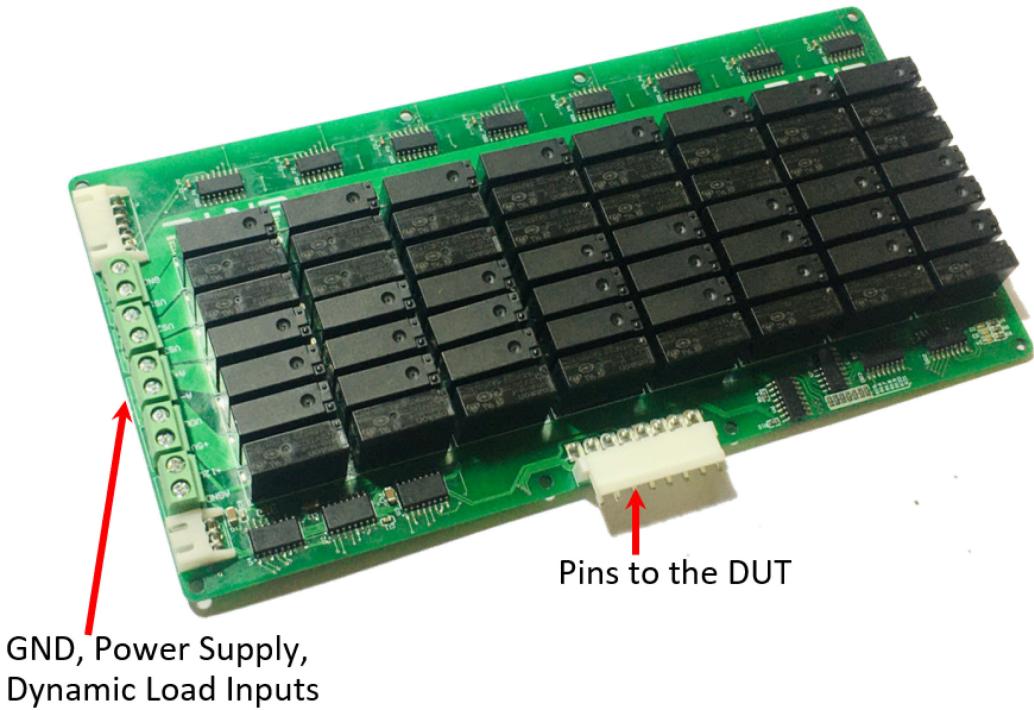


Figure 2.6 Switch matrix PCB

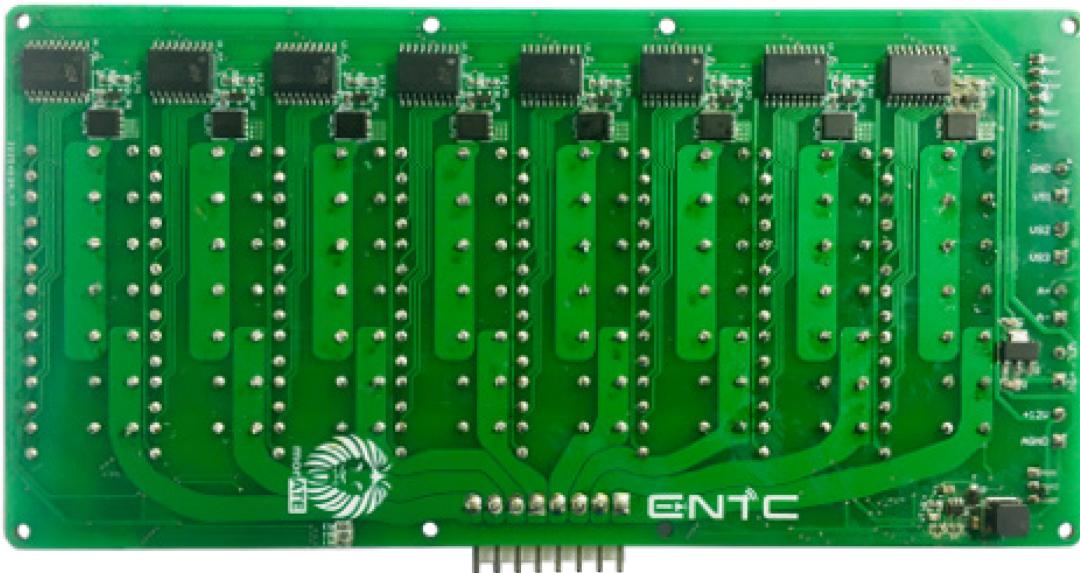


Figure 2.7 Switch matrix PCB backside

Routing all the resources to the physical interface of DUT pins is handled with the switch matrix. The matrix is constructed with single pole DC relays with low contact resistance and high current carrying capability such as 3A and 5A and high-speed MOSFETs. Relays

and MOSFETs are controlled by the relay driver ICs and shift registers. The bit pattern to shift registers is passed by the microcontroller. The power lines and measuring instruments are connected to the DUT pins with relays, while the ground connection is constructed with MOSFETs.

There are two switch matrix PCBs in one pin card. Each contains 10x8 relay and MOSFET matrices. These relays route three power supplies, voltmeter, ammeter, dynamic load, and ground plane to 16 physical pins of DUT.

2.4 Digital I/O Drivers

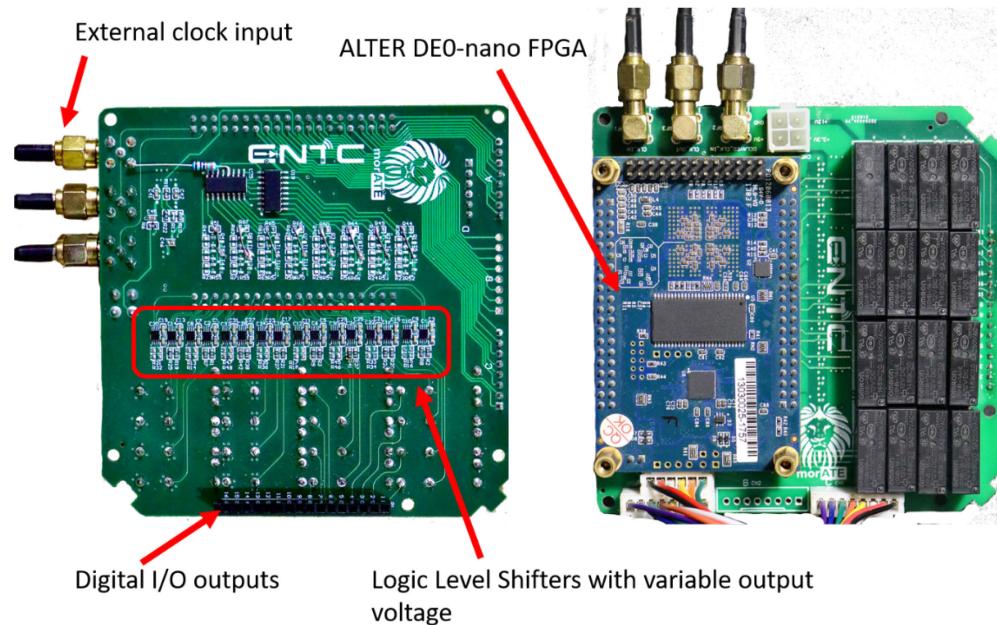


Figure 2.8 Digital I/O driver PCB

The main component of this section is Altera DE0 nano educational development board. The PCB is designed in such a way that the FPGA board can be directly plugged into it. Input clocks to the FPGA are provided externally by the main microcontroller. The board is designed as a 4-layer PCB with impedance-controlled tracks for digital inputs and outputs between FPGA and DUT pins.

The immediate inputs and outputs of FPGA are connected to logic level shifters. They serve the conversion between the logic level of DUT and FPGA (3.3V logic). The other

ends of logic level shifters are connected to relays which can isolate the connection between FPGA and DUT pins.

The logic voltage of the level shifters can be changed to a desired level between 0.8V – 5V with a variable power supply controlled by the main microcontroller.

2.5 IC Tester Software Development

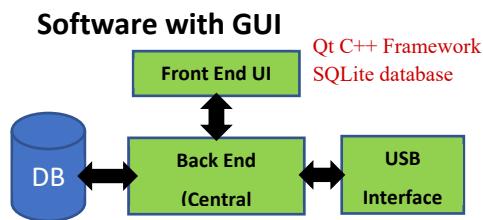


Figure 2.9 Block diagram of the IC Tester software

IC tester software architecture can be segmented into 4 subcomponents as shown in the above figure namely, backend of the software, frontend graphical user interface, DBMS, and the USB interface.

IC Tester Software is developed as a stand-alone desktop application using Qt framework with backend in C++ language. Moreover, this software is the top level of the control hierarchy of the IC tester which entirely handles the high-level controlling of the whole system.

The front-end UI is made as a Qt widget application. The test engineer can easily work with the machine to develop test programs via the GUI. The test programs configured in the GUI are stored in an SQLite DB in a raw format. In the backend, the input data from the user interface which are recorded in the database are converted to custom-made packets of data and instructions which are then passed through the interface of the main MCU. Packets sent from the software are decoded by the main MCU and these instructions are used to operate the subsystems accordingly. Once the test execution starts, the raw test results are sent back to the computer in real-time through USB serial communication and those will be decoded, and test reports are generated in the software and saved to text files.

Chapter 3

RESULTS

3.1 Software Development Results

The frontend and the backend design and development of the standalone computer software of the ATE machine are fully completed. The remaining parts of the software are simple fine tunings and calibrations that have to be done according to testing of the hardware. The main functionalities of the IC tester software that have been tested and verified to work without any bugs are as follows.

- Creating test programs
- Configuring test programs and saving them in a database.
- Executing test programs by sending data packets and instructions to the main microcontroller unit.
- Receiving and analyzing test results
- Generating test reports

Following screen captures from the IC tester software GUI highlights the main parts of the software starting from creating a test project, up until the execution of tests and report generation.

3.1.1 Home Window

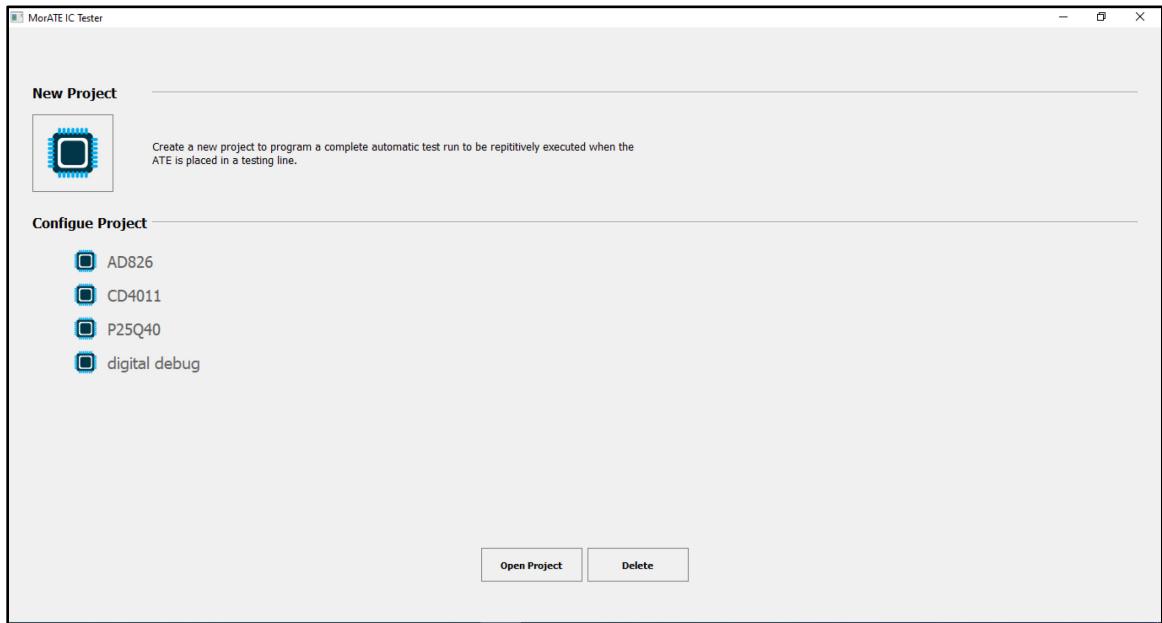


Figure 3.1 Home Window of the GUI

This is the home window of the software GUI where the user can create a new test project or open an existing project.

3.1.2 Electrical testing and configuration canvas

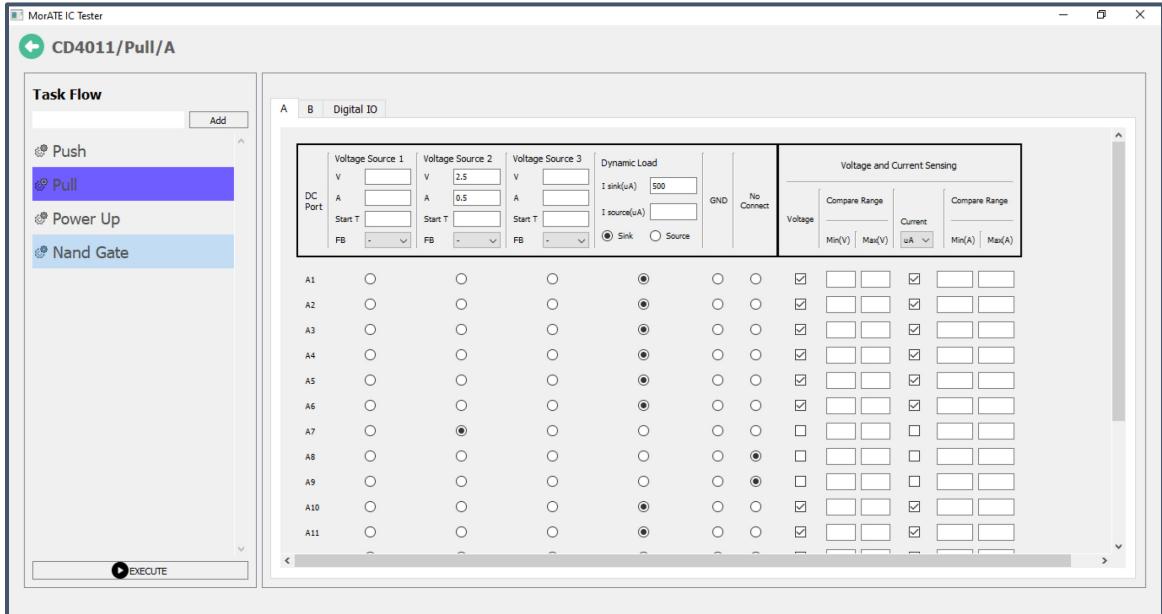


Figure 3.2 Electrical testing and configuration canvas

The above figure shows the canvas used to configure power connections and electrical testing of the DUT. There on the left panel user can add a new task to the task flow and program the task using the canvas provided on the right side.

3.1.3 Digital testing and configuration canvas

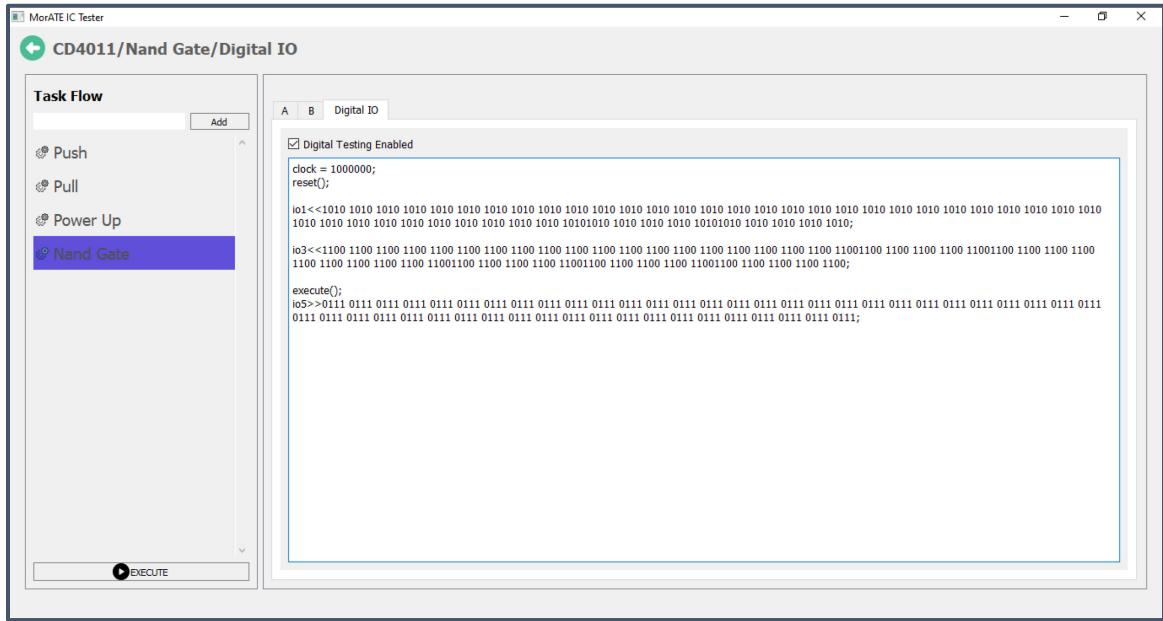


Figure 3.3 Digital testing and configuration canvas

On the right-side canvas that is used to program a task in the task flow, several tabs are used to switch between different tester hardware segments of the IC tester. Using the digital IO tab, the user can get into the digital testing canvas which is shown above. It is in the form of a text editor where the user can write a code for a custom digital test.

3.1.4 Test Execution Window

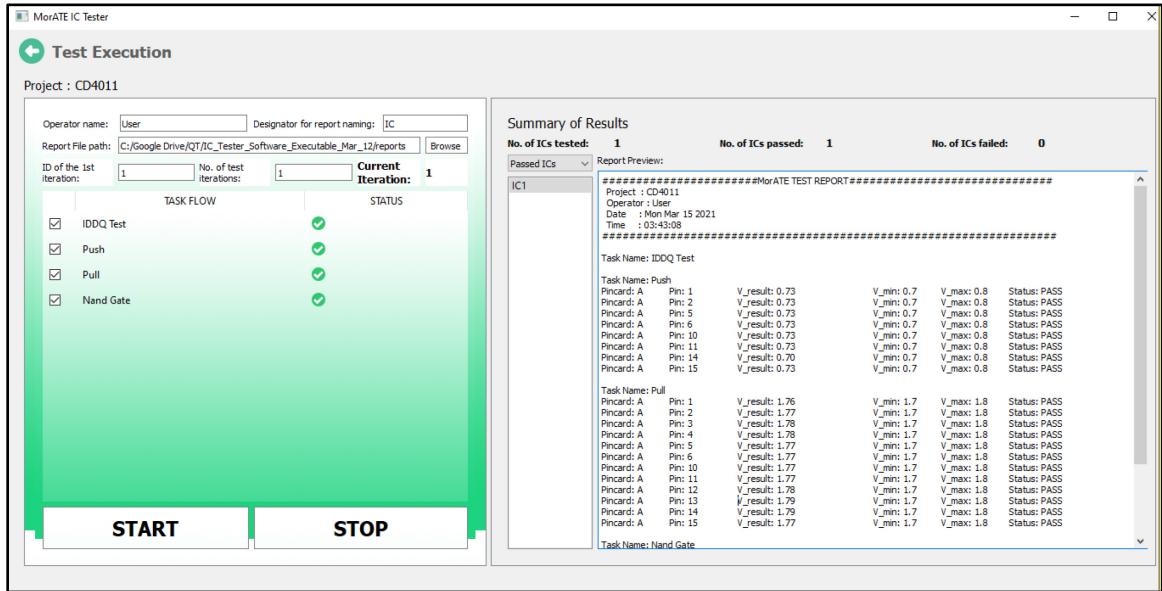


Figure 3.4 Test execution window

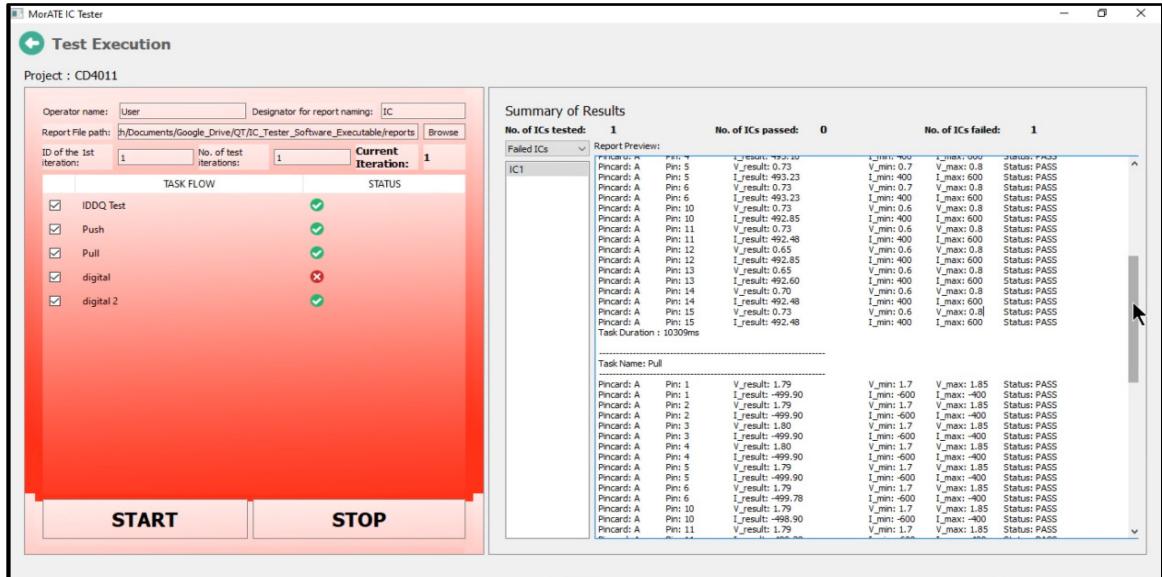


Figure 3.5 Test execution window with an indication of a failure

The above figures are some screen captures of the test execution window of the software which facilitates the environment needed to set up and run a sequence of testing a batch of ICs in an industrial testing line. Green and red colours are used to highlight the test status of the execution as PASS or FAIL, from the computer screen to the user very clearly. The execution window also features a real-time console where the user can see what is happening in real-time.

Below are few example reports generated from test executions in the IC tester. In testing a batch of ICs, such reports are generated for each IC tested. A report consists of all the measurements directed to be done in the test program made by the user and the digital output data vector comparisons.

3.1.5 Test Report – CD4011 NAND Gate IC

MorATE TEST REPORT

Project : CD4011

Operator : User

Date : Mon Jul 26 2021

Time : 02:01:18

Task Name: IDDQ Test

Pincard: A Pin: 9 V_result: 3.74 V_min: 3.65 V_max: 3.85 Status: PASS
Pincard: A Pin: 9 I_result: 7.25 I_min: 1 I_max: 100 Status: PASS
Task Duration : 1661ms

Task Name: Push

Pincard: A	Pin: 1	V_result: 0.73	V_min: 0.6	V_max: 0.8	Status: PASS
Pincard: A	Pin: 1	I_result: 493.35	I_min: 400	I_max: 600	Status: PASS
Pincard: A	Pin: 2	V_result: 0.73	V_min: 0.6	V_max: 0.8	Status: PASS
Pincard: A	Pin: 2	I_result: 493.35	I_min: 400	I_max: 600	Status: PASS
Pincard: A	Pin: 3	V_result: 0.65	V_min: 0.6	V_max: 0.8	Status: PASS
Pincard: A	Pin: 3	I_result: 493.35	I_min: 400	I_max: 600	Status: PASS
Pincard: A	Pin: 4	V_result: 0.65	V_min: 0.6	V_max: 0.8	Status: PASS
Pincard: A	Pin: 4	I_result: 493.48	I_min: 400	I_max: 600	Status: PASS
Pincard: A	Pin: 5	V_result: 0.73	V_min: 0.7	V_max: 0.8	Status: PASS
Pincard: A	Pin: 5	I_result: 493.48	I_min: 400	I_max: 600	Status: PASS
Pincard: A	Pin: 6	V_result: 0.73	V_min: 0.7	V_max: 0.8	Status: PASS
Pincard: A	Pin: 6	I_result: 493.23	I_min: 400	I_max: 600	Status: PASS
Pincard: A	Pin: 10	V_result: 0.73	V_min: 0.6	V_max: 0.8	Status: PASS
Pincard: A	Pin: 10	I_result: 493.10	I_min: 400	I_max: 600	Status: PASS
Pincard: A	Pin: 11	V_result: 0.73	V_min: 0.6	V_max: 0.8	Status: PASS
Pincard: A	Pin: 11	I_result: 492.73	I_min: 400	I_max: 600	Status: PASS
Pincard: A	Pin: 12	V_result: 0.65	V_min: 0.6	V_max: 0.8	Status: PASS
Pincard: A	Pin: 12	I_result: 493.10	I_min: 400	I_max: 600	Status: PASS
Pincard: A	Pin: 13	V_result: 0.65	V_min: 0.6	V_max: 0.8	Status: PASS
Pincard: A	Pin: 13	I_result: 492.73	I_min: 400	I_max: 600	Status: PASS
Pincard: A	Pin: 14	V_result: 0.70	V_min: 0.6	V_max: 0.8	Status: PASS
Pincard: A	Pin: 14	I_result: 492.85	I_min: 400	I_max: 600	Status: PASS
Pincard: A	Pin: 15	V_result: 0.73	V_min: 0.6	V_max: 0.8	Status: PASS
Pincard: A	Pin: 15	I_result: 492.85	I_min: 400	I_max: 600	Status: PASS

Task Duration : 10201ms

Task Name: Pull

Pincard: A	Pin: 1	V_result: 1.79	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 1	I_result: -499.78	I_min: -600	I_max: -400	Status: PASS
Pincard: A	Pin: 2	V_result: 1.79	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 2	I_result: -499.78	I_min: -600	I_max: -400	Status: PASS

Pincard: A	Pin: 3	V_result: 1.80	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 3	I_result: -499.65	I_min: -600	I_max: -400	Status: PASS
Pincard: A	Pin: 4	V_result: 1.80	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 4	I_result: -499.78	I_min: -600	I_max: -400	Status: PASS
Pincard: A	Pin: 5	V_result: 1.79	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 5	I_result: -499.78	I_min: -600	I_max: -400	Status: PASS
Pincard: A	Pin: 6	V_result: 1.79	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 6	I_result: -499.78	I_min: -600	I_max: -400	Status: PASS
Pincard: A	Pin: 10	V_result: 1.79	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 10	I_result: -498.78	I_min: -600	I_max: -400	Status: PASS
Pincard: A	Pin: 11	V_result: 1.79	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 11	I_result: -499.03	I_min: -600	I_max: -400	Status: PASS
Pincard: A	Pin: 12	V_result: 1.80	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 12	I_result: -498.90	I_min: -600	I_max: -400	Status: PASS
Pincard: A	Pin: 13	V_result: 1.81	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 13	I_result: -499.53	I_min: -600	I_max: -400	Status: PASS
Pincard: A	Pin: 14	V_result: 1.82	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 14	I_result: -499.90	I_min: -600	I_max: -400	Status: PASS
Pincard: A	Pin: 15	V_result: 1.79	V_min: 1.7	V_max: 1.85	Status: PASS
Pincard: A	Pin: 15	I_result: -499.78	I_min: -600	I_max: -400	Status: PASS

Task Duration : 10198ms

Task Name: digital

io5

Expected: XXXX0110

Received: 01110110

Status: PASS

io7

Expected: 01110110

Received: 01110110

Status: PASS

Task Duration : 1085ms

Task Name: digital 2

io8

Expected: 01110110

Received: 01110110

Status: PASS

io10

Expected: 01110110

Received: 01110110

Status: PASS

Task Duration : 952ms

Overall result : PASS

Total Testing Time : 26553ms

3.1.6 Test Report – SD RAM

```
#####
#MorATE TEST REPORT#####
Project : SD RAM
Operator : User
Date   : Mon Jul 26 2021
Time   : 22:57:08
#####

-----
Task Name: IDDQ
-----
Pincard: A      Pin: 1      V_result: 3.29      V_min: 3 V_max: 3.5      Status: PASS
Task Duration : 1311ms

-----
Task Name: WRITE
-----
Task Duration : 37ms

-----
Task Name: READ
-----
io5
Expected: xxxxxxxx00111111xxxxxxxxx11111100xxxxxxxxx11110011xxxxxxxxx11001100xxx
Received: 00000000011111000000001111110000000000111100110000000011001100000
Status: PASS
io3
Expected: xxxxxxxx00000011xxxxxxxxx00000011xxxxxxxxx00001100xxxxxxxxx00000011xxx
Received: 00000000000001100000000000000110000000000000110000000000000011000
Status: PASS
io7
Expected: xxxxxxxx11000000xxxxxxxxx11111100xxxxxxxxx00111111xxxxxxxxx11110011xxx
Received: 000000110000000000011111000000000001111100000000111100110000000011110011000
Status: PASS
io9
Expected: xxxxxxxx00001100xxxxxxxxx11110000xxxxxxxxx00110011xxxxxxxxx11111100xxx
Received: 0000000000011000000000011110000000000011001100000000111110000000011110011000
Status: PASS
io10
Expected: xxxxxxxx00000000xxxxxxxxx00000011xxxxxxxxx00001111xxxxxxxxx00001100xxx
Received: 000000000000000000000000000000001100000000000001111000000000001100000
Status: PASS
io8
Expected: xxxxxxxx11000011xxxxxxxxx00001100xxxxxxxxx00001111xxxxxxxxx11001100xxx
Received: 000000011000011000000000000110000000000000111100000000011001100000
Status: PASS
io6
Expected: xxxxxxxx00000011xxxxxxxxx00001100xxxxxxxxx00001100xxxxxxxxx11001111xxx
Received: 0000000000011000000000011000000000000011000000000000011001111000
Status: PASS
Task Duration : 3689ms
#####
Overall result : PASS
#####
Total Testing Time : 7514ms
```

3.2 Tested Capabilities of Communication Protocols Used

Three communication protocols are used in the prototype design.

1. USB - Serial communication between the tester and the computer.
2. SPI - Communication between the main microcontroller and the IO drivers.
3. I2C - Communication between the main microcontroller and the Pin Cards.

All three communication protocols were tested for their maximum capability and the results are given below.

3.2.1 USB

USB Serial communication (USB CDC class) was used to communicate between the computer and the Main Microcontroller. The communication speed was highly dependent on the computer software and the USB driver library. However, for the IC tester software, the QSerial USB serial library which is the default Serial Library offered by the Qt SDK was used and the maximum data transfer rates are shown below.

Table 3.1 USB interface speed results

PC to Main Microcontroller	2.28 Mbits/s
Main Microcontroller to PC	4.57 Mbits/s

3.2.2 SPI

SPI communication protocol is used to load the test vectors to the IO driver cards and transfer the captured outputs back to the main microcontroller. SPI is a synchronous protocol where the main microcontroller acts as the master and provides the clock signal. The data transfer rate is directly proportional to the frequency of the clock signal and the maximum obtainable frequency depends on the signal integrity of the transmission path. The prototype design was tested up to 10 Mbits/s bidirectional communication without any issues.

3.2.3 I2C

I2C (or IIC) protocol is used to communicate between the pin cards and the main microcontroller. This is also a synchronous protocol where the main microcontroller acts

as the master and provides the clock signal. Unlike SPI, there are several standard data rates defined for the I2C. The IC tester prototype was tested for both standard (100 kbits/s) and fast mode (400 kbits/s) data transfer rates.

3.3 Tested Capabilities of the Pin Cards

The pin cards are used to perform the DC tests and power the IC while performing the Digital tests. A pin card is consisting of three programmable power supplies, one programmable load, one voltmeter, and one ammeter. Upon the completion of the assembly, each sub-module was tested for its capabilities and the results are shown below.

3.3.1 Power supplies

Table 3.2 Power supply capabilities tested

	Supply 1	Supply 2	Supply 3
Programmable voltage range	0 – 5V	0.8 – 5V	0.8 – 15V
Voltage accuracy	0.1V	0.1V	0.1V
Current capability	1A max	5A max	1A max

3.3.2 Programmable load

Table 3.3 Programmable load capabilities tested

Current source capability	Up to 2.5 mA in 100 μ A steps
Current sink capability	Up to 2.5 mA in 100 μ A steps
Output voltage range	-1.2V to +5.5V

3.3.3 Voltmeter

Table 3.4 Voltmeter capabilities tested

Measurable voltage range	0 – 20 V
Accuracy	0.01v

3.3.4 Ammeter

Table 3.5 Ammeter capabilities tested

	uA range	mA range	A range
Measurable range	Up to ± 1500 uA	Up to ± 1500 mA	Up to ± 5 A
Accuracy	$\pm 10\mu A$	± 0.1 mA	± 0.01 A

3.4 Tested Capabilities of Digital I/O Drivers

The Digital IO drivers used to perform the Digital tests over device under test. The testing frequency depends on the specifications provided by the manufacturer of the IC. After the assembly of the prototype, the IO driver card was tested with several basic logic ICs to check the performance and there were no issues. However, the basic logic gates operate only up to 1MHz. Therefore, to further test the operational frequency of the digital design inside the FPGA and the electrical circuitry, a simple short circuit was created between an input and output pin, and the IO driver card was tested for frequencies up to 100 MHz provided by external programmable PLL. The design did not arise any issues up to 100 MHz and proposed specifications were met.

During the testing process of the IO card, a hardware error that was made during the designing of the PCBs was identified. It prevented the pins of the IO card from being configured as either an input or an output by the software. Instead, the pins could be configured as a fixed input or output. This error prevented the IC tester from testing ICs with bi-directional data pins. Since this was an easily solvable error, the PCB was redesigned to fix the error. The redesigned PCB was thoroughly tested and the following results were obtained.

Table 3.6 Capabilities of Digital I/O drivers

Digital Channels	48 Channels (16 per Digital I/O driver)
Test Frequency	10kHz -100MHz
I/O Logic voltage	1.2V – 5V (variable 0.1V increments)
Test vector depth	2Kbytes per I/O driver

3.5 Overall Functionality of the Fully Assembled System

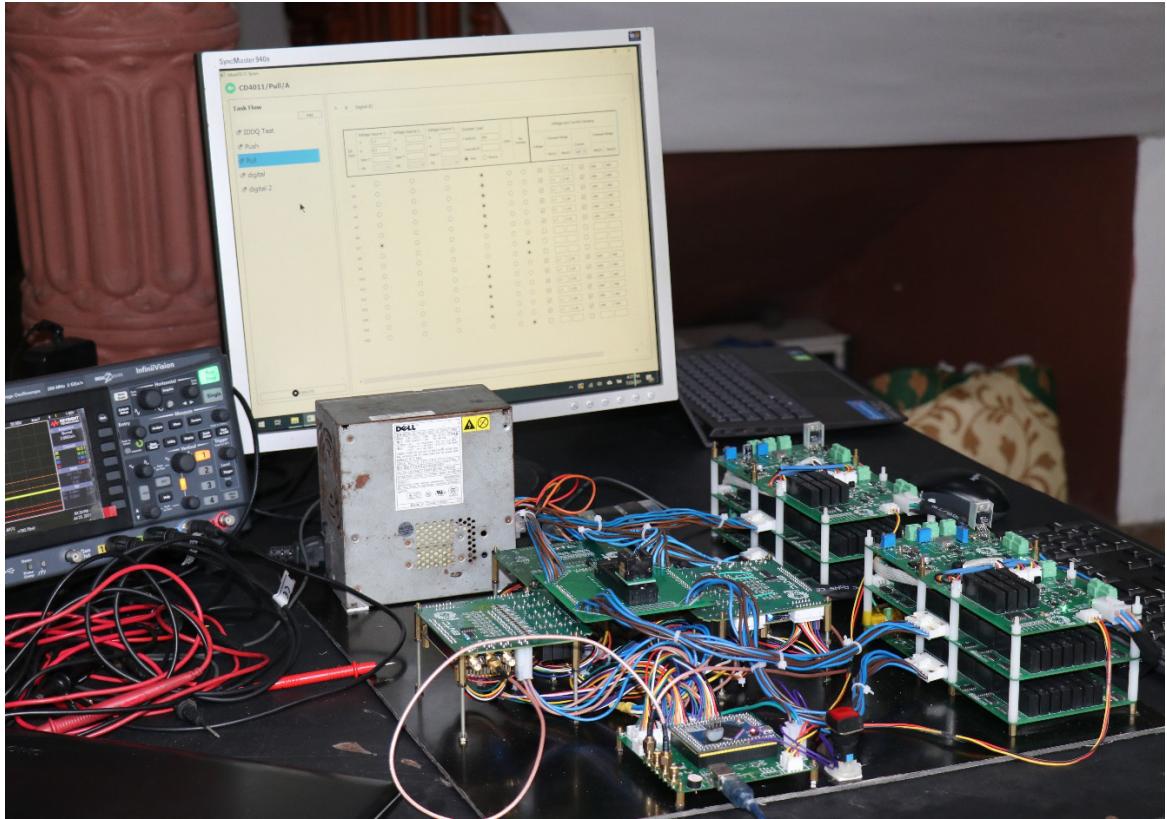


Figure 3.6 Fully assembled ATE

The above photo shows the assembled ATE prototype. The two pin cards, three digital I/O driver cards, main controller PCB, device interface board, and the computer power supply are clearly visible in this photo of the assembly. Using this assembled ATE, several digital ICs were tested. 7HC595D shift register IC, 25Q40 SPI flash IC, CD4011 quad AND gate IC and HYB 39S128800CT SD ram IC are some of those ICs which was tested successfully using the fully assembled system.

With the fully assembled system, both electrical and digital tests could be done to the same IC. Iddq test, continuity test, and digital functional tests were carried out on the ICs which were tested. In 3.1.5 there is a report generated by testing CD4011 IC using this fully assembled system.

3.6 Timing results

The ATE prototype mainly carryout three tests which are IDDQ test Push/Pull test and Digital vector test. After running multiple iterations of tests on several ICs and by averaging the measurements, the following timing results were obtained.

Table 3.7 Average timing results

Average time for an IDDQ test per pin	1600ms
Average time for a push/pull test	420ms per pin
Average time for a digital test	Highly depends on the test vector size test frequency.

Chapter 4

DISCUSSION AND CONCLUSIONS

4.1 Interpretation of the Overall Results

Each of the hardware components, communication interfaces, and the software GUI were explained in detail in chapter 2 of this report along with their results in chapter 3. Although those results obtained from evaluating the performance of the IC tester, cannot compete with the cutting edge ATE machines used in the industry, they highlighted that there is a good potential in further development of our IC tester in future stages to arrive at an industrial-grade ATE that can be commercialized.

Our IC Tester standalone software with a GUI can be considered as a simple controller of the tester hardware which is visually appealing and very user friendly. Although the software provides all necessary features to create, configure and execute test programs with test report generation, it is in a base level of IC testing where there is no specific protocol-wise test implementation such as ethernet, JTAG, etc. The software outputs do not adhere to the IEEE standards for industrial testing software either. According to a book on digital VLSI testing [6], modern ATE software comprises all digital protocol implementations, but none of these aspects conveys that the software is unacceptable because it precisely works for the basic testing principles and therefore it can be used as an Application Programming Interface (API) to develop software that can test with different protocols while adhering to IEEE standards of IC testing.

According to the results obtained by testing the capabilities of the prototyped hardware, the test equipment is suitable to test most of the general tests such as Iddq test, push-pull test, and digital logical test for many of the common ICs found in the market. Yet, in future stages, those values have to be further improved by using more expensive components and methods to arrive at an industrial-grade ATE machine. Also, the testing time has to be improved with faster relay switching and more parallelism in testing.

4.2 Value and Correspondence to Existing Industrial Methodologies

The current state-of-the-art in IC testing consists of very high-speed digital testing capabilities even up to 5Gbps, highly parallel testing capabilities along with automation in all possible areas. Teradyne, Advantest, LTX-Credence are some leading commercial vendors of Automatic Test Equipment (ATE). The price of an ATE tester from such a vendor is millions of dollars. The ultimate motive of this project is to start IC testing in Sri Lanka. This first step of developing a locally made ATE which can create new business opportunities within the country.

Although the tested capabilities of the software and hardware developed in this project are lagging behind the capabilities of ATE machines used in the industry right now, the results are highly favourable as a first stage of developing such an advanced, high-tech machine. Just like the methods applied in our project, we can observe the use of relays for switching and FPGAs for data parallelism in the existing industrial methodologies as well. By adding more resources for more parallelism and improving the quality of electrical measuring and power supply hardware, the project can be carried forward with the ultimate goal of creating a commercial product that can add significant value to the electronic industry in Sri Lanka.

4.3 Potential further Improvements

4.3.1 Replacing Switching Power Supplies with Linear Power Supplies

The pin card of the prototype ATE has 3 power supplies where two of them are switch-mode power supplies. During the test phase, it was observed that switching power supplies were not convenient for providing variable voltages. Further, they have higher noise at the output compared to linear regulators. Therefore, switching power supplies can be replaced by suitable linear regulators which have higher noise immunity and higher stability over a wide output range.

4.3.2 Using Reed Relays instead of Generic Switching Relays

In the prototype, generic relays are used in the switching matrix and, they have an average switching time of 20ms. By replacing them with Reed relays, which have switching times

less than 5ms, IC testing time can be significantly improved. Furthermore, they have a higher lifespan (switching cycles) and reliability.

4.3.3 Changing the Communication Scheme between Main Controller and Digital IO Drivers

In the current ATE prototype, a custom-designed parallel protocol is used to communicate between the main controller and digital IO drivers. The use of a parallel protocol provides a higher bandwidth at the expense of a large number of parallel wire connections. Replacing the parallel communication scheme with a serial communication protocol will significantly reduce the number of wire connections and the associated wiring cost and overhead.

4.3.4 Replacing the Main Controller with USB Hub or Ethernet Switch

The main controller is merely a command distributor between the software interface and ATE hardware. Replacing it with USB Hub or Ethernet Switch will reduce the communication delays associated with the main controller and reduces the required number of wire connections. With such configuration, the computer can directly communicate with pin cards and digital IO drivers which provides more flexibility to the computer software to parallelize tasks improving the overall test time.

4.4 Conclusion

The architecture and the overall functionality of our low-cost ATE have been described under each main component, i.e., hardware, communication interfaces, and software GUI.

The current state-of-the-art techniques in IC testing consist of very high-speed digital testing capabilities, even up to 60Gbps and high parallelism and automation in all possible areas. Hence, digital testing has become very expensive nowadays.

However the results of the prototyped design presented in this paper highlight how most of the mid-range digital ICs operating up to a frequency of 100MHz can be tested with an educational level FPGA development board like the DE0- nano board. Furthermore, the prototyped low-cost ATE is capable of performing electrical tests on digital ICs such as the IDDQ test to measure the quiescent power consumption of the IC and the push-pull test

to check the input protection diodes. Voltages between 0-20V can be measured with 10mV accuracy and currents can be measured down to the microampere range with $10\mu\text{A}$ accuracy.

The software that handles the digital testing functionality used in the proposed solution is still at a lower level. However, the current hardware specification is sufficient to develop the software further with additional features and integrate it with an existing Automatic Test Pattern Generator (ATPG) tool in a compatible manner.

Our ultimate conclusion on the continuation of the project is that it should be carried forward as an undergraduate project to the next year as well with developing more advanced software features, more accurate and robust power supply units, voltmeters, ammeters, and faster communication techniques.

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APPENDIX

The following link is for the Github repository containing all the design files and the source codes of the Automated Test Equipment (ATE) developed under this project.

<https://github.com/nalithlakshan/FYP-MorATE>

Below is the youtube link for the final demonstration video of this project.

https://youtu.be/_BMeR-ZwBSQ