ADVD ASSIGNMENT

MICROWIND

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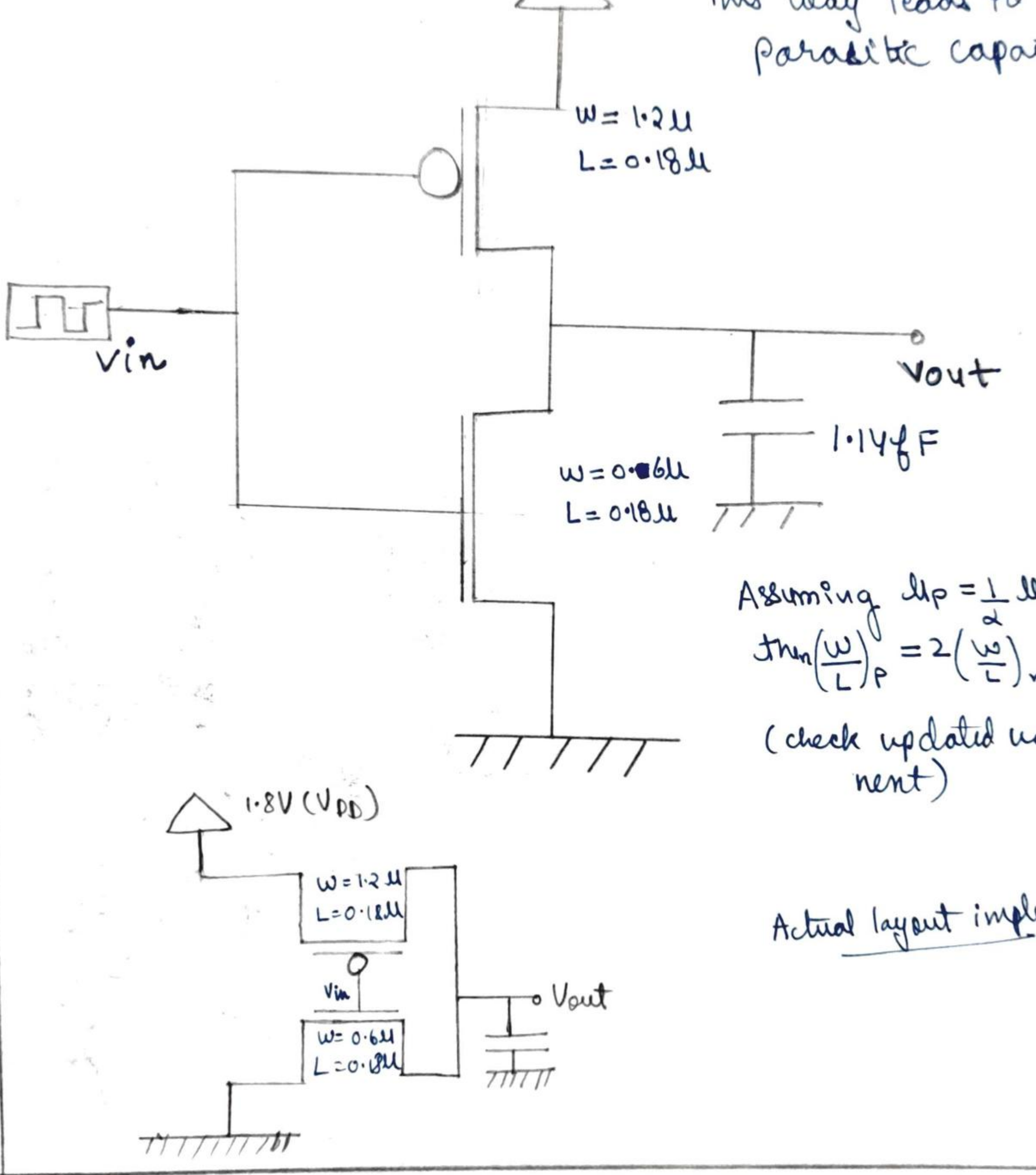
Problem Statement:- Design of an inverter

Design a CMOS inverter at 500 MHZ with load Capacitance of 10pF.

* Use of CMOS to get highest output voltage swing compared to any other design style.

Schematic:-

Representation Purpose only.
This way leads to more parasitic capacitance.



Assuming $\mu_p = \frac{1}{\alpha}\mu_n$,
then $\left(\frac{W}{L}\right)_p = 2\left(\frac{W}{L}\right)_n$

(check updated values next)

Actual layout implementation

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Determining W_p, W_n :-

When observing the outputs of delay graph (V_{out} vs t_p) based on the assumption of $\frac{W_n}{W_p} = 2$, the $T_{PLH} = 10\,pS$,

and $T_{PHL} = 15\,pS$, i.e. $T_{PLH} \neq T_{PHL}$

It is known that the maximum current drive is at $V_M = V_{th}$ (switching threshold) which is $\frac{V_{DD}}{2}$ for our chosen design. To achieve that, one condition must satisfy: $T_{PHL} = T_{PLH}$ (i.e. equal current drive)

* Varying W_p/W_n, keeping either constant, after various iterations, the required W_p/W_n came out to be 1.3 for W_p/W_n equal.

* For this design, given $L = 180nm$, $W_n = 0.600\,um$ that is $W_p = 0.780\,um$

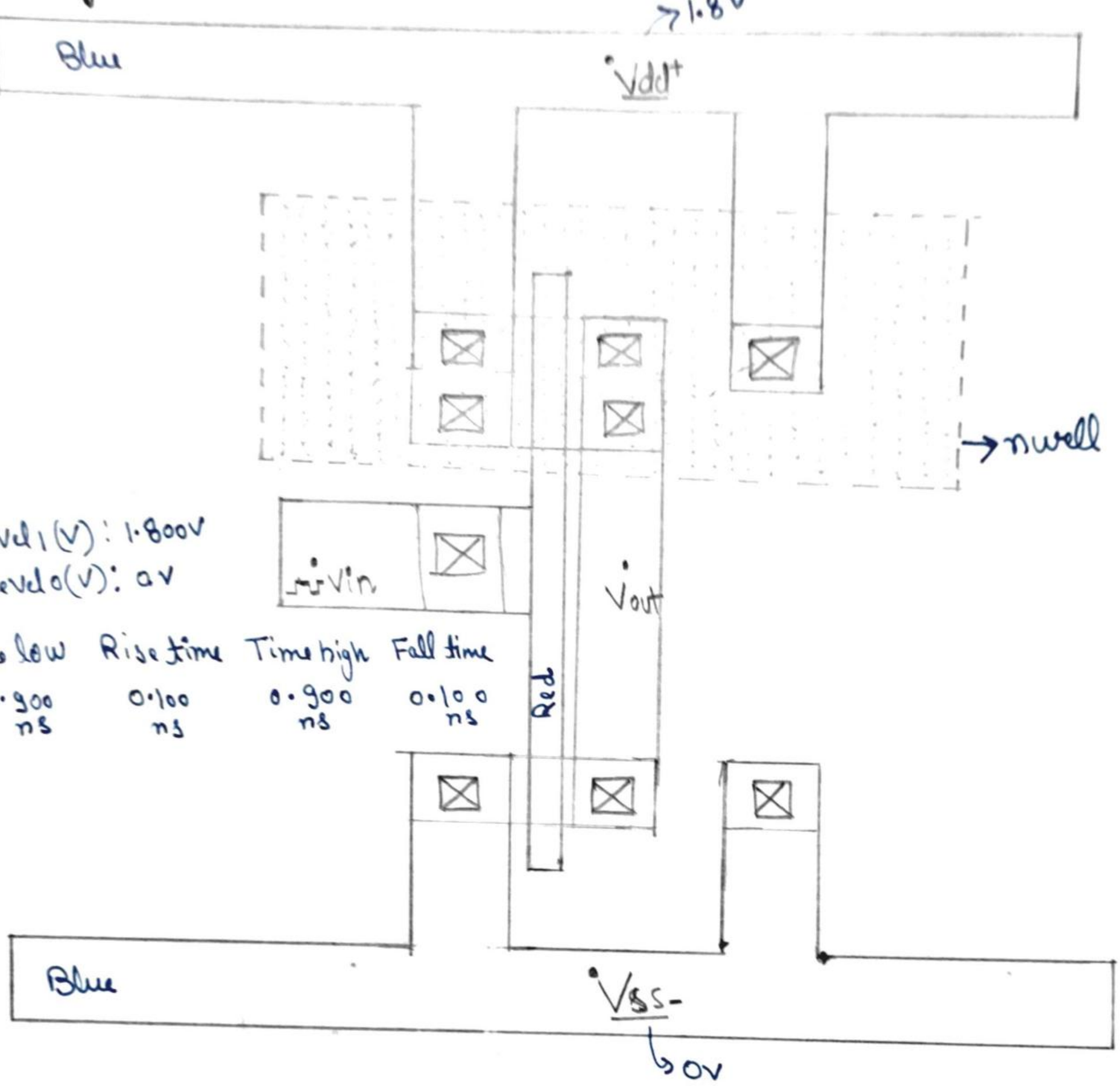
* Finally, $T_{PHL} = T_{PLH} = 10\,pS$ (although due to some problems with microwind software, exact, L, W_p, W_n values could not be set).

$\Rightarrow \left(\frac{W}{L}\right)_n = 3.33, \left(\frac{W}{L}\right)_p = 4.33, \frac{W_p}{W_n} = 1.3$

* for $\frac{W_p}{W_n} > 1.3$, PMOS drives more current. (higher T_{PLH})

* for $\frac{W_p}{W_n} < 1.3$, NMOS drives more current. (lower T_{PLH})

Layout:-



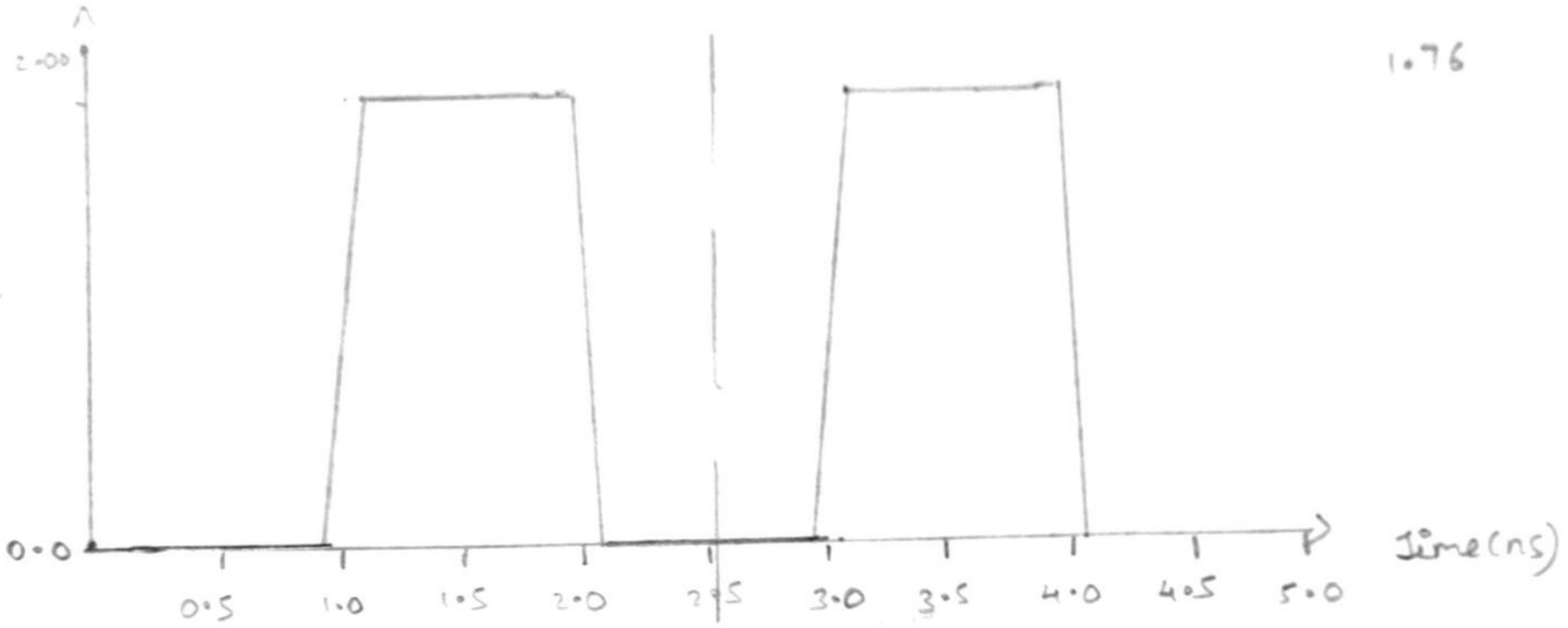
Time low	Rise time	Time high	Fall time
0.900 ns	0.100 ns	0.900 ns	0.100 ns

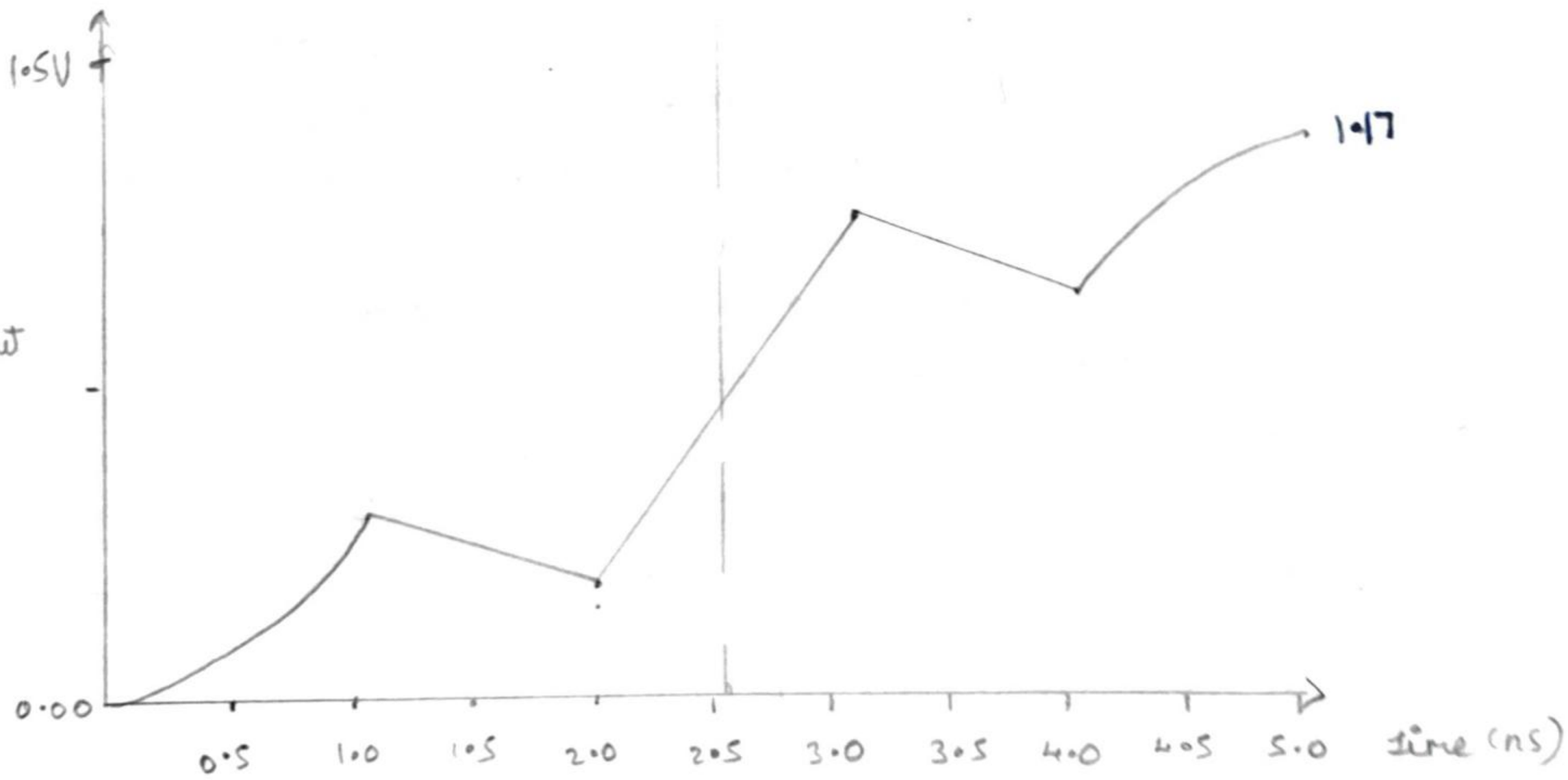
① ▷RC is checked using Microwind, which gives no errors.

② PEx extraction (Microwind) => final output capacitance = 1.093ff (0.0093% of given 10pf)

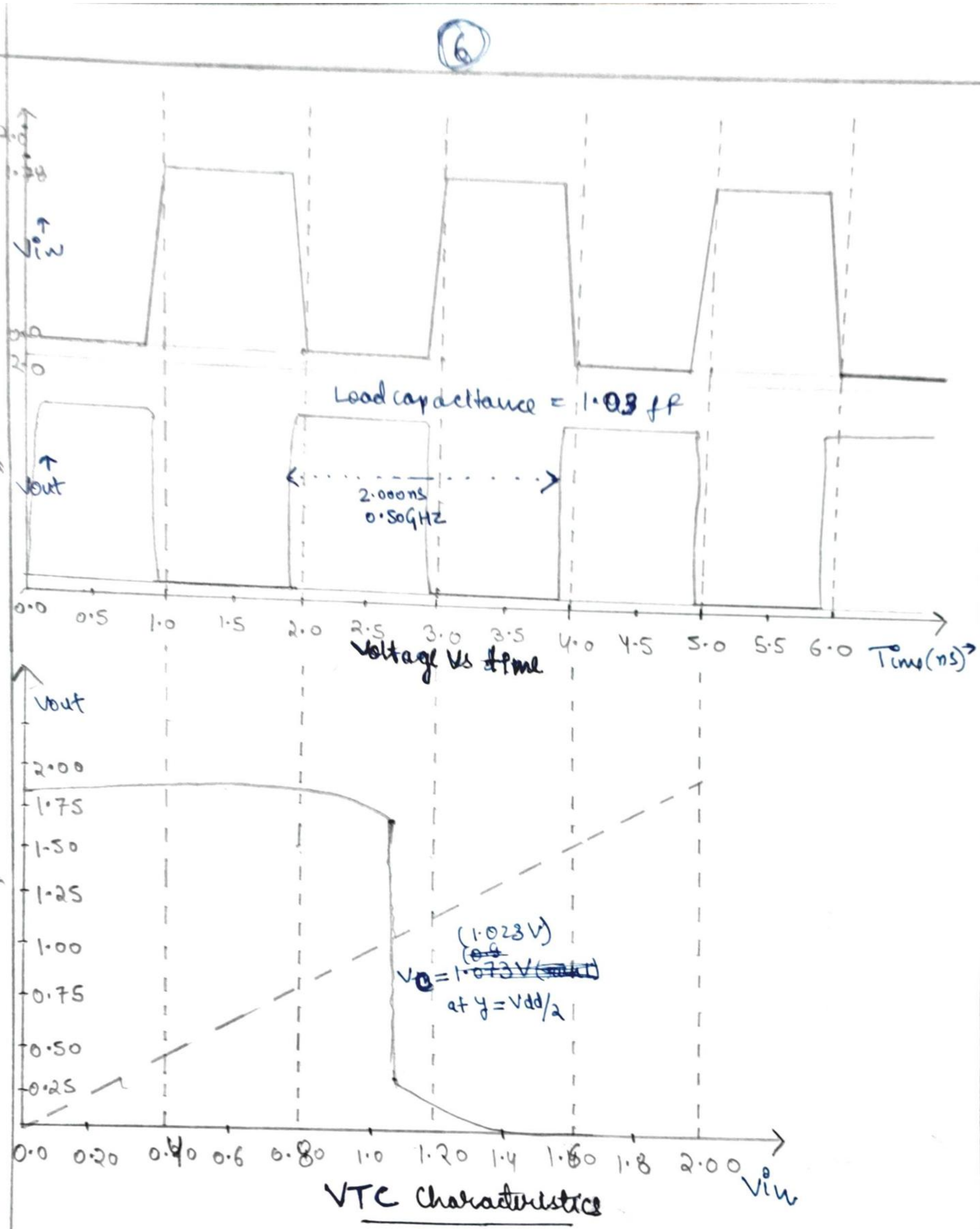
③ DSCH was used to draw schematic and Microwind for layout. Both of them match and LVS is passed.

Inverter output with 1pf load :-

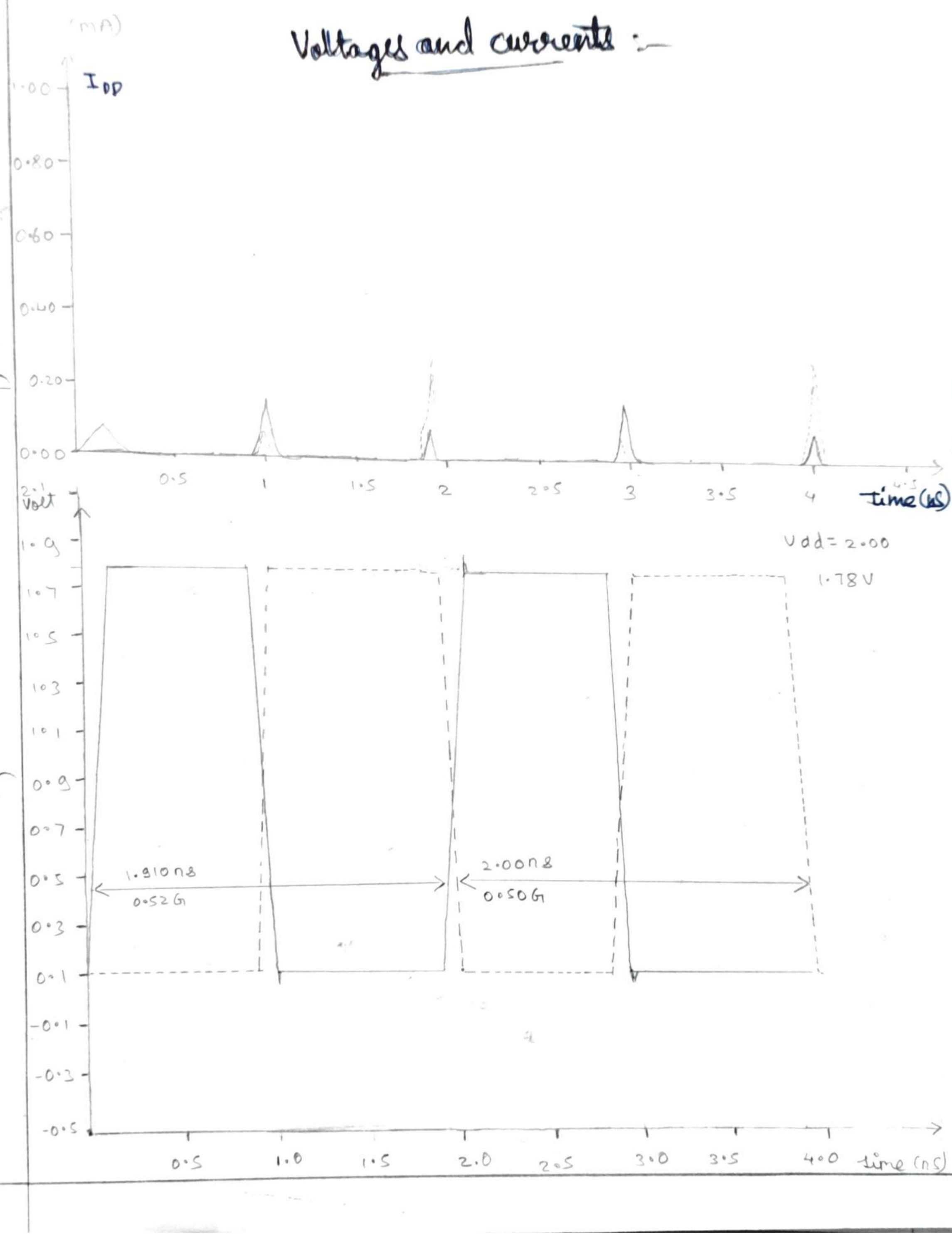




Remarks:- Not a feasible design.



Voltages and currents :-



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Calculations :-

$C_g = 2.18ff$ $C_L = 1.03ff$, $V_{DD} = 1.8V$, $f = 500MHz$ (of operation)

Switching power for a cycle = $C_L V_{DD}^2$

Switching power per unit time = $C_L V_{DD}^2 f$

$= (1.03 \times 10^{-15} \times (1.8)^2 \times 5 \times 10^8)\ W$

$= 1.6686\ \mu W$

Dynamic power (by Mentor) = $4.039\ \mu W$

Short circuit power = Dynamic power - Switching power

$= 2.3704\ \mu W$

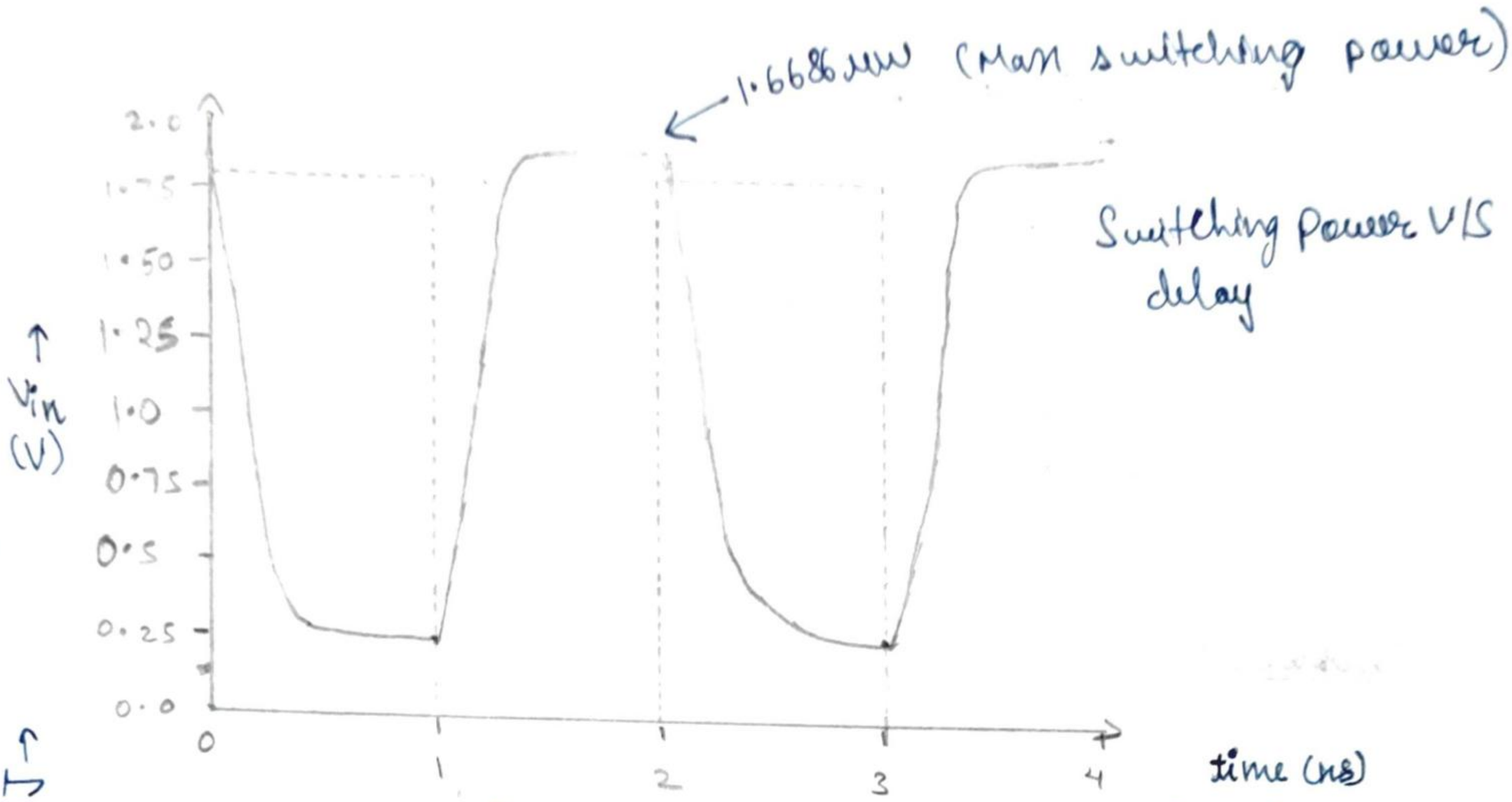
Expected dynamic power consumption (1st order equations) = $C_g V_{DD}^2 f$

$= 2.18 \times 10^{-15} \times (1.8)^2 \times 5 \times 10^8$

$= 3.53\ \mu W$

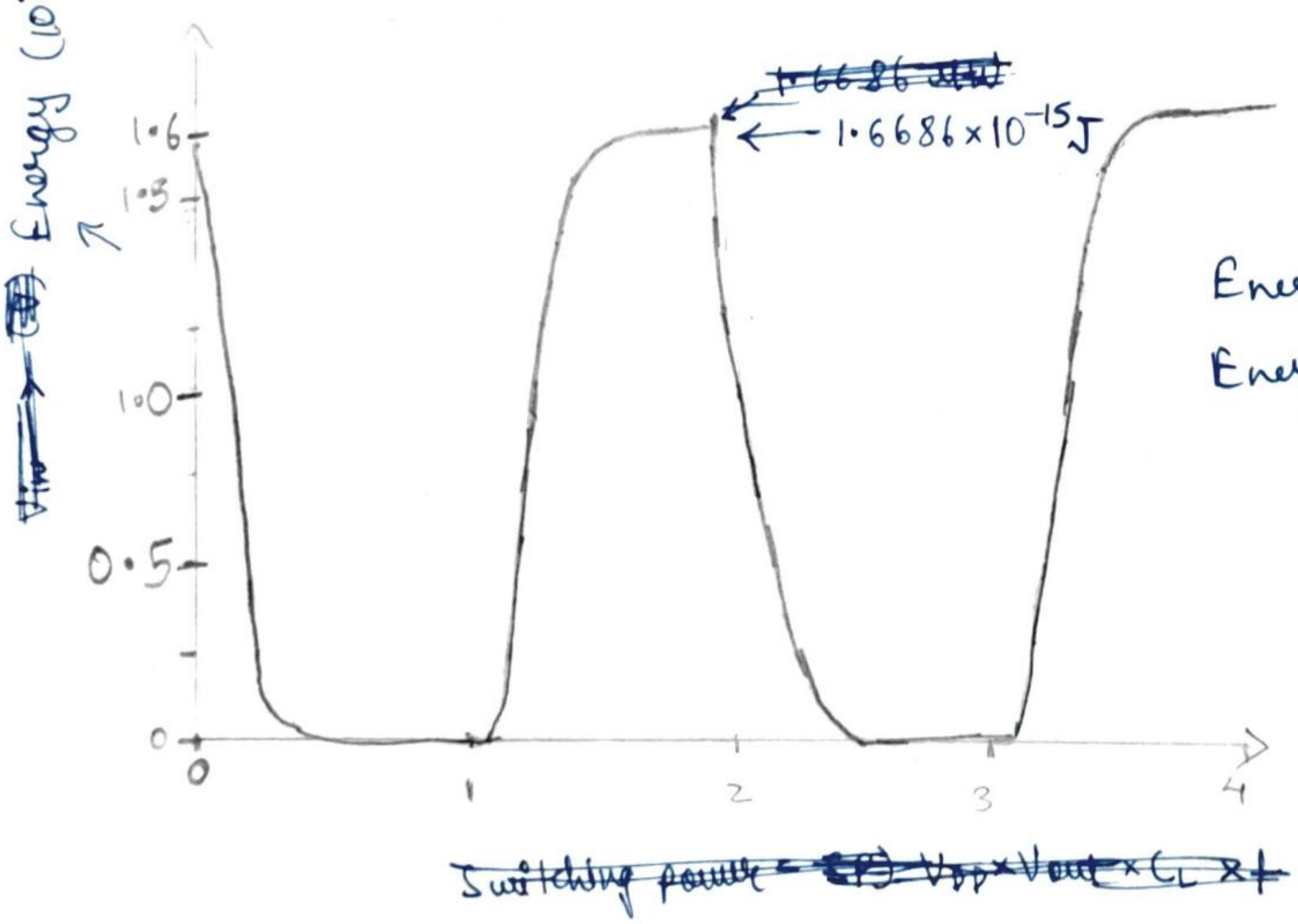
Switching power at an instant = $C_L \times V_{DD} \times V_{out} \times f$

Short circuit power = $I_{DS} \times V_{DD}$



Switching Power V/S delay

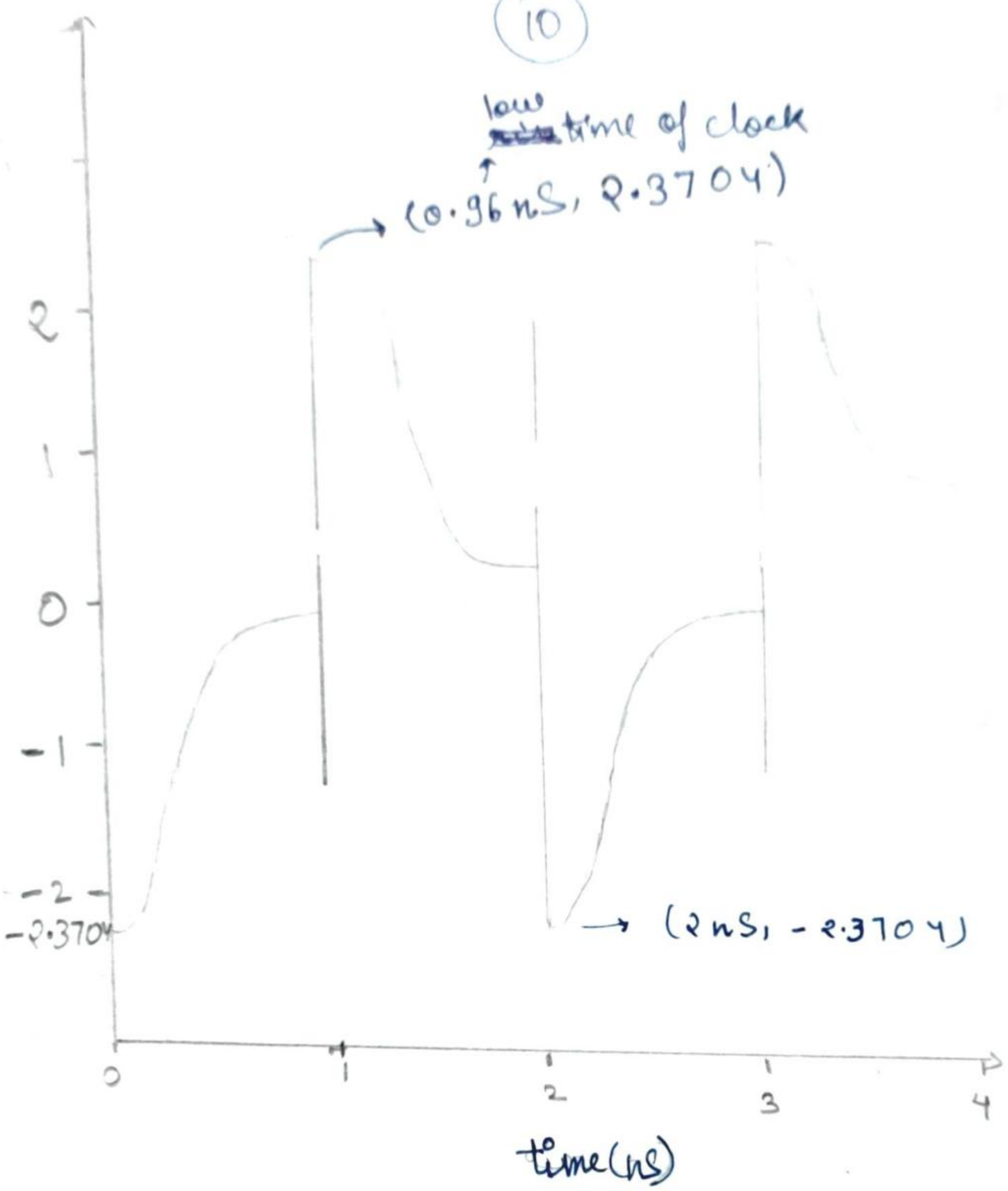
Switching power = $V_{DD} \times V_{out} \times C_L \times f$



Energy V/S delay

Energy = $\frac{C_L V_{out}^2}{2}$

~~Switching power = $V_{DD} \times V_{out} \times C_L \times f$~~



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Results and Conclusions :-

The designed inverter works for frequencies beyond 500MHz, but for observation purposes, operated at 500MHz

L =	180 nm
W_n =	0.60 μm
W_p =	0.78 μm

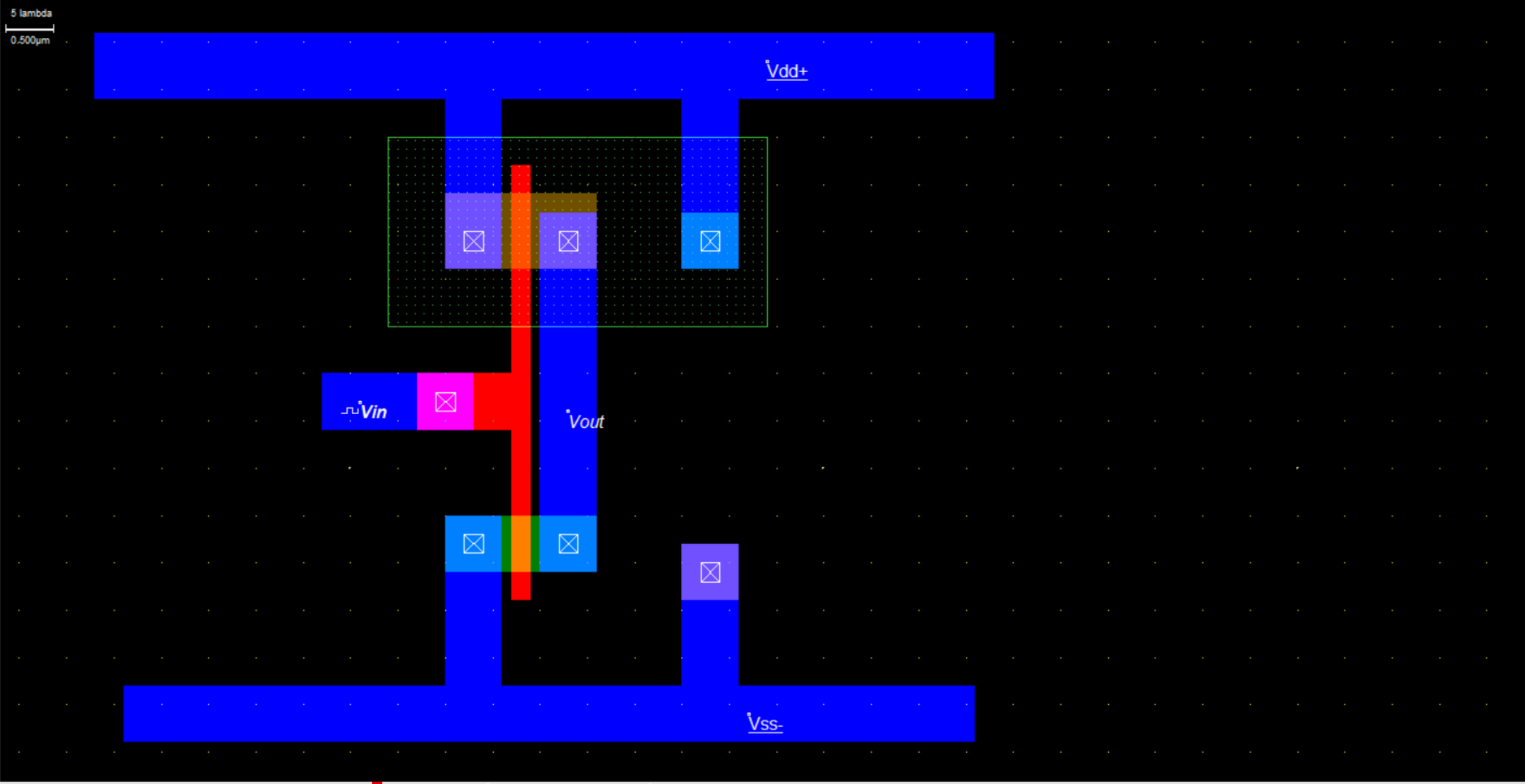
Dynamic power =	4.039 μW
Short ckt power =	2.3704 μW
Switching power =	1.6686 μW

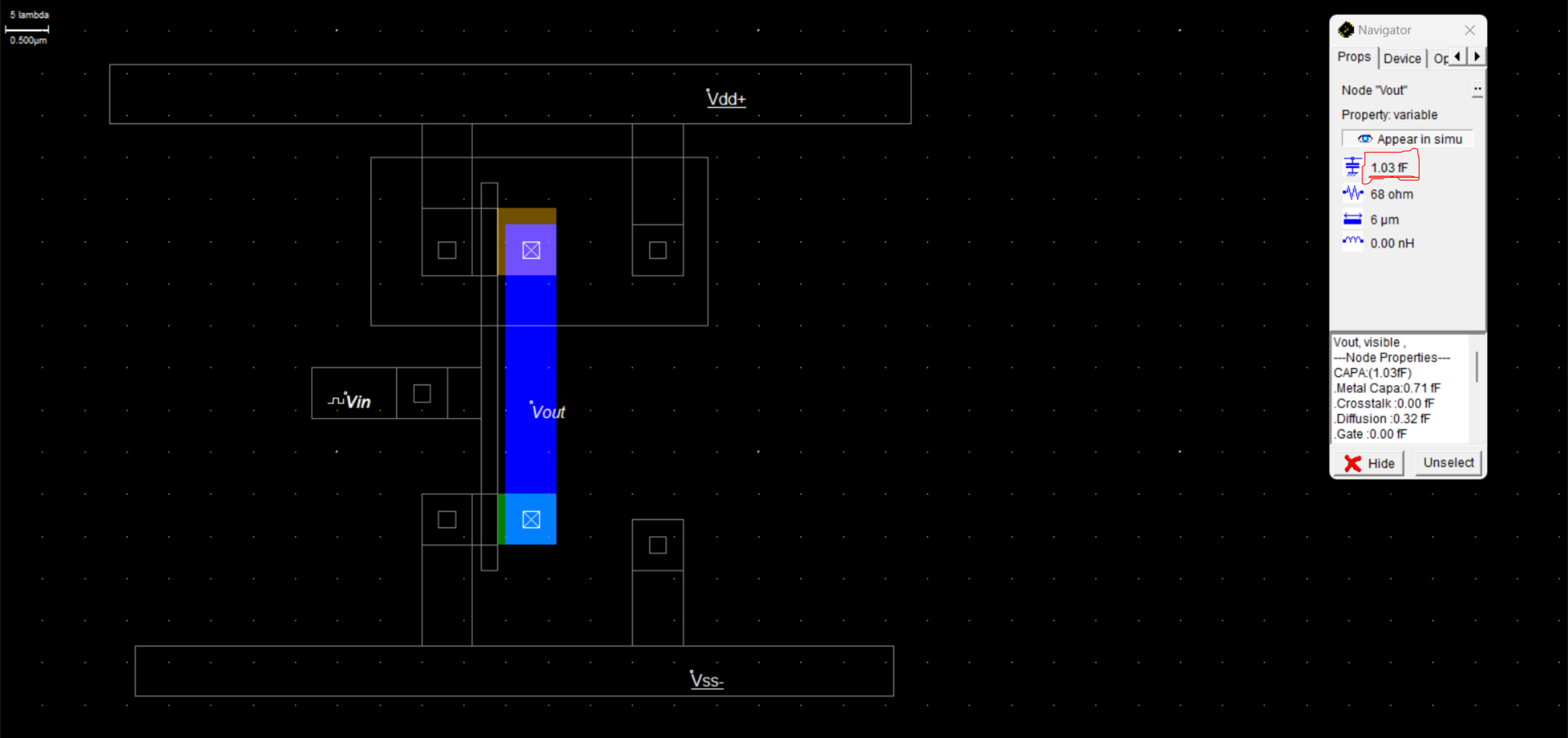
Problems

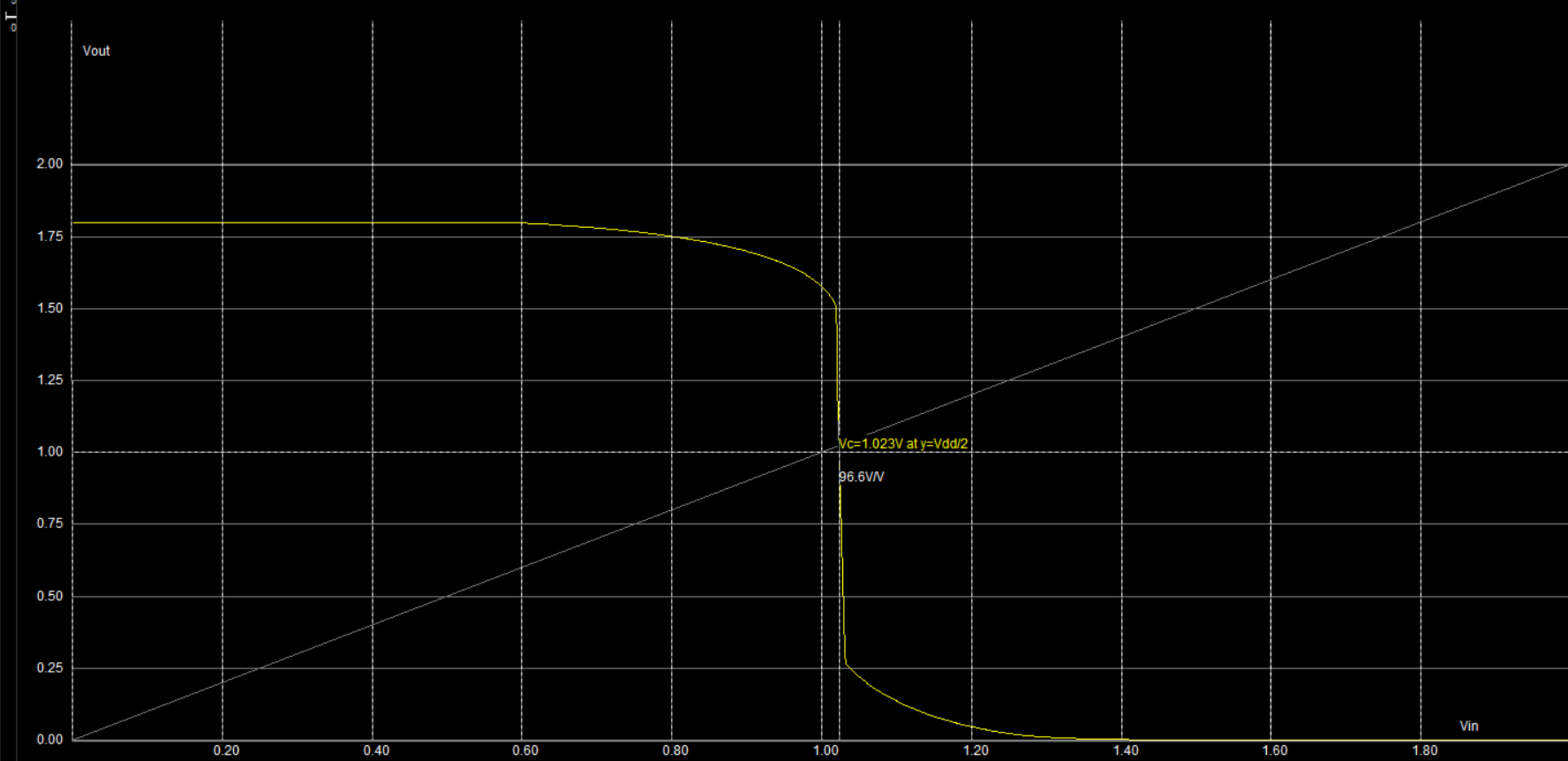
i) Load capacitance of 10 pF is not possible (rather not desired) as asked in the question, for a small digital circuit like an inverter. [consider page (5) for sample]

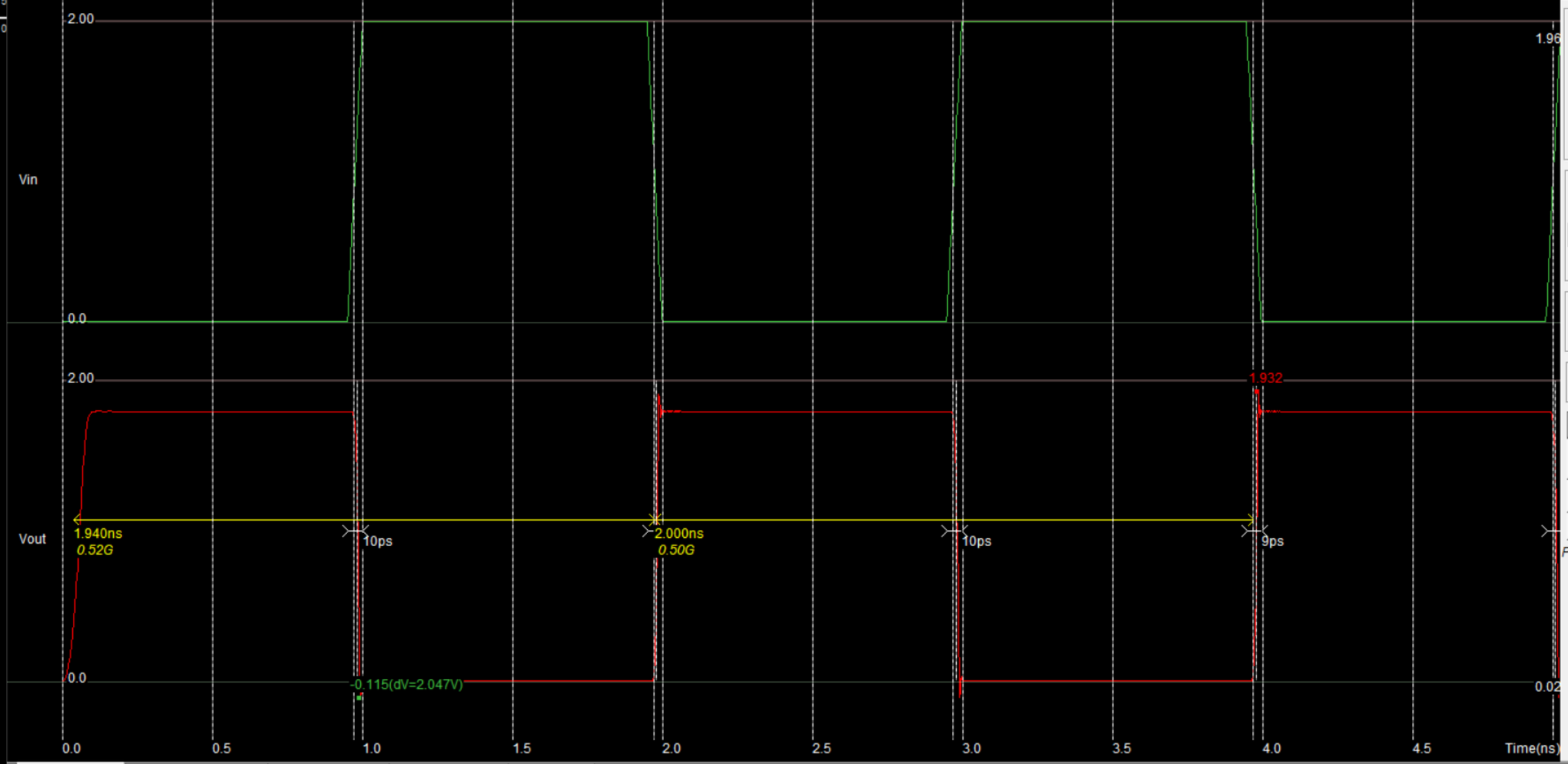
ii) Microwind kept setting the length to 200 nm in contrast to 180 nm (desired input)

iii) Energy, static and switching power could not be visualized in Microwind.


5 lambda
0.500µm
Vdd+
Vin
Vout
Vss-


5 lambda
0.500µm
Vdd+
Vin
Vout
Vss-
Navigator
Props
Device
Op
Node "Vout"
Property: variable
Appear in simu
1.03 fF
68 ohm
6 µm
0.00 nH
Vout, visible ,
---Node Properties---
CAPA:(1.03fF)
.Metal Capa:0.71 fF
.Crosstalk :0.00 fF
.Diffusion :0.32 fF
.Gate :0.00 fF
Hide
Unselect


Vout
2.00
1.75
1.50
1.25
1.00
0.75
0.50
0.25
0.00
0.20
0.40
0.60
0.80
1.00
1.20
1.40
1.60
1.80
Vin
Vc=1.023V at y=Vdd/2
96.6V/V



Display
- delay
- Bus value between...
- Vin
- and...
- Vout

Evaluate
- min/max/av
- Frequency
- Vout
- FFT

Time scale
- 5n

Step(ps)
- 0.500

Reset

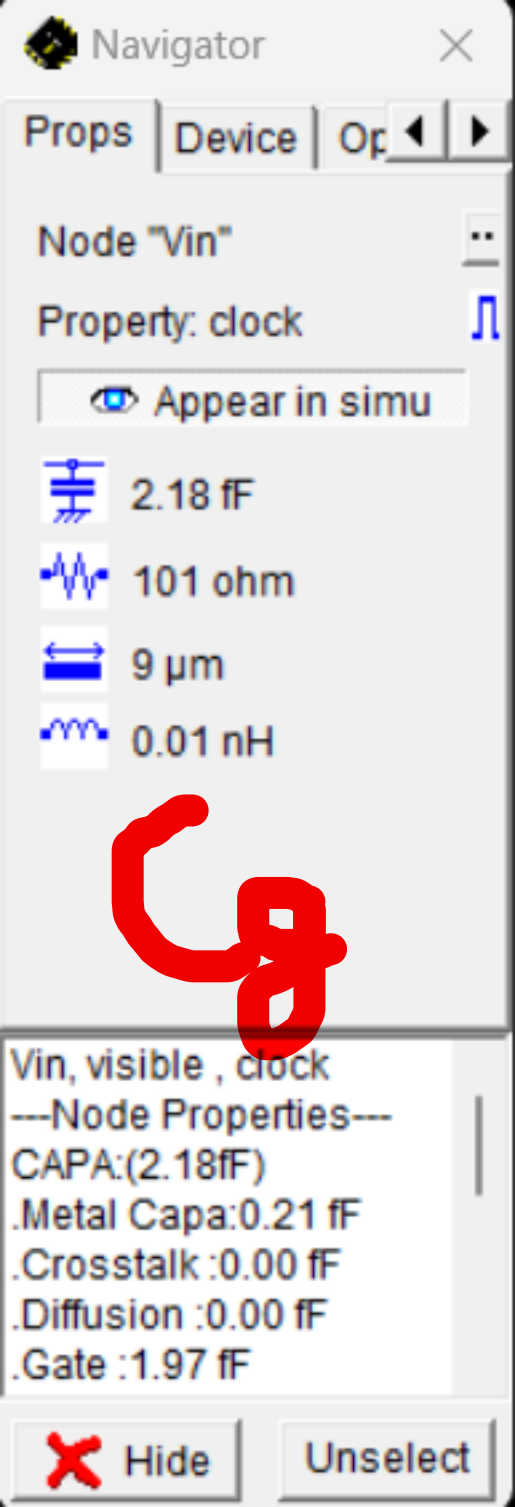
More

Close

Print

P=4.039μW

Voltage vs. time | Voltages and currents | Voltage vs. voltage | Frequency vs.time | Eye diagram


Navigator
Props
Device
Node "Vin"
Property: clock
Appear in simu
2.18 fF
101 ohm
9 µm
0.01 nH
Vin, visible , clock
---Node Properties---
CAPA:(2.18fF)
.Metal Capa:0.21 fF
.Crosstalk :0.00 fF
.Diffusion :0.00 fF
.Gate :1.97 fF
Hide
Unselect