ANALOG AND DIGITAL VLSI DESIGN

EEE F313/INSTR F313

ANALOG ASSIGNMENT
Differentiator Circuit using Telescopic OPAMP

MADE BY: -

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PROBLEM STATEMENT

Question 4

Design a Differentiator using Telescopic OPAMP as shown in the figure in Subthreshold Region:

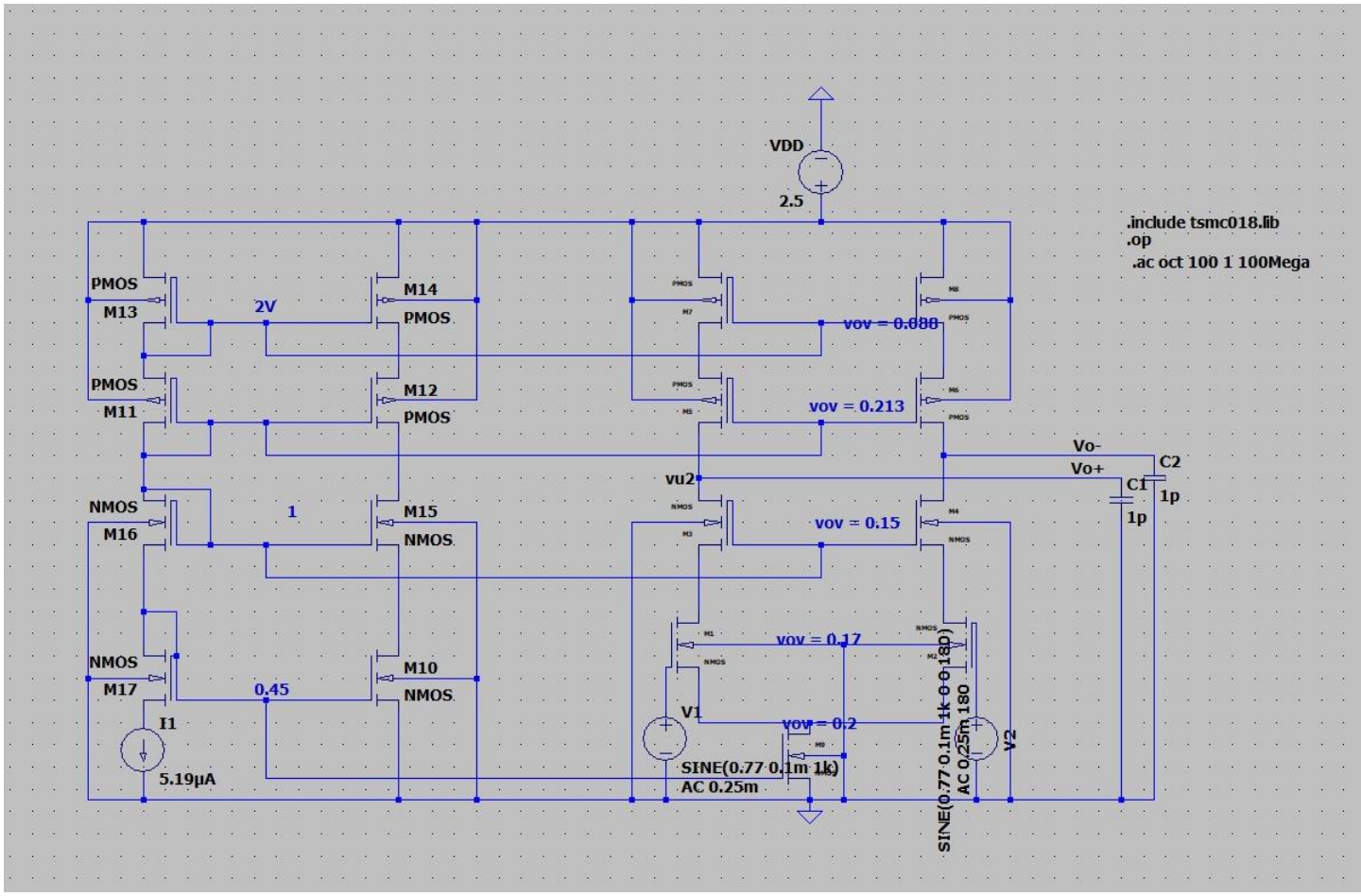
a) Analysis of all equations of your design, with a systematic derivation of all transistor's W/L ratios and simulation of the circuit for the following specifications.
b) Open loop gain (DC gain) ≥ 80 dB with slew rate ≥ 20V/usec

c) Show a biasing circuitry to bias all the voltages in your design (except the input).

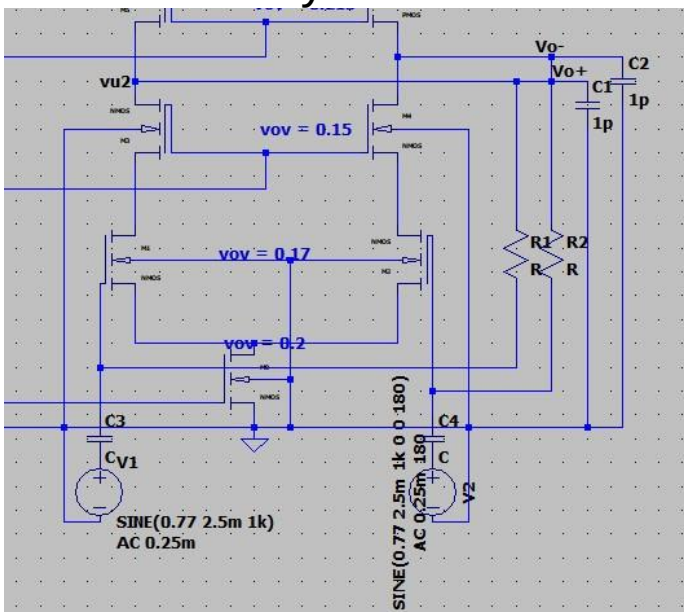
d) Calculate and plot the following parameters for your OPAMP: DC gain, Bode plot for AC gain and phase, ICMR plot, slew rate, Output voltage swing differential (dc + Transient), power consumption, and input and output offset voltage.

Technology - MOS018 library (as shared for assignment via mail)

Circuit Diagram

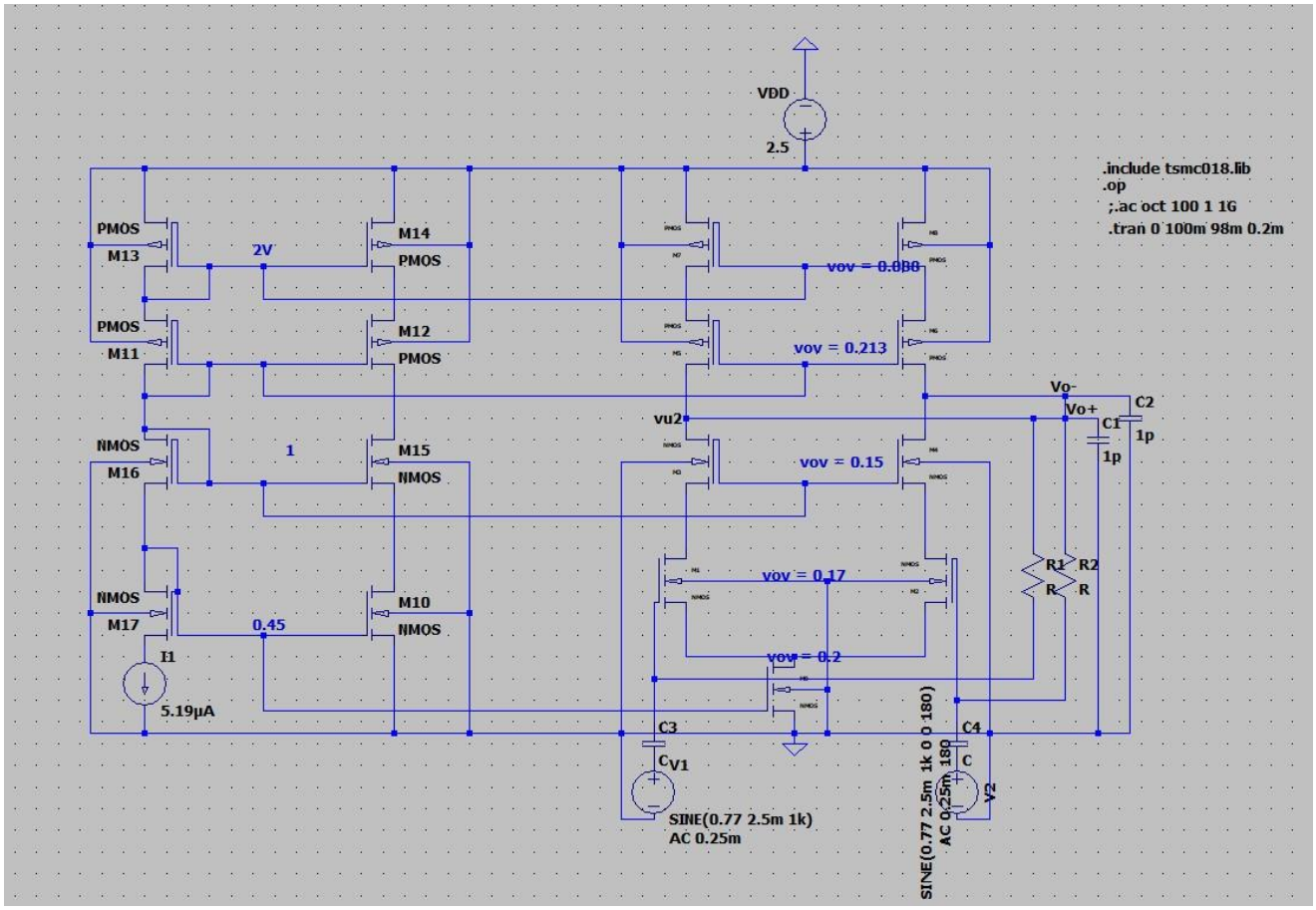


Extra Circuitry added to OPAMP



(Library used- MOS018)

Circuit Diagram



New Circuitry

Design Steps

Power Budget and current:

No power constraint was given for the question, so we began with fixing a current for the circuit. We started by fixing the current in the differential amplifier's branch as 1.5uA. But that gave some problems with the biasing circuit, we could not get the required gate voltage for the PMOS(s) in the circuit. We then decreased the current and so on with various iterations, we ended up with the design above.

Overdrive voltages:

The differential voltage swing is 2.5 V; thus, the sum of overdrive voltages (modulus for PMOS) is 1.25. Overdrive Voltages (M 1 + 3 + 5 + 7 + 9) = 1.25. We can take same overdrive voltages for all the MOSFETSs, but since the current through them is not equal, depending on the current from them, we decided their overdrive voltages. The transistor with the maximum current has maximum overdrive voltage.

W/L of the MOS:

Assuming the overdrive voltage and drain current we can find the starting W or L of MOS from the standard drain current equation of the MOS. In our case, we fixed the L to be 0.35u. We could use the first order equations, but to avoid the errors due to body effect in the 5-transistor long chain, we decided to go with LTSPICE simulations for fixing W/L. Moreover, we fixed the VDS voltages of all the transistors, with 3:1 ratio for PMOS/NMOS respectively.

Now, we do new sizing of the transistors which were based on several careful iterations. The length of the current mirror is chosen to be large to have better resistance of the current mirror.

The minimum lengths of all the MOSFETS in the design is 350nm. Thewidth for different MOSFETS is summarized in the table below.

W/L table

MOSFET No	W/L	MOSFET No	W/L
M1	1.463u/.35u	M11	0.35u/.35u
M2	1.463u/.35u	M12	0.35u/.35u
M3	10.987u/.35u	M13	15.128u/.35u
M4	10.987u/.35u	M14	15.128u/.35u
M5	12.129u/.35u	M15	34.545u/0.35u
M6	12.129u/.35u	M16	34.545u/.35u
M7	0.737u/.35u	M17	24.93u/0.35u
M8	0.737u/.35u		
M9	3.1814u/.35u		
M10	24.93u/.35u		

DC Operating Point

Voltage and Current Table

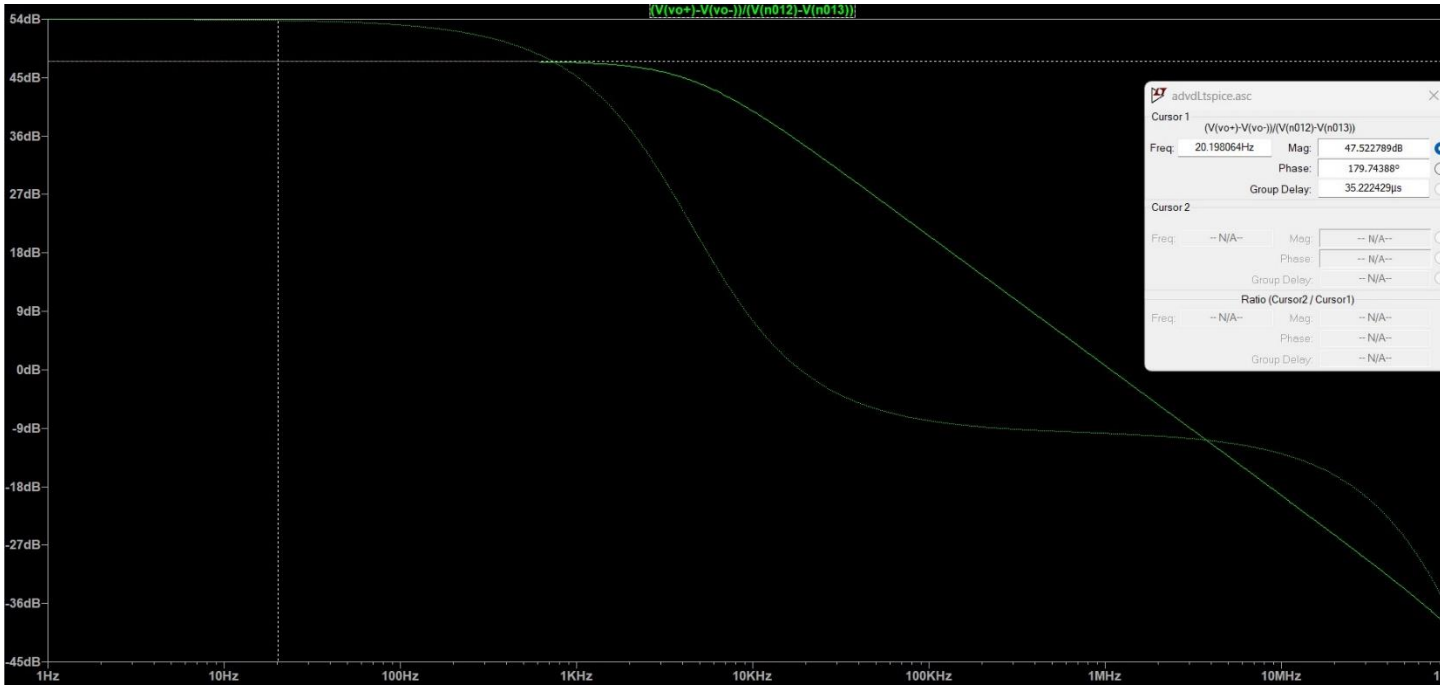
--- Operating Point ---

V(n009):	0.507796	voltage
V(n012):	0.77	voltage
V(n015):	0.250431	voltage
V(n013):	0.77	voltage
V(n010):	0.507796	voltage
V(n006):	0.999477	voltage
V(vo+):	1.74408	voltage
V(vo-):	1.74408	voltage
V(n004):	1.74603	voltage
V(n001):	2.5	voltage
V(n005):	1.74603	voltage
V(n002):	1.9999	voltage
V(n008):	0.449513	voltage
V(n003):	2.11023	voltage
V(n007):	1.94463	voltage
V(n011):	0.45693	voltage
V(n014):	-0.000448543	voltage
Id(M14):	5.12978e-006	device_current
Ig(M14):	-0	device_current
Ib(M14):	3.99773e-013	device_current
Is(M14):	-5.12978e-006	device_current
Id(M13):	-5.19e-006	device_current
Ig(M13):	-0	device_current
Ib(M13):	5.10096e-013	device_current
Is(M13):	5.19e-006	device_current
Id(M12):	5.12978e-006	device_current
Ig(M12):	-0	device_current
Ib(M12):	9.65143e-013	device_current
Is(M12):	-5.12978e-006	device_current
Id(M11):	-5.19e-006	device_current
Ig(M11):	-0	device_current
Ib(M11):	2.02062e-012	device_current
Is(M11):	5.19e-006	device_current
Id(M8):	2.9661e-007	device_current
Ig(M8):	-0	device_current
Ib(M8):	7.63966e-013	device_current
Is(M8):	-2.9661e-007	device_current
Id(M7):	-2.9661e-007	device_current
Ig(M7):	-0	device_current
Ib(M7):	7.63966e-013	device_current
Is(M7):	2.9661e-007	device_current
Id(M6):	2.9661e-007	device_current
Ig(M6):	-0	device_current
Ib(M6):	1.52989e-012	device_current
Is(M6):	-2.96612e-007	device_current

DC Operating Point

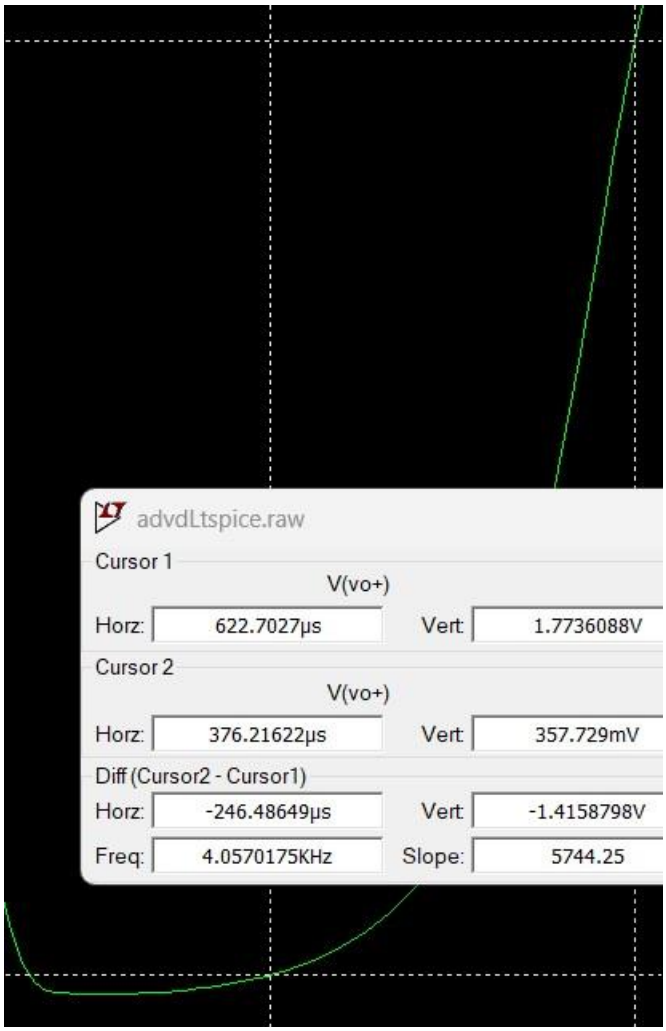
Is(M6):	-2.96612e-007	device_current
Id(M5):	-2.96612e-007	device_current
Ig(M5):	-0	device_current
Ib(M5):	1.52989e-012	device_current
Is(M5):	2.9661e-007	device_current
Id(M17):	-5.19e-006	device_current
Ig(M17):	0	device_current
Ib(M17):	-4.5889e-013	device_current
Is(M17):	5.19e-006	device_current
Id(M10):	5.12978e-006	device_current
Ig(M10):	0	device_current
Ib(M10):	-4.6693e-013	device_current
Is(M10):	-5.12978e-006	device_current
Id(M16):	-5.19e-006	device_current
Ig(M16):	0	device_current
Ib(M16):	-1.46899e-012	device_current
Is(M16):	5.19e-006	device_current
Id(M15):	5.12978e-006	device_current
Ig(M15):	0	device_current
Ib(M15):	-2.42156e-012	device_current
Is(M15):	-5.12978e-006	device_current
Id(M9):	5.93218e-007	device_current
Ig(M9):	0	device_current
Ib(M9):	-2.6043e-013	device_current
Is(M9):	-5.93217e-007	device_current
Id(M4):	2.96612e-007	device_current
Ig(M4):	0	device_current
Ib(M4):	-2.27187e-012	device_current
Is(M4):	-2.9661e-007	device_current
Id(M3):	-2.9661e-007	device_current
Ig(M3):	0	device_current
Ib(M3):	-2.27187e-012	device_current
Is(M3):	2.96612e-007	device_current
Id(M2):	-2.96609e-007	device_current
Ig(M2):	0	device_current
Ib(M2):	-7.78226e-013	device_current
Is(M2):	2.9661e-007	device_current
Id(M1):	2.9661e-007	device_current
Ig(M1):	0	device_current
Ib(M1):	-7.78226e-013	device_current
Is(M1):	-2.96609e-007	device_current
I(C2):	1.74408e-024	device_current
I(C1):	1.74408e-024	device_current
I(I1):	5.19e-006	device_current
I(V2):	0	device_current
I(V1):	0	device_current
I(Vdd):	-1.0913e-005	device_current

Gain Plot



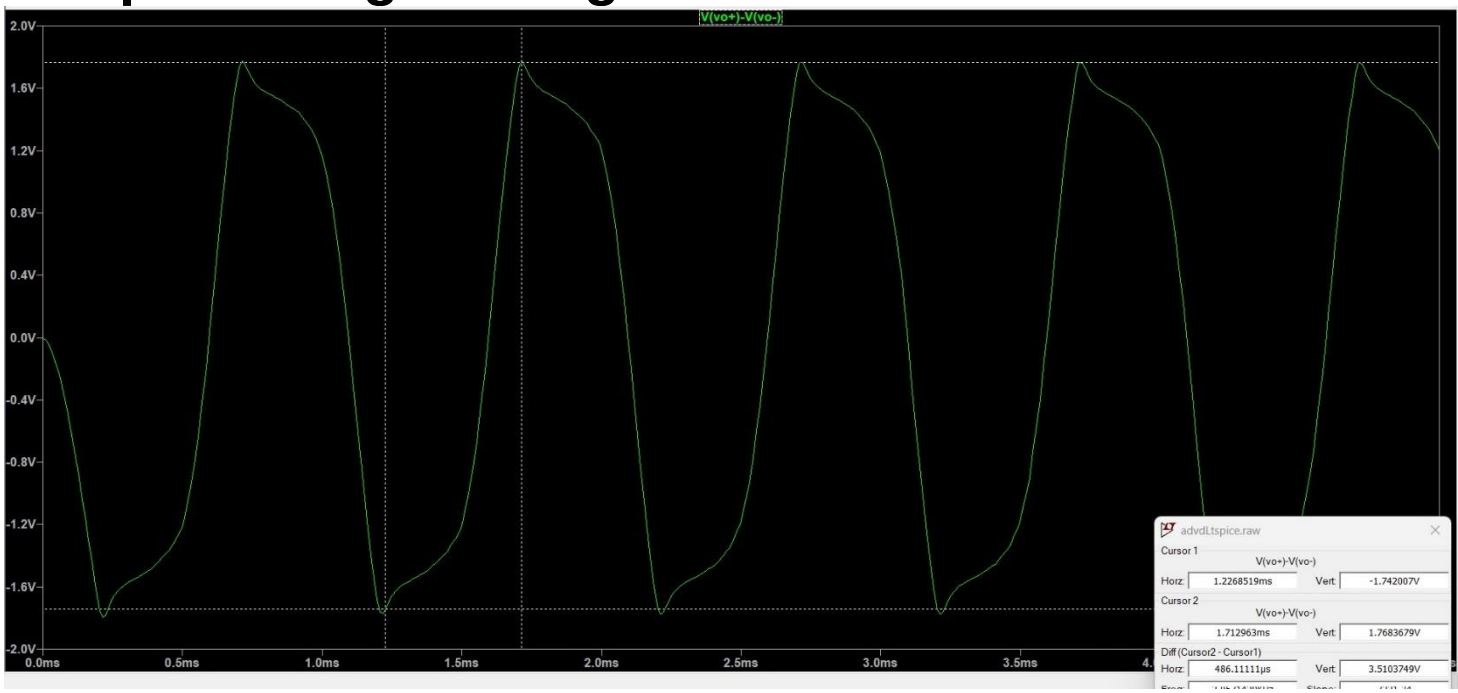
Gain of 47.52 dB is obtained.

Slew Rate



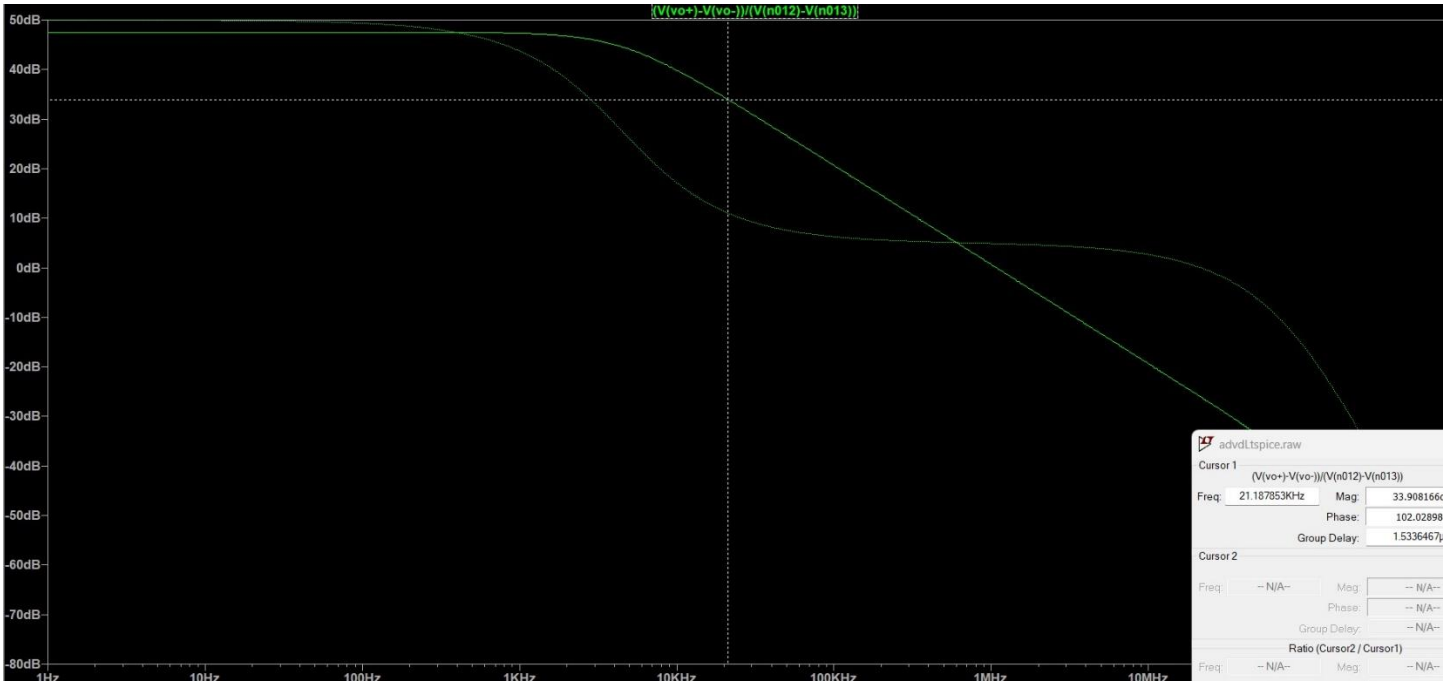
Slew rate= $(V(90\%) - V(10\%))/time$ =5736.0996V/s

Output voltage Swing



Output voltage swing of 3.51

3 dB Frequency



Input and output offset voltage

Output offset voltage

```
        --- Operating Point ---

V(n009):        0.507796        voltage
V(n012):        0.77            voltage
V(n015):        0.250431        voltage
V(n013):        0.77            voltage
V(n010):        0.507796        voltage
V(n006):        0.999477        voltage
V(vo+):         1.74408         voltage
V(vo-):         1.74408         voltage
```

The difference in output voltages is zero (as both the arms are matched). Thereby the output offset voltage is zero.

Input offset

```
V(vout+):       4.43704e-009    voltage
V(vout-):       4.43704e-009    voltage
```

The input offset voltage is Vos= (Difference in outputvoltage)/Gain of OPAMP when no input is given.

The differential output is zero when no input is given and thereby the input offset voltage iszero.

Conclusion

S.no	Parameter	Value	Required Specification
1	Gain (At 27C)	48.2dB	>=80dB
2	Output Swing	3.5103V	-
3	Input Offset	0	-
4	Output offset	0	-
5	3dB	21.1878kHz	-
7	Slew Rate	5736.0996V/s	20V/usec
8	Power Dissipation	27.45 uW	-
10	Phase Margin	48.5° (Stable)	-
11	C_{load}	1pf	<=1pF

Problem Faced

- We faced a problem in getting a gain over 80dB.
- The Gain changes drastically with the temperature.
- Due to unavailability of Cadence, we were not able to do analysis for process corners.

Innovation

- Biasing Circuit: - We designed a Biasing Circuit symmetric toour amplifier so that bias could be generated for all the gates for our circuit.