Submission of Project Type Course Pre-Registration Application

Inbox ×

noreply@bits-pilani.ac.in Fri, Nov 18, 2022, 8:08 AM

to me

Dear NAMAN MEHTA,

Your application for pre-registration of Project Type Course in the Second Semester 2022 - 2023 has been successfully submitted for the approval by the concerned.

The details are as follows:

Course No.	:	INSTR F376
Course Title	:	DESIGN PROJECT
Project Title	:	Negative Capacitance and MOS simulation (TCAD)
Department	:	Dept of Elect & Electronics
Supervisor	:	SATYENDRA KUMAR MOURYA

You will receive an email when your application status (Approved/Not Approved) is decided. Alternatively, you may view the status of the same via ERP Project application page.

For any clarifications you can contact the AUGSD office.

Associate Dean (AUGSD)

NEGATIVE CAPACITANCE WORKING AND SIMULATION USING SILVACO TCAD

BITS Pilani
Pilani | Dubai | Goa | Hyderabad

Presented By: Naman Mehta 2019B2A80981P

Instructor: Dr. Satyendra Kumar Maurya

Abstract

This document is based upon the recent developments in the field of electronic devices, especially MOSFETs (metal-oxide-semiconductor field-effect transistor) and FINFETs (fin field-effect transistor).

Our focus in this document will be on Ferro-Electric materials and how they can be used with the existing technology to make that even better.

We would start with the introduction of Ferro-Electric materials and how they lead to Negative Capacitance, discussing some of their properties and why those properties are groundbreaking for the present-day Electronics industry. We will also discuss why these Ferro-Electric materials are considered important to solve one of the most challenging problems in the world of electronic devices.

We will compare some of the results achieved by using the Ferro-Electric materials and how they are superior to those when these materials are not used.

Towards the end we would talk about modelling of various electronic devices using Silvaco TCAD with the use of Ferro-Electric materials.

Acknowledgement

First, to thank Birla Institute of Technology and Science and Dr. Satyendra Kumar Maurya, for providing me with the opportunity to do this project.

Dr. Satyendra Maurya provided all the resources and mentorship that were essential for this project.

On the recommendation of Dr. Satyendra Maurya, I followed the works of Dr. Chenming Hu, Dr. Yogesh Singh Chauhan and Dr. Girish Pahwa who are experts in this field. Their work in this field is aspiring and has motivated me to investigate the field in greater detail.

I would also like to thank all the teaching assistants who have helped me with all my doubts regarding the project.

Lastly, I would like to thank my friends who have helped me in many ways during the project.

Introduction

Moore's law has been known to us since 1965 and is the observation that the number of transistors in an integrated circuit doubles about every two years. Following the trend, we have now reached a place where the dimensions of a transistor are in nanometers.

Although this law has been upheld for a long time, in the recent future, it is predicted that the number of transistors in an IC cannot keep growing exponentially and thus the saturation of Moore's law would be achieved.

Decreasing the dimensions of a MOSFET beyond a certain point has led to various short channel effects and various other problems. Consider the image below:

$$I_D = 0 \begin{cases} V_{GS} > V_T \end{cases}$$

$$I_{D,lin} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] \begin{cases} V_{GS} \leqslant V_T \\ V_{DS} > V_{GS} - V_T \end{cases}$$

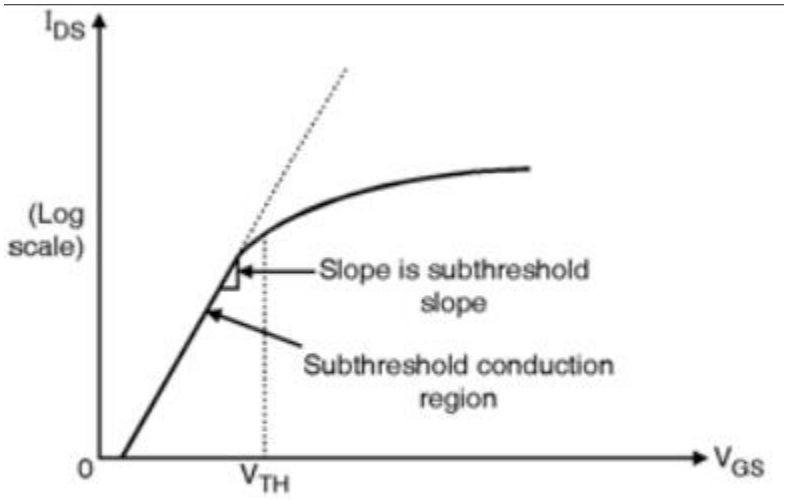
$$I_{D,sat} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \begin{cases} V_{GS} \leqslant V_T \\ V_{DS} \leqslant V_{GS} - V_T \end{cases}$$

If one would consider the current equation of a MOSFET, as we decrease its dimensions, to maintain the same I_d, the difference ($V_{gs} - V_t$) must increase. But this in turn means that the gate voltage must be increased to do the same. But this leads to issues like enormous heat density in the semiconductor chip and higher power consumption.

How Ferro-Electric materials can be used to show the phenomenon of negative capacitance and how this negative capacitance can help us tackle this problem is what we will discuss ahead. Further, tackling this problem will help us to follow Moore's law for more time.

Subthreshold Slope (SS) and Boltzmann Tyranny

Talking about an ideal MOSFET, as soon as the gate-source voltage is below the threshold voltage, the MOSFET should stop conducting. But for all practical purposes, even below the levels of threshold voltage, there is some observable current I_{off} , that is, there is sub-threshold conduction.



I_{DS} Vs V_{GS} characteristics in log scale

Subthreshold Slope is an important quantity to judge the switching characteristics of a MOSFET. We want the ratio of On and Off current (in subthreshold region) to be very high and for that purpose, the SS should be very low. In the scaled devices, due to the short channel effects, the minimum value of SS is restricted to 60 mV/decade. This value of 60 mv/decade is thus known as Boltzmann Tyranny.

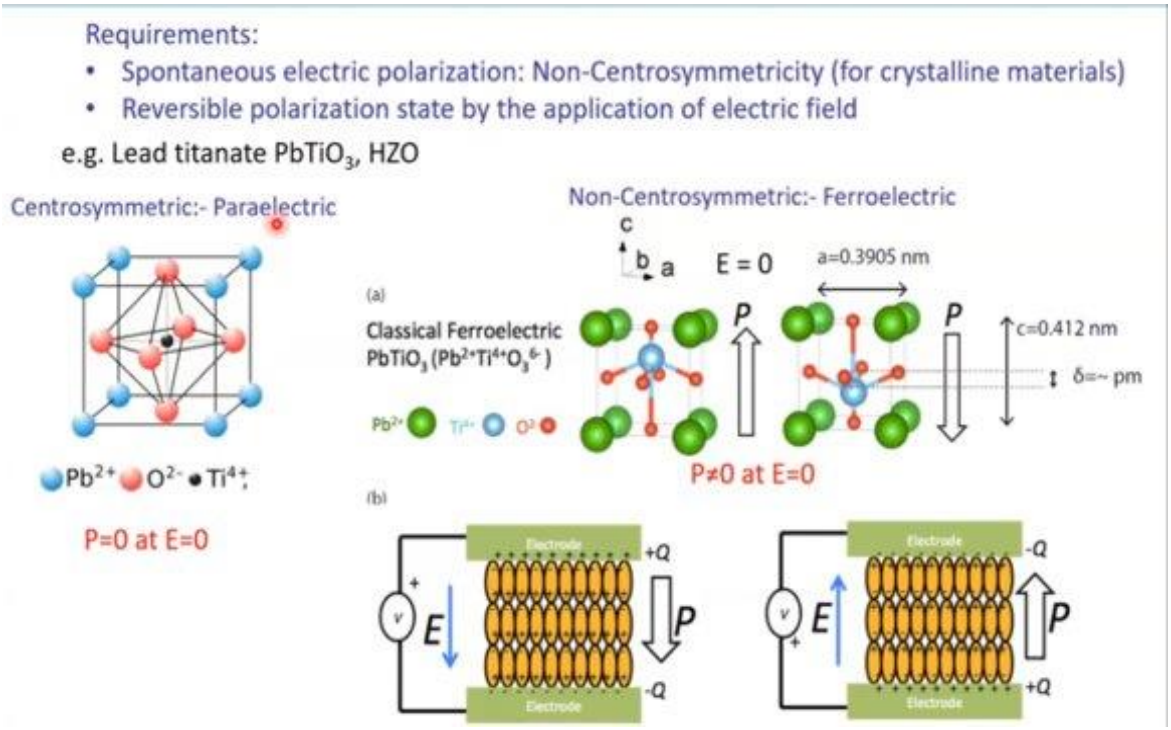
Ferro-electric materials have a promising future pertaining to the fact that using these, the Subthreshold Slope for a FINFET (or maybe a MOSFET) was demonstrated to be lower than 60 mv/decade. We will discuss it later.

It is the right time for us to now discuss Ferro-Electric materials and Negative Capacitance.

Ferro-Electric Materials

Dielectric materials can be divided into two types, namely, Paraelectric and Ferroelectric materials. (Take analogy from Paramagnetic and Ferromagnetic materials). Both materials show polarization when an external electric field is applied.

For Paraelectric material, polarization shows a linear behavior with the external electric field and is zero when no electric field (E) is applied. However, Ferroelectric materials show a hysteresis behavior of polarization with external electric field. Polarization is not zero even when E is absent. That is, there is a remanent polarization in the case of Ferroelectric material. This is the property of Ferroelectric material we would be using later for demonstrating negative capacitance. The important thing to note is, HfO2 is preferred to make ferroelectric materials from doping, because it is also compatible with CMOS process. Non-centrosymmetric unit cell leads to non-zero polarization at E = 0.



Landau Theory for Non-linear Dielectrics

Landau-Devonshire Theory[1]:

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \quad , \alpha = \alpha_0(T - T_0), \alpha_0 > 0$$

G = free energy density (per unit vol.), P = Polarization, T = Temperature,
T_0 =Curie Temperature, E = Electric Field

- α, β and γ are Landau coefficients.
- In general, α and β can be +ve or –ve but γ is always +ve for stability reasons.

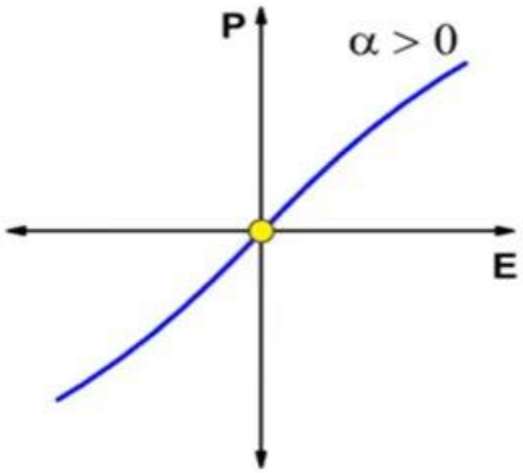
Landau-Khalatnikov (L-K) Theory[2]:

Dynamics of G is given by: $\delta \frac{dP}{dt} = -\frac{\partial G}{\partial P}$, where δ = Polarization damping factor

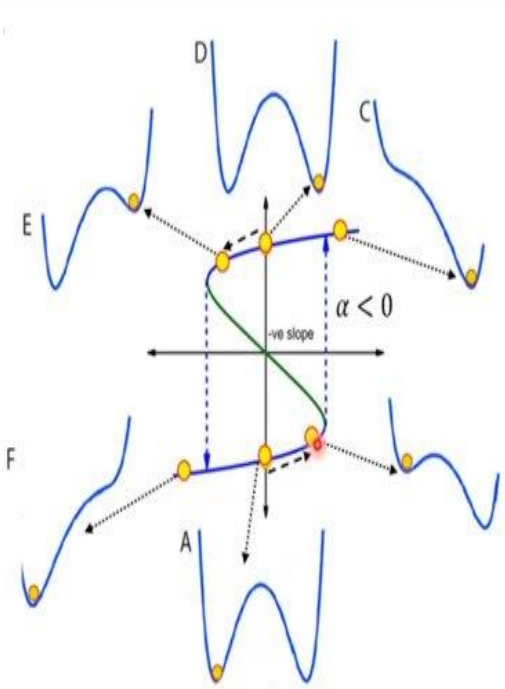
In steady state,

$$\delta \frac{dP}{dt} = -\frac{\partial G}{\partial P} = 0 \implies E = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

(Energy minima)



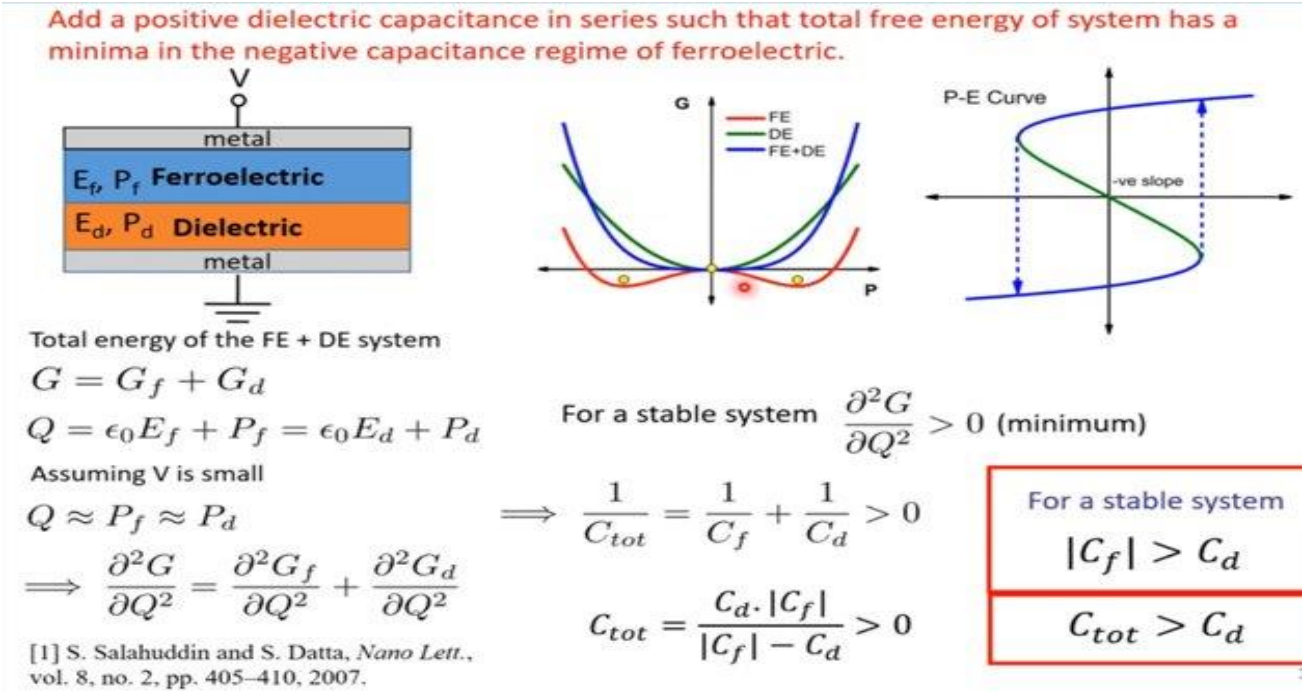
Paraelectric
[A Positive Capacitor]



Ferroelectric
[A Conditionally Negative Capacitor]

A typical capacitor uses paraelectric materials between them and hence can store charges across them. But for ferro electric materials, we end up with P-E characteristics something like a S-shaped curve. Although the part with negative slope is unstable and is hence unachievable in a solo Ferroelectric material and a hysteresis behavior is shown as discussed before. But if we somehow make this negative slope part stable, this characteristic is exact opposite of that of a paraelectric material (left picture). That is, we would have achieved negative capacitance, with behavior the exact opposite of a regular capacitor.

Now, to make this state stable, we always use the Ferroelectric materials in series with paraelectric materials such that negative capacitance is observable.

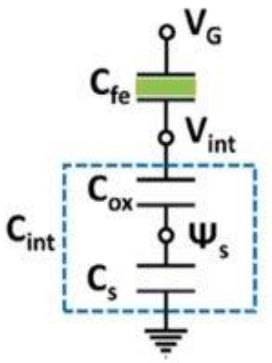


Check the G (free energy) - P (Polarization) curve. For a series combination of FE (Ferroelectric) and Paraelectric (PE) materials, the energy is minimum for zero polarization. Thus, the S-shaped P-E curve is now observable.

The important thing to note here is that the total capacitance C tot is greater than the magnitudes of both the solo capacitances (One from FE and other from PE material).

Negative Capacitance FET (NCFET) and Subthreshold Slope (SS)

MFMIS NCFET Circuit Model



$$C_{fe} = \frac{\partial Q}{\partial V_{fe}}$$

$$SS = \frac{\partial V_G}{\partial \psi_S}\frac{\partial \psi_S}{\partial \log_{10} I_D} = \frac{\partial V_G}{\partial V_{int}}\frac{\partial V_{int}}{\partial \psi_S}\frac{\partial \psi_S}{\partial \log_{10} I_D}$$

$$= \frac{1}{A_V}.\frac{1}{m}.60 \text{ mV/dec}$$

where $m = \frac{\partial \psi_S}{\partial V_{int}} = \left(1 + \frac{C_s}{C_{ox}}\right)^{-1} < 1$

Internal Voltage Gain,

$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}} \quad (C_{fe} < 0)$$

Capacitance matching between $|C_{fe}|$ and C_{int} increases the gain.

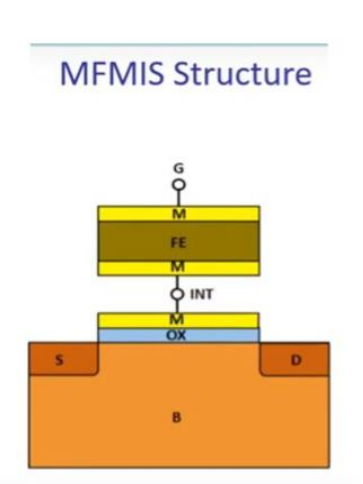
For SS < 60 mV/dec

$$A_V > \frac{1}{m}$$

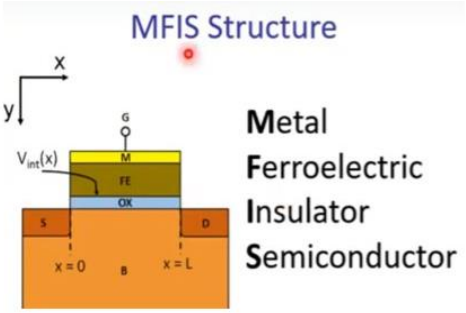
Revisiting the Subthreshold Slope, we now see that when C (FE) is connected in series with C (int) (which is the typical representation of a MOS capacitor), we see that C (total) is greater than C (int) itself. Thus, more charge can be stored for less voltage now. We can safely say that V int has been amplified.

Thus, with negative capacitance, with lesser gate voltage, we can still maintain the same on current in the MOSFET. This is a great solution to the problem of heating and high-power consumption at very small MOSFET dimensions.

NCFET Modelling



Metal
Ferroelectric
Metal
Insulator
Semiconductor



Metal
Ferroelectric
Insulator
Semiconductor

The two methods to simulate a NCFET (Negative Capacitance Field Effect Transistor) are MFMIS and MFIS. The MFMIS method (structure) with an additional metal layer in between (which provides an equipotential surface) is very easy to model and simulate because the Ferroelectric MOSFET and the baseline FINFET can be considered two separate circuits and thus can be modelled differently.

MFIS is a rather challenging model to simulate. Due to the varying potential at the Ferroelectric-oxide junction (like the variation in voltage from the source to drain) the baseline FINFET and Ferroelectric MOSFET cannot be considered as separate entities and a new set of equations must be developed to continue with the simulation of MFIS type of structure.

Introduction to Silvaco TCAD

TCAD software is often used to develop and simulate new semiconductor processes and devices because they reduce the cost and time to market these devices.

Silvaco TCAD is one such tool. The structure of a device is approximated by a mesh consisting of many discrete elements. Differential equations relating to electric potential and carrier distributions are applied to each element till the boundary of simulation. Numerical solver is used to find solutions to these equations. The general structure of an atlas program (written inside Silvaco deck build, to simulate devices) is as follows:

Section	Statements
1. Structure Specification	MESH REGION MATERIAL ELECTRODE DOPING
2. Model Specification	CONTACT MODEL
3. Numerical Model Selection	METHOD
4. Solution Specification	SOLVE LOG SAVE
5. Result Analysis	EXTRACT TONYPLOT

To start with Silvaco TCAD, we first simulated a MOSFET model. The code for the same is shown in the following images. Attached to them are the results after running the program. Notice carefully that the code for the simulation follows the general structure mentioned above.

```
go atlas
TITLE WORKSHOP mos simul

mesh space.mult=1.0

x.mesh loc=0 spacing = 0.25
x.mesh loc=1 spacing = 0.25
x.mesh loc=10 spacing = 0.25
x.mesh loc=11 spacing = 0.25

y.mesh loc=-0.08 spacing = 0.01
y.mesh loc=0 spacing = 0.01
y.mesh loc=0.5 spacing = 0.01
y.mesh loc=0.6 spacing = 0.01

#save outfile=NMOS1.str
#tonyplot
#quit

region  num=1 x.min=0 x.max=11 y.min=-0.08 y.max=0 material= oxide
region  num=2 x.min=2 x.max=8 y.min=-0.07 y.max=-0.06 material= poly
region  num=3 x.min=0 x.max=11 y.min=0 y.max=0.5 material= silicon
region  num=4 x.min=4 x.max=5 y.min=-0.08 y.max=-0.07 material= aluminum
region  num=5 x.min=0.25 x.max=0.5 y.min=-0.08 y.max=0.01 material= aluminum
region  num=6 x.min=10.5 x.max=10.75 y.min=-0.08 y.max=0.01 material= aluminum
region  num=7 x.min=0.0 x.max=11 y.min=0.5 y.max=0.6 material= aluminum

electrode x.min=4 x.max=5 y.min=-0.08 y.max =-0.07 name=gate
electrode x.min=0.25 x.max=0.5 y.min=-0.08 y.max =0.01 name=source
electrode x.min=10.5 x.max=10.75 y.min=-0.08 y.max =0.01 name=drain
electrode x.min=0.0 x.max=11 y.min=0.5 y.max =0.6 name=substrate

doping uniform conc=1e21 n.type reg=2
doping uniform conc=1e17 p.type reg=3
doping uniform conc=1e19 n.type reg=3 x.min=0 x.max=2 y.min=0 y.max=0.3
doping uniform conc=1e19 n.type reg=3 x.min=8 x.max=11 y.min=0 y.max=0.3
#save outfile=NMOS1.str
```

```
#tonyplot

contact name=gate workfunction=0
contact name=substrate workfunction=0
contact name=source workfunction=0
contact name=drain workfunction=0

models fermi cvt consrh bgn
method gummel newton

solve init
solve vdrain=0.005
solve vdrain=0.05
solve vdrain=0.5
solve vdrain=1
solve vdrain=1.5
solve vdrain=2
solve vdrain=2.5
solve vdrain=3

solve vsubstrate=0 name=substrate

log outfile=NMOSfin.log
save outfile=NMOSfin.str

solve vgate=0 vstep=0.025 vfinal=5 name=gate

tonyplot
quit
```

Fig. The code for MOSFET simulation.

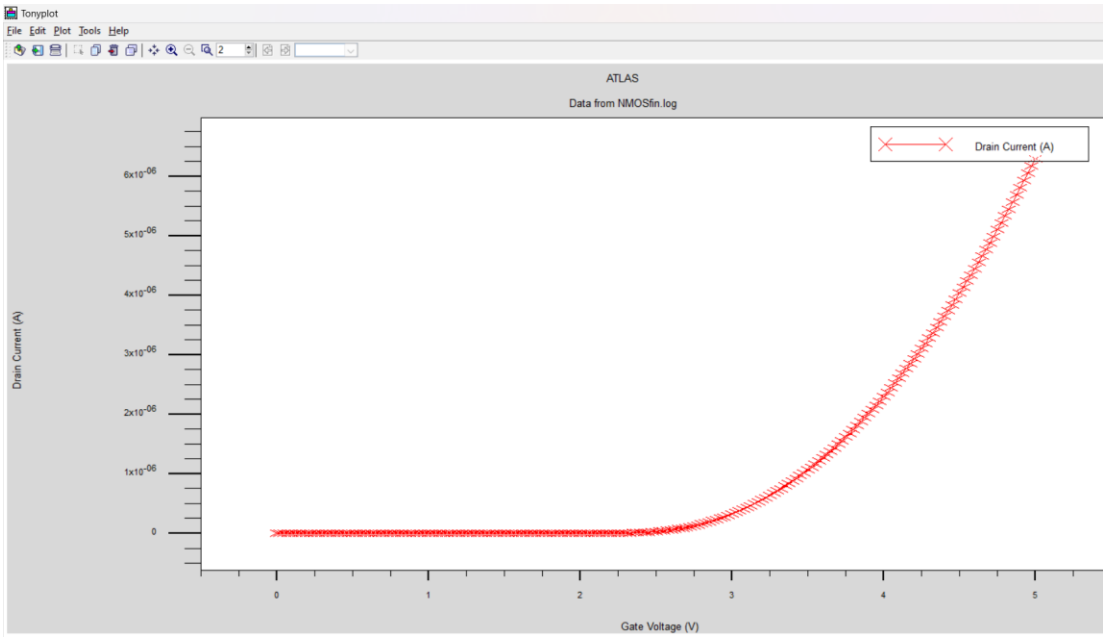


Fig. Input characteristics of a MOSFET

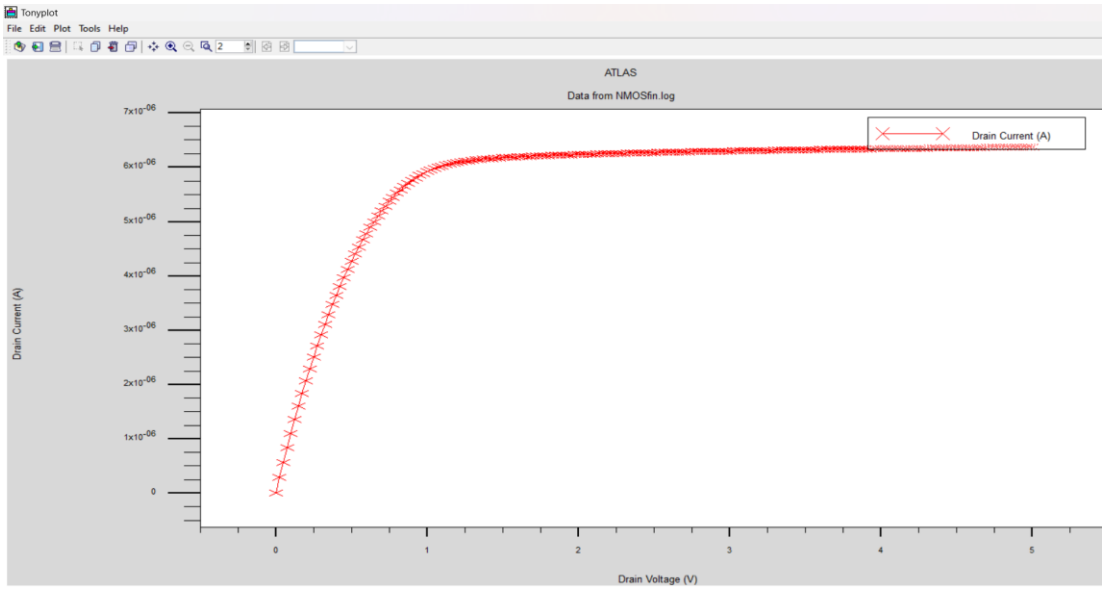


Fig. Transfer characteristics of a MOSFET

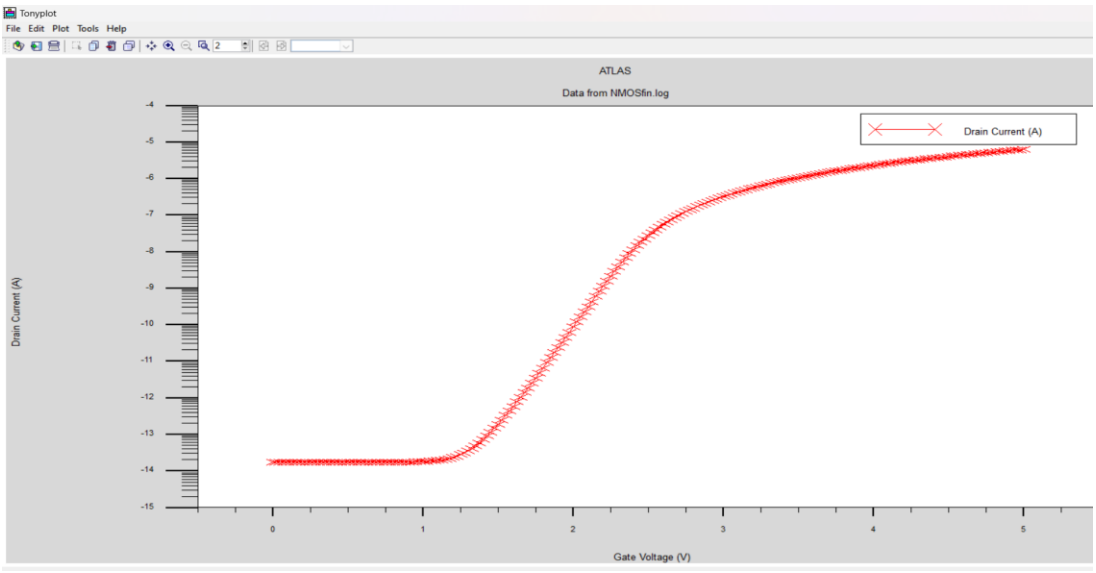


Fig. Log (I_d) vs Vgs graph to extract subthreshold swing.

```
# extract the device parameter SubVt...
extract init inf="moslex03_1.log"
extract name="nsubvt" 1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))
tonyplot moslex03_1.log -set moslex03_1_log.set

quit
```

Fig. Statement to extract the SS of a MOSFET

Variables history

gateox	155.558795232627	(# 84)
nxj	0.176352390119392	(# 87)
n1dvt	0.663102495004693	(# 89)
sheet cond v bias	9.88131291682493e-324	(# 92)
n++ sheet rho	31.0221150810526	(# 94)
ldd sheet rho	2170.56611555275	(# 96)
chan surf conc	3.68892732955156e+16	(# 98)
nsubvt	0.0911873127096014	(# 141)

Fig. MOSFET SS (nsubvt) extracted.

Variables history

nsubvt	0.149532107776098	(# 64)

Fig. Simulation with different conditions.

NCFET Simulations

$$V_{fe} = t_{fe}(2\alpha Q + 4\beta Q^3 + 6\gamma Q^5)$$

$$C_{fe} = \frac{\partial Q}{\partial V_{fe}} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2 + 30\gamma Q^4)}$$

Before getting started with the simulations, the one thing we should discuss is capacitive matching. According to the Landau model (theory) discussed before, the following equations are derived for the capacitance because of ferro electric materials.

It is easy to notice that as t_{fe} increases, C_{fe} decreases. The concept of capacitive matching becomes clear when we revisit the subthreshold slope expression again. We want the gain A_v to be large. For this to happen, the denominator should be tending to "zero" for the A_v expression. That is, C_{fe} should nearly be equal to C_{int}. An important thing to note here is that if $C_{int} > C_{fe}$, then that is the region of instability and hysteresis may be obtained for Id Vg curves.

Although increasing the thickness of the Ferroelectric material improves capacitive matching and hence Av and thus leads to better Subthreshold-Slope. For modern devices, the thickness of the ferroelectric material is nearly 1nm (Considering 7nm tech) and should not be increased further. A_v might be compromised for decreasing the size of NCFET. One thing that can be done regarding this is to try different FE materials.

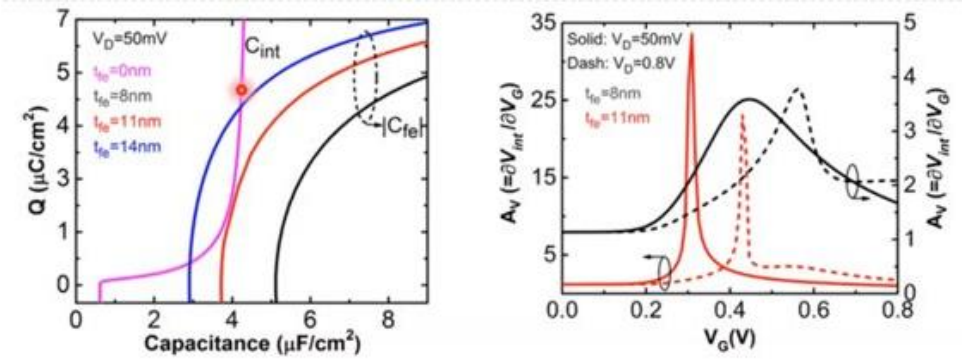
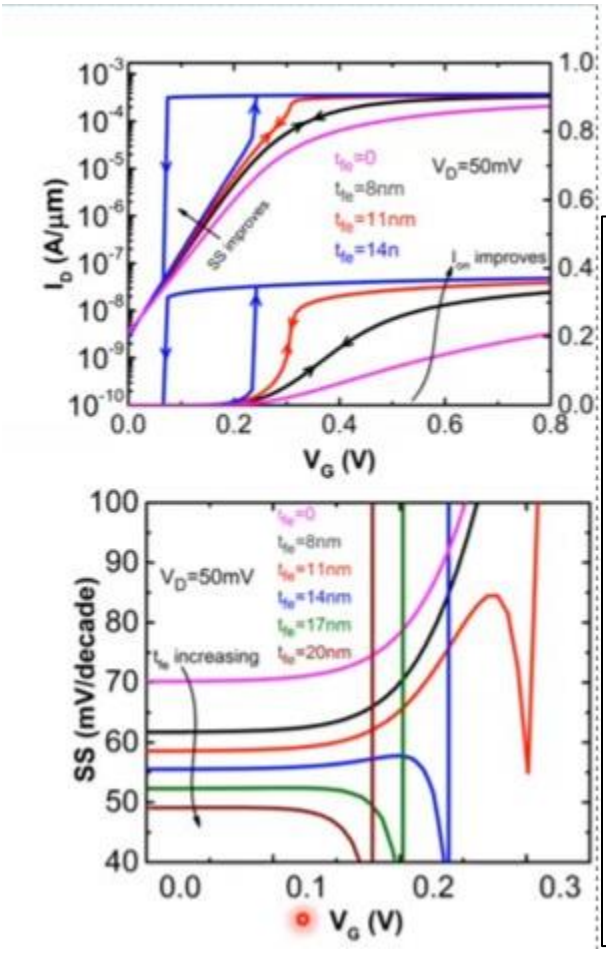


Fig. Capacitance Matching and corresponding increase in A_v.



It is clearly seen that as the thickness of FE layer is increased, the subthreshold swing dramatically improves, along with the Ion characteristics. But increasing the thickness too much leads to instability and hence hysterisis characteristics for both SS and Ion curves.

References

- Technical Report No. UCB/EECS-2020-60 Click here.
- S. Salamin, G. Zervakis, F. Klemme, H. Kattan, Y. S. Chauhan, J. Henkel, and H. Amrouch, "Impact of NCFET Technology on Eliminating the Cooling Cost and Boosting the Efficiency of Google TPU", IEEE Transactions on Computers, 2022
- Negative capacitance in a ferroelectric capacitor Asif Islam Khan1, Korok Chatterjee1, BrianWang1, Steven Drapcho2, Long You1, Claudy Serrao1, Saidur Rahman Bakaul1, Ramamoorthy Ramesh2,3,4 and Sayeef Salahuddin1,4 DOI: 10.1038/NMAT4148
- Negative Capacitance Effect in Semiconductor Devices Maxim Ershov, Member, IEEE, H. C. Liu, L. Li, M. Buchanan, Z. R. Wasilewski, and Andrew K. Jonscher IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 45, NO. 10, OCTOBER 1998
- Design of Negative Capacitance Field-Effect Transistor by Ming-Yen Kao
- YouTube 2021 https://www.youtube.com/watch?v=W0uPmCDjDvg&ab_channel=EEE%40ULAB