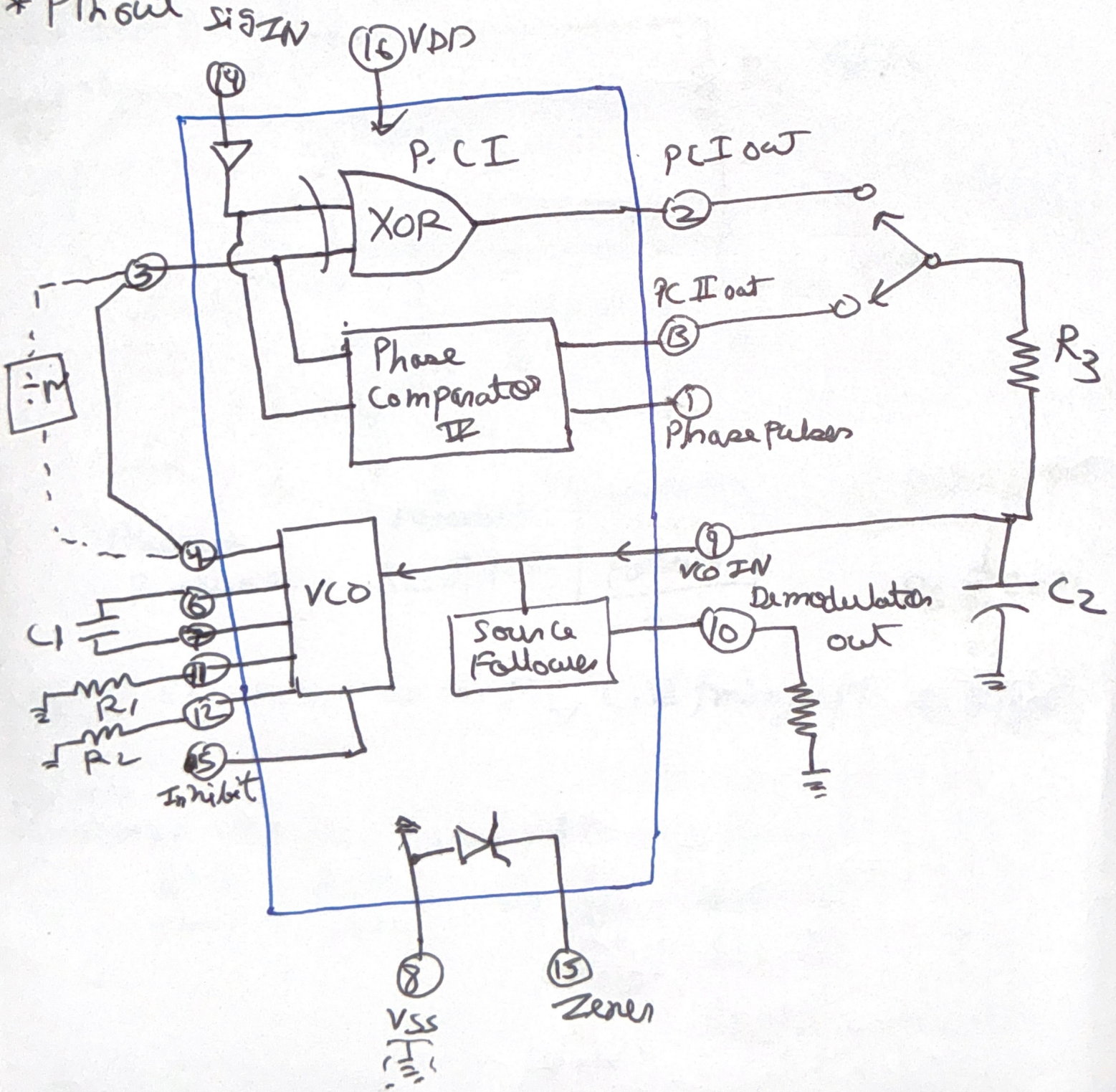
PLL

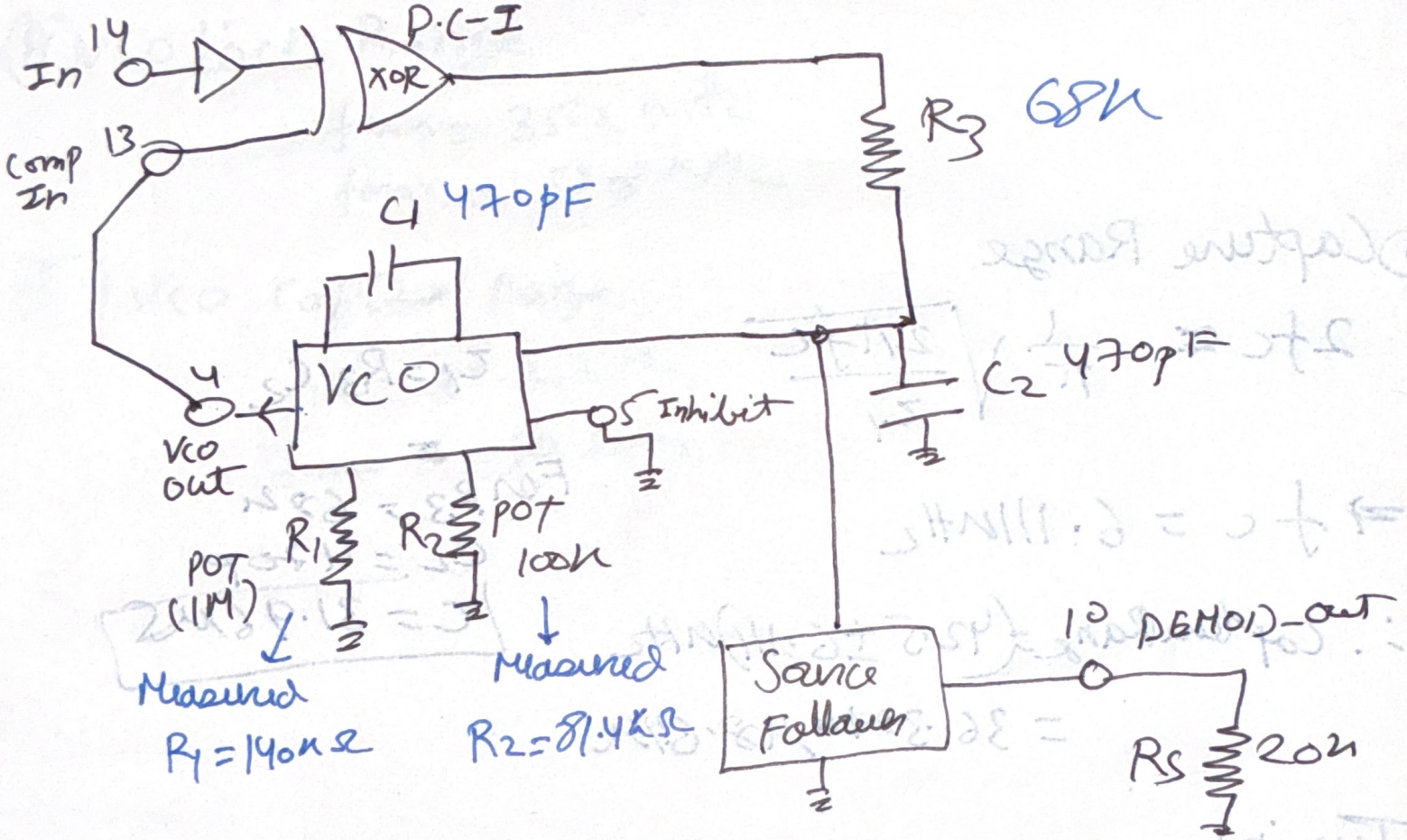
Phase Locked Loop

CD4046 PLL

* Pinout



Our Circuit



Note: C1, chosen as per R_2, C1 Vs fmin graph ⇒ Fig 6

Design

① Choose VCO free Range / VCO full Range

fmin = 35k

fmax = 50k

→ ~~fo = fmax - fmin~~

f_L (Range) $= \frac{50-35}{2} = 7.5k$

f_0 (center) $= \frac{50+35}{2} = 42.5k$

② P.C I is used

③ Capture Range

$$2f_c \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_c}{\tau_1}}$$

$\tau_1 = R_3 C_2$

For $R_3 = 6.2k$

$C_2 = 470p$

$\tau = 31.96\mu s$

$\Rightarrow f_c = 6.111kHz$

$\therefore$ Capture Range $= (42.5 \pm 6.111)kHz$

$= 36.389kHz, 48.611kHz$

Tuning

① Fmin

(a) $V_{control}$ to GND

(b) Adj R2 until V_{coout} (pin 4) = 35 kHz

(c) $\Rightarrow R2 = 84.4k\Omega$

② Fmax

(a) $V_{control}$ to VCC (5V)

(b) Adj R1 until V_{coout} = 50 kHz

(c) $\Rightarrow R1 = 140k\Omega$

Our Measurements

(A) VCO Lock Range

$f_{min} = 35.2$ MHz

$f_{max} = 50.8$ MHz

(B) VCO Capture Range

$f_{min} = 35.2$ MHz

$f_{max} = 50$ MHz