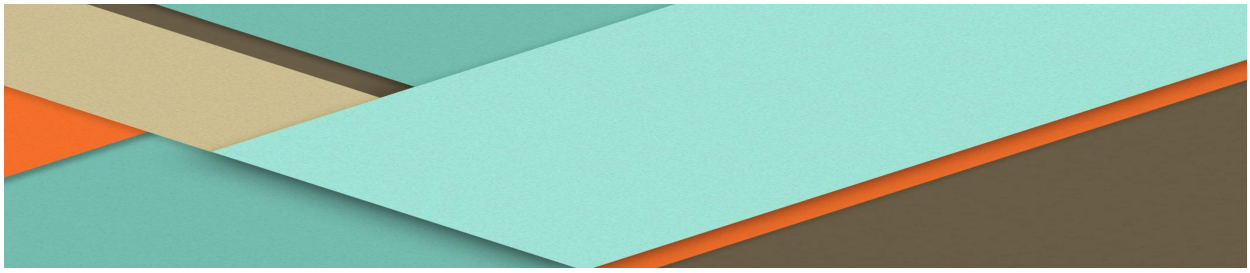

HFE TESTER

Submitted by: Group 32

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CONTENTS

User Requirements & Technical Specifications

Design a microprocessor based transistor hFE tester. The system has to display the h_{FE} value of NPN transistors on a seven segment display.

- The transistor under test is inserted in the socket, and its base is energized with a current I given as:

  $I = V * 10^{-6}$ A

- Emitter of the transistor is grounded.
- Collector is connected to a 1K resistor whose other end is connected to the 5V supply.
- Voltage drop across 1K resistor is related to hFE as:

  $h_{FE} * I * 1000$ = Voltage Drop

- An alarm should be sounded if h_{FE} is less than 20.
- Current I ranges from 1-10 μA with a resolution of 1μA.

Assumptions & Justifications

Justification

- NPN transistor always operates in the active region.
- Since the h_{FE} values to be displayed in the range of 10 to 500, only three seven segment displays are used.
- Polling is done to wait for EOC signal to become high after ADC completes conversion.

Formula Justification :-

Vin : Voltage given to DI

new_Vin : Voltage after passing Vin to DAC

Vout : Voltage at collector terminal

new_Vout : Voltage obtained by passing Vout from ADC

$I = Vin * 10^{-6}$

$I * h_{FE} * 1000 = (5 - Vout)$

[5 - Vout is done because we need difference across the 1000 ohm resistor, and as it was connected to 5V DC Voltage we need to subtract it from 5 to get voltage difference across that resistor]

new_Vin = Vin * 25.6/256

[Applied 25.6 V into Vref+ and 0V to V_{ref-} of DAC as 256 V in V_{ref+} might be a very voltage value to physically manage and we compensated it into below mentioned VCCS]

$I = (Vin/10) * 10^{-5}$

$I= new\_Vin * 10^{-5}$

[The Transconductance of VCCS is set to 10^{-5} so when new_Vin is applied across it, then it gives current as the above mentioned formula]

new_Vout = Vout * 256/5

[V_{ref+} = 5V for ADC]

[In asm file, the values of Vin and new_Vout are present as they both were digital in nature]

$I * h_{FE} * 1000 = (5 - Vout)$

$h_{FE} = (5 - Vout) *1000/Vin$

$h_{FE} = (256- new\_Vout) * 20 / Vin$

Assumptions

- This system is designed only for integral values of h_{FE}.

Components used with Justification Wherever Required

- 8086 - Microprocessor
- 8253 - To generate the clock signal
- 8284 - 8086 Clock & pClock Signal Generator
- 2N2369 - NPN Switching Transistor
- Generic NPN Bipolar transistor - Used to operate buzzer
- Optocoupler NPN - Used in buzzer implementation
- 1K Ohm Resistor - Connected to the collector terminal of the transistor
- VCCS - Linear voltage controlled current source (the device DI)
- 8255A - (2 Nos.) For interfacing with ADC and 7447
- 2716 - (4 Nos.) Smallest ROM chip available is 2K and we need odd and even bank.
- 6116 - (2 Nos.) Smallest RAM chip available is 2K and we need odd and even bank. We need RAM for stack and temporary storage of data
- ADC0808 - For converting analog voltage drop across 1K resistor into digital value.
- DAC_8 - To give analog input voltage to the NPN transistor.
- 74LS373
- 74LS245
- Common Anode Seven Segment Display - (3 Nos.)
- 7447 - (3 Nos.) BCD to Common Anode 7 Segment Converter
- 74LS138 - 1 decoder
- Required Gates
- Buzzer
- Optocoupler-npn
- NPN -
- Switch

Address Map

Memory Map

ROM1: 00000H - 00FFFH → (2 ROM chips each of size 2K) ⇒ 4K

RAM1: 01000H - 01FFFH → (2 RAM chips each of size 2K) ⇒ 4K

ROM2: FF000H - FFFFFH → (2 ROM chips each of size 2K) ⇒ 4K

I/O Map

- 1st 8255: 00H - 06H

  I/O Organization:

  Port A - 00H → O/P

  Port B - 02H → I/P

  Port C Lower - 04H → O/P

  Port C Upper - 04H → O/P

  CREG - 06H

- 2nd 8255: 08H - 0EH

  I/O Organization:

  Port A - 08H → O/P

  Port B - 0AH → O/P

  Port C Lower - 0CH → O/P

  Port C Upper - 0CH → O/P

  CREG - 0EH

Control Word

For 1st 8255A : 10000010B

- Port A :- Output from port A is fed as input voltage to DAC
- Port A is used for generating voltage(V) across the NPN transistor
- Port B :- Input V_0 from ADC
- Port C :- PC_0-PC_3 are used for ADC control signals(ALE, SOC, OE, EOC),

  PC_4 - LE of DAC, PC_5 - Used for output signal to buzzer

For 2nd 8255 : 10000000B

- Port A :- PA_0-PA_3 used as inputs to 7447(1) to output 1st digit
- Port B :- PB_0-PB_3 used as inputs to 7447(2) to output 2nd digit
- Port C :- PC_0-PC_3 used as inputs to 7447(3) to output 3rd digit

  PC_7 - Used as input from switch

Design

Complete design shown. (attached)

Flow Chart

Main Program