

# Microprocessor and Computer Architecture

UE20CS252

4th Semester, Academic Year 2021-22

Date:07-02-2022

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Week# \_\_\_\_4\_\_\_\_ Program Number: \_\_\_\_1\_\_\_\_

Title of the Program

**Write a program in ARM7TDMI-ISA to find GCD of two numbers.**

**a. Assume operands to be in the CPU registers**

**1. ARM Assembly Code(1)**

```
.TEXT  
MOV R0,#9  
MOV R1,#27
```

```
WHILE:  
CMP R0,R1  
BEQ L1  
BGT L2  
B L3
```

```
L1:  
MOV R3,R0  
SWI 0X011  
B L4
```

```
L2:  
SUB R0,R1  
B WHILE
```

```
L3:  
SUB R1,R0  
B WHILE
```

```
L4:  
.END
```

## **2. Output Screen Shot (1)**

File View Cache Debug Watch Help

RegistersView ✕ CodeView

General Purpose Floating Point

Hexadecimal  
Unsigned Decimal  
Signed Decimal

R0 : 00000009  
R1 : 00000009  
R2 : 00000000  
R3 : 00000009  
R4 : 00000000  
R5 : 00000000  
R6 : 00000000  
R7 : 00000000  
R8 : 00000000  
R9 : 00000000  
R10 (s1) : 00000000  
R11 (fp) : 00000000  
R12 (ip) : 00000000  
R13 (sp) : 00011400  
R14 (lr) : 00000000  
R15 (pc) : 00011400

-----  
CPSR Register  
Negative (N) : 0  
Zero (Z) : 1  
Carry (C) : 1  
Overflow (V) : 0  
IRQ Disable: 1  
FIQ Disable: 1  
Thumb (T) : 0  
CPU Mode : System  
-----  
0x600000df

1a.o

```
.TEXT
00001000:E3A00009  MOV R0,#9
00001004:E3A0101B  MOV R1,#27

      WHILE:
00001008:E1500001  CMP R0,R1
0000100C:0A000001  BEQ L1
00001010:CA000003  BGT L2
00001014:EA000004  B L3

      L1:
00001018:E1A03000  MOV R3,R0
0000101C:EF000011  SWI 0X011
00001020:EA000003  B L4

      L2:
00001024:E0400001  SUB R0,R1
00001028:EAF000F6  B WHILE

      L3:
0000102C:E0411000  SUB R1,R0
00001030:EAF000F4  B WHILE

      L4:
      .END
```

### 3. Output Table (1)

R0	:00000009
R1	:00000009
R2	:00000000
R3	:00000009
R4	:00000000
R5	:00000000
R6	:00000000
R7	:00000000
R8	:00000000
R9	:00000000
R10 (sl)	:00000000
R11 (fp)	:00000000
R12 (ip)	:00000000
R13 (sp)	:00011400
R14 (lr)	:00000000
R15 (pc)	:00011400
-----	
CPSR Register	
Negative (N)	:0
Zero (Z)	:1
Carry (C)	:1
Overflow (V)	:0
IRQ Disable	:1
FIQ Disable	:1
Thumb (T)	:0
CPU Mode	:System
-----	
0x600000df	

b. Assume operands in the memory locations.

#### 1. ARM Assembly Code(1)

.DATA

A: .WORD 25,8

.TEXT

LDR R5,=A

ADD R6,R5,#4

LDR R0,[R5]

LDR R1,[R6]

WHILE:

CMP R0,R1

BEQ L1

BGT L2

B L3

L1:

MOV R3,R0

STR R3,[R4]

SWI 0X011

B L4

L2:

SUB R0,R1

B WHILE

L3:

SUB R1,R0

B WHILE

L4:

.END

## 2. Output Screen Shot (1)

ARMSim# - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView CodeView

General Purpose Floating Point

Hexadecimal  
Unsigned Decimal  
Signed Decimal

R0 : 00000001  
R1 : 00000001  
R2 : 00000000  
R3 : 00000001  
R4 : 00000000  
R5 : 00001044  
R6 : 00001048  
R7 : 00000000  
R8 : 00000000  
R9 : 00000000  
R10 (s1) : 00000000  
R11 (fp) : 00000000  
R12 (ip) : 00000000  
R13 (sp) : 00011400  
R14 (lr) : 00000000  
R15 (pc) : 00001024

-----  
CPSR Register  
Negative (N) : 0  
Zero (Z) : 1  
Carry (C) : 1  
Overflow (V) : 0  
IRQ Disable : 1  
FIQ Disable : 1  
Thumb (T) : 0  
CPU Mode : System  
-----  
0x600000df

1b.o

```
.DATA
00001044:00000019      A: .WORD 25,8
:00000008

.TEXT
00001000:E59F5038      LDR R5,=A
00001004:E2856004      ADD R6,R5,#4
00001008:E5950000      LDR R0,[R5]
0000100C:E5961000      LDR R1,[R6]

WHILE:
00001010:E1500001      CMP R0,R1
00001014:0A000001      BEQ L1
00001018:CA000004      BGT L2
0000101C:EA000005      B L3

L1:
00001020:E1A03000      MOV R3,R0
00001024:E5843000      STR R3,[R4]
00001028:EF000011      SWI 0X011
0000102C:EA000003      B L4

L2:
00001030:E0400001      SUB R0,R1
00001034:EAF00005      B WHILE

L3:
00001038:E0411000      SUB R1,R0
0000103C:EAF00003      B WHILE

L4:
00001040:00000000      .END
```

### 3. Output Table (1)

```
R0      :00000001
R1      :00000001
R2      :00000000
R3      :00000001
R4      :00000000
R5      :00001044
R6      :00001048
R7      :00000000
R8      :00000000
R9      :00000000
R10 (s1):00000000
R11 (fp):00000000
R12 (ip):00000000
R13 (sp):00011400
R14 (lr):00000000
R15 (pc):00001024
-----
CPSR Register
Negative (N) :0
Zero (Z)      :1
Carry (C)     :1
Overflow (V)  :0
IRQ Disable:1
FIQ Disable:1
Thumb (T)     :0
CPU Mode      :System
-----
0x600000df
```

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UE20CS252

4th Semester, Academic Year 2021-22

Date:

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Week# \_\_\_\_4\_\_\_\_ Program Number: \_\_\_\_2\_\_\_\_

Title of the Program

**Write a program in ARM7TDMI-ISA to find the sum of N data items at alternate [ odd or even positions] locations in the memory. Store the result in the memory location.**

**a. Use Pre-indexing addressing mode**

**1. ARM Assembly Code(1)**

```
.DATA  
X: .WORD 3,2,4,7  
S: .WORD 0
```

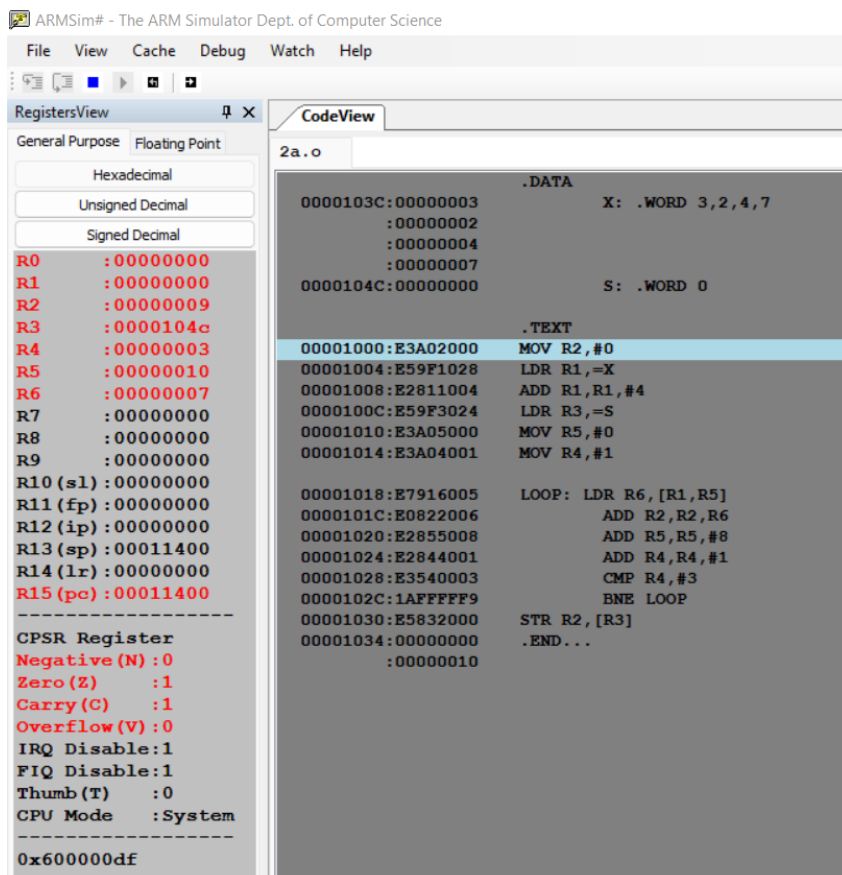
```
.TEXT  
MOV R2,#0  
LDR R1,=X  
ADD R1,R1,#4
```



```
LDR R3,=S
MOV R5,#0
MOV R4,#1
```

```
LOOP: LDR R6,[R1,R5]
ADD R2,R2,R6
ADD R5,R5,#8
ADD R4,R4,#1
CMP R4,#3
BNE LOOP
STR R2,[R3]
.END
```

## 2. Output Screen Shot (1)



### 3. Output Table (1)

```
R0      :00000000
R1      :00000000
R2      :00000009
R3      :0000104c
R4      :00000003
R5      :00000010
R6      :00000007
R7      :00000000
R8      :00000000
R9      :00000000
R10 (sl):00000000
R11 (fp):00000000
R12 (ip):00000000
R13 (sp):00011400
R14 (lr):00000000
R15 (pc):00011400
-----
CPSR Register
Negative (N) :0
Zero (Z)      :1
Carry (C)     :1
Overflow (V)  :0
IRQ Disable:1
FIQ Disable:1
Thumb (T)     :0
CPU Mode      :System
-----
0x600000df
```

#### b. Use Post- Indexing addressing mode

##### 1. ARM Assembly Code(1)

```
.DATA
X: .WORD 1,3,6,8
S: .WORD 0
```

```
.TEXT
MOV R2,#0
LDR R1,=X
ADD R1,R1,#4
LDR R3,=S
MOV R5,#8
MOV R4,#1

LOOP: LDR R6,[R1],R5
      ADD R2,R2,R6
      ADD R4,R4,#1
      CMP R4,#3
      BNE LOOP
STR R2,[R3]
.END
```

## 2. Output Screen Shot (1)

ARMSim# - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView CodeView

General Purpose Floating Point

Hexadecimal  
Unsigned Decimal  
Signed Decimal

R0 :00000000  
R1 :00000000  
R2 :0000000b  
R3 :00001048  
R4 :00000003  
R5 :00000008  
R6 :00000008  
R7 :00000000  
R8 :00000000  
R9 :00000000  
R10 (s1) :00000000  
R11 (fp) :00000000  
R12 (ip) :00000000  
R13 (sp) :00011400  
R14 (lr) :00000000  
R15 (pc) :00011400

-----  
CPSR Register  
Negative (N) :0  
Zero (Z) :1  
Carry (C) :1  
Overflow (V) :0  
IRQ Disable:1  
FIQ Disable:1  
Thumb (T) :0  
CPU Mode :System  
-----  
0x600000df

2b.o

```
.DATA
00001038:00000001      X: .WORD 1,3,6,8
      :00000003
      :00000006
      :00000008
00001048:00000000      S: .WORD 0

.TEXT
00001000:E3A02000      MOV R2,#0
00001004:E59F1024      LDR R1,=X
00001008:E2811004      ADD R1,R1,#4
0000100C:E59F3020      LDR R3,=S
00001010:E3A05008      MOV R5,#8
00001014:E3A04001      MOV R4,#1

00001018:E6916005      LOOP: LDR R6,[R1],R5
0000101C:E0822006              ADD R2,R2,R6
00001020:E2844001              ADD R4,R4,#1
00001024:E3540003              CMP R4,#3
00001028:1AFFFFFA              BNE LOOP
0000102C:E5832000      STR R2,[R3]
00001030:00000000      .END...
      :00000010
```

### 3. Output Table (1)

```
R0      :00000000
R1      :00000000
R2      :0000000b
R3      :00001048
R4      :00000003
R5      :00000008
R6      :00000008
R7      :00000000
R8      :00000000
R9      :00000000
R10 (sl):00000000
R11 (fp):00000000
R12 (ip):00000000
R13 (sp):00011400
R14 (lr):00000000
R15 (pc):00011400
-----
CPSR Register
Negative (N) :0
Zero (Z)      :1
Carry (C)     :1
Overflow (V)  :0
IRQ Disable:1
FIQ Disable:1
Thumb (T)     :0
CPU Mode      :System
-----
0x600000df
```

### **Disclaimer:**

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:



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Section: D

Date: 07-02-2022