INTERNSHIP REPORT

Project:

Color Mixer using four Single Slope ADCs and four PWM outputs

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ACKNOWLEDGEMENT

I owe my deep gratitude to Prof. Dhananjay V. Gadre, Associate Professor, ECE Division at Netaji Subhas University of Technology, for providing me an opportunity to learn Embedded System Design under him and giving all the support and guidance to complete my project "FPGA Based Color Mixer using single slope ADC" duly. Apart from the technical skills learnt and implemented, he provided an environment aimed at learning, exploring, innovating, making, and spreading knowledge.

I would also like to thank my family for their constant support.

INTRODUCTION:

As the FPGAs are inherently digital devices so we can't sense any analog input using it without any external ADC, so during the internship period I started to design single slope ADCs using external comparator to create analog to digital convertor inside the FPGA, whose basic concept is discussed as follows.

In a single slope ADC, an external comparator's output is connected to the FPGA. The negative input terminal of the comparator is connected to the analog voltage that we would like to measure, and the positive input terminal is connected to a capacitor which is being charged by a constant current source. The voltage of the capacitor increases linearly, $dV/dt = I/C$ and when it matches with the voltage connected at the negative terminal, the output of the comparator goes HIGH, this can be sensed by the FPGA and the ADC value can hence be obtained.

To present the output which is matched with the analog input I decided to use a 3W RGB LED, whose intensity would define the given input analog voltage.

So, at the input we would have four potentiometers to vary the analog voltage and at the output we would connect the RGB LED whose intensity will also be controlled, thus requiring four PWM outputs.

DESCRIPTION:

Facing the user, the board is having four linear rotary potentiometers, one for varying the intensity of red color, second for varying the intensity of green color, third for varying the intensity of blue color and fourth for varying the intensity of the resultant color. At the top of the PCB there is a 3W RGB LED which is used to output the red, green and blue colors. At the center lies the brain of the complete system which is Xilinx Spartan 3AN XC3S50AN FPGA soldered on a breakout board.

Below the FPGA is the circuitry for the clock of the complete system, which is made using Schmitt Trigger oscillator oscillating at 12Mhz.
The project also has a reset switch which can be pressed if the system enters in any faulty condition or state.

About FPGA:

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks. Although one-time programmable (OTP) FPGAs are available, the dominant types are SRAM based which can be reprogrammed as the design evolves.

Some of the key features of the selected FPGA are:

- Xilinx Spartan FPGA - XC3S50AN
- In-system Flash memory of 1 Mb for storing non-volatile data
- 50k gates
- 176 CLBs
- 108 user IO pins
- Can be programmed through JTAG (Joint Test Action Group) protocol

Beginning with Roti, Kapda, Makaan and Internet of our system.

Just as today every human being requires four basic things for his/her survival, similar is the case with the FPGAs. They also require four basic things, which we generally refer to their ecosystem and toolchain.

The four basic requirements for the FPGAs are:

- Power Supply
- System Clock
- Reset, and
- Ability to download program

1. Power Supply

One of the most important sub-part of the embedded system is the power supply. The power supply for the selected IC is divided into four groups, the below table taken from the datasheet shows the required voltage levels.

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	$V_{CCO}+0.5$	V

Figure 1: Power Supply Requirements

Making and testing of the power supply board:

The power supply was designed and soldered on a general purpose PCB for testing using two linear low dropout regulators -

- LM1117 - Fixed 3.3V output
- LM1117 adj - Adjustable output voltage, configured to output 1.25V

The figure below shows the images of the general purpose testing board for the power supply system.

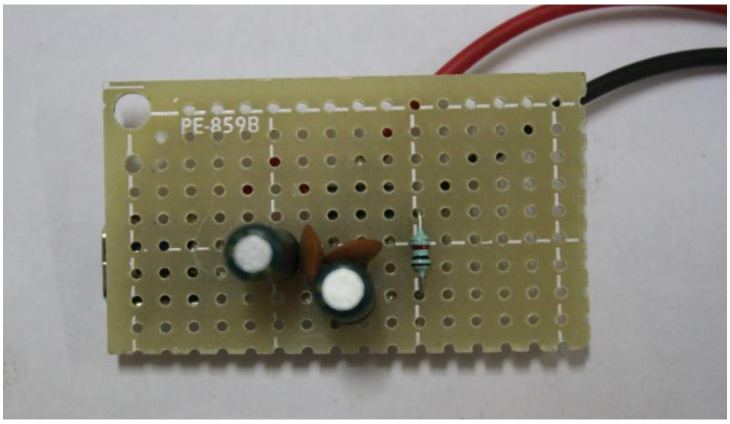


Figure 2 : Power Supply Test Board (Front)

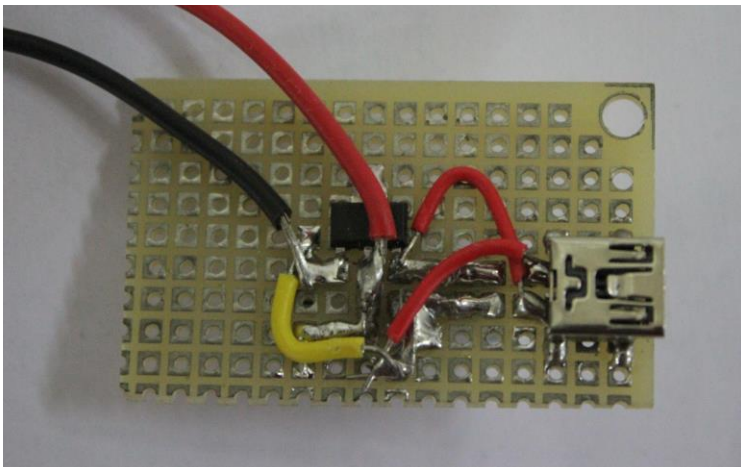


Figure 3: Power Supply Test Board (Bottom)

2. System Clock

The system clock of 12Mhz was designed using an oscillator and schmitt trigger IC 74HC14 and tested on a general purpose board.

The figures below shows the circuit diagram, and the soldered general purpose board for the testing.

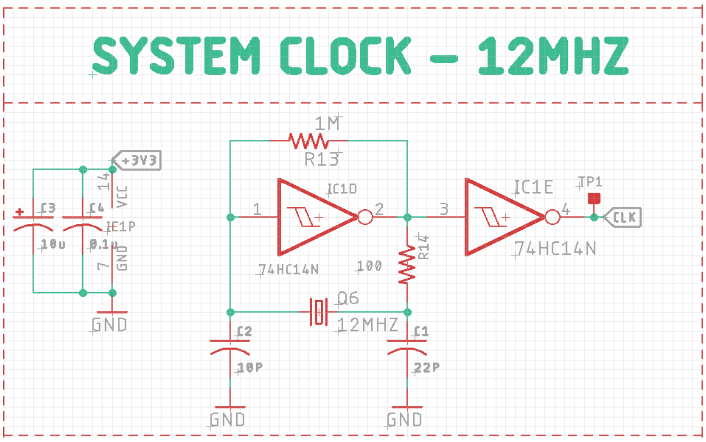


Figure 5 : Circuit Diagram of Clock System

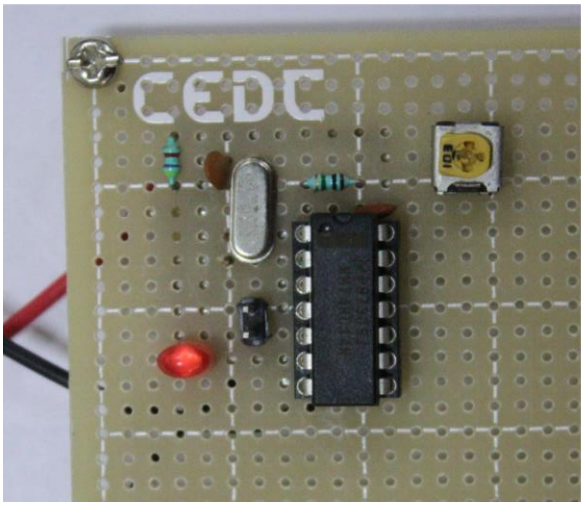


Figure 4: Clock System Test Board

3. Program download Capability

The flash memory of the device can be programmed by the JTAG programmers. A separate PCB was made to test the programming of the device.

The below image shows the JTAG programmer used for programming the FPGA.

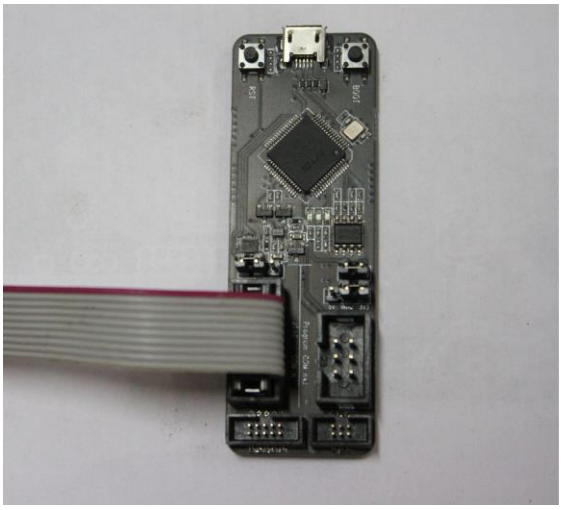


Figure 6: JTAG Programmer

4. Reset

Reset signal is given from a push-button on the final PCB and is incorporated in the state machine to reset the system.

The below image shows the circuit diagram for the reset push-button.

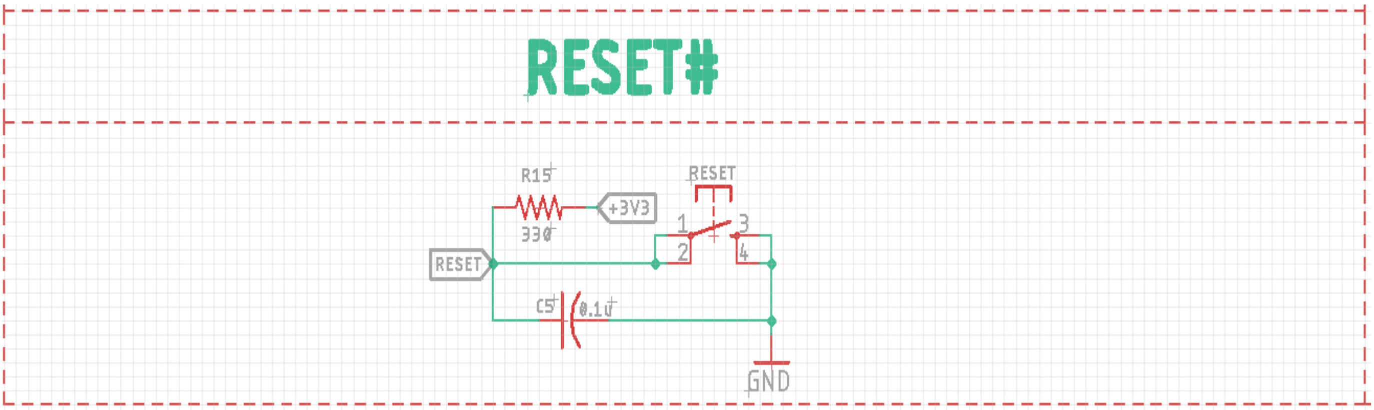


Figure 7: Circuit Diagram Reset Signal

BLOCK DIAGRAM

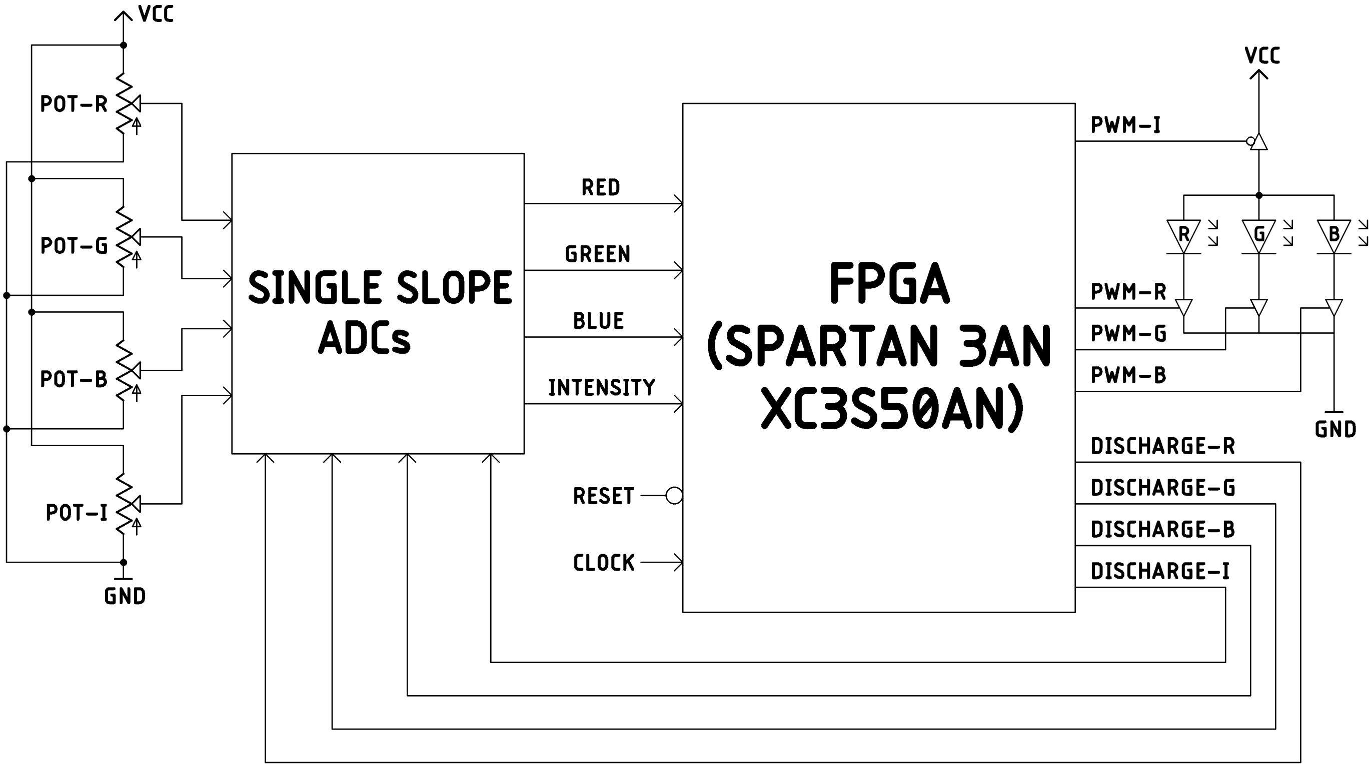


Figure 8: Block Diagram of Complete System

I/O BLOCKS:

1. **Reset switch:** To Reset in any given condition.
2. **3W RGB LED:** To output Red, Green and Blue color.
3. **Single slope ADCs**: Constructed using a comparator, they output signal based on comparison of two signals, one being the voltage of the linearly charged capacitor while other being the voltage from the potentiometer,
4. **Linear Rotary Potentiometers:** To give analog input to the single slope ADCs.

CONTROL AND DATA PATH:

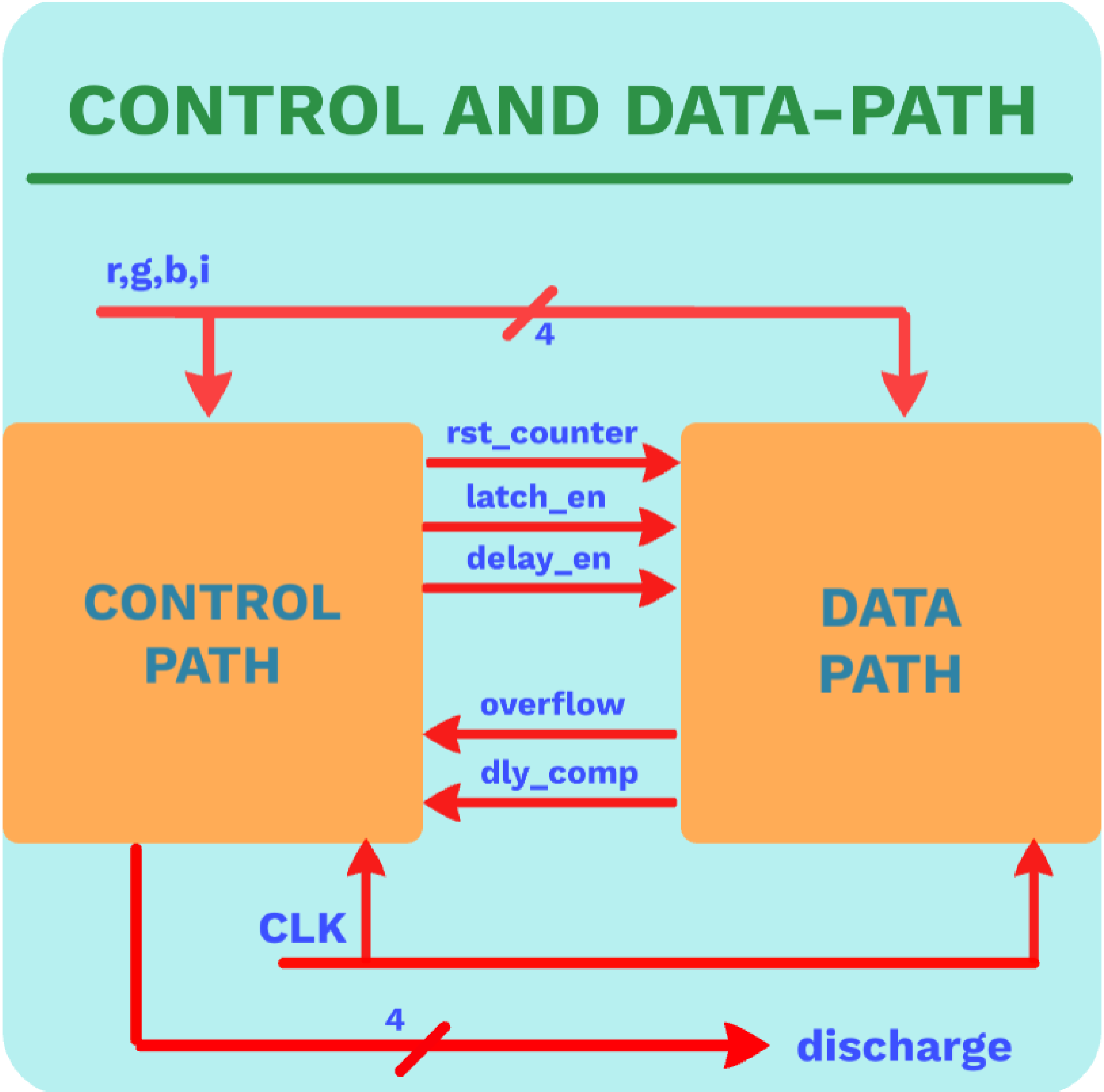


Figure 9: Control and Data Path

CONTROL PATH:

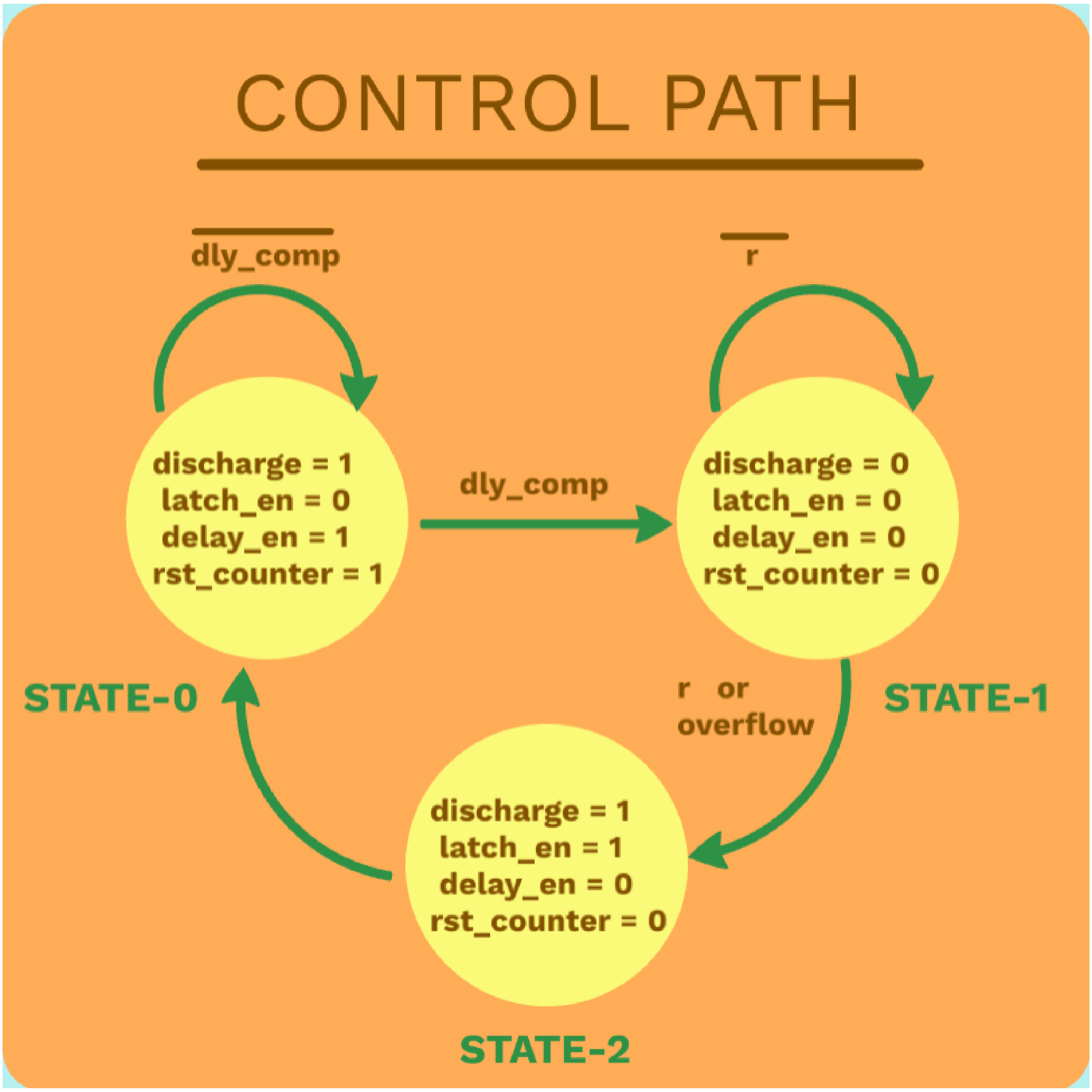


Figure 10: Control Path

ELEMENTS OF DATA PATH:

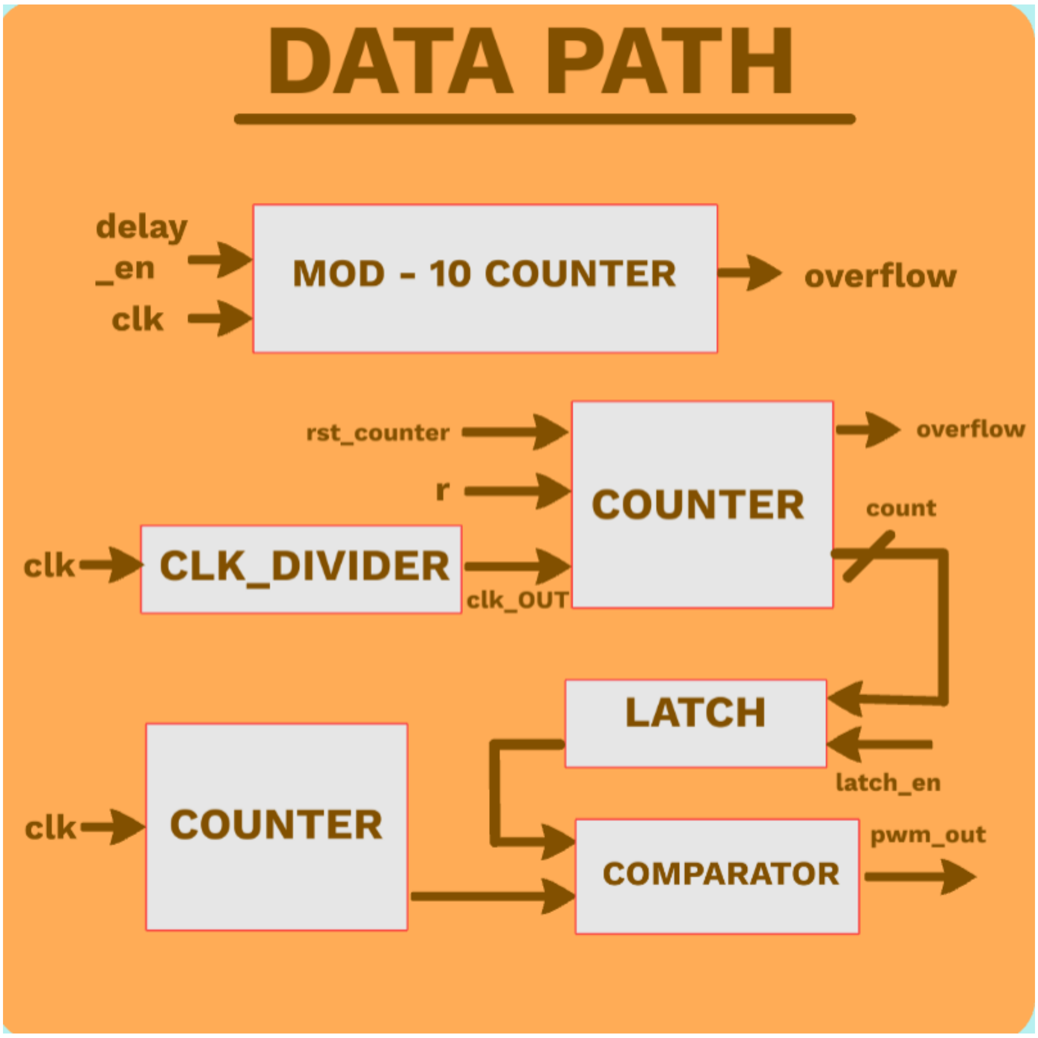


Figure 11: Data Path

1. Mod - 10 Counter: This is used to generate some delay to discharge the capacitor to start the new cycle.

2. 8 bit Counter1: It is used to count until the compare match happens on the external comparator to measure the analog input voltage.

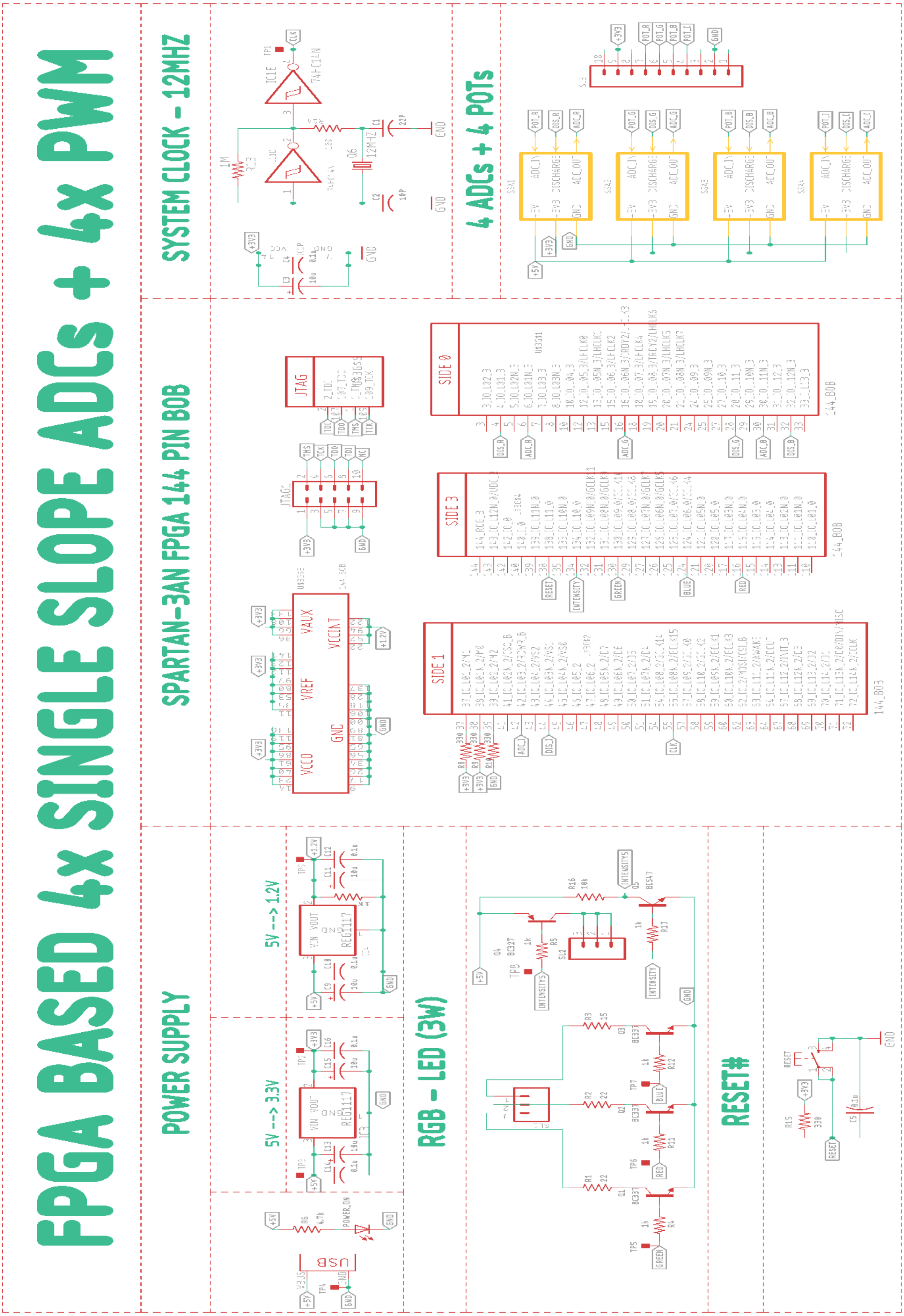
3. Clock Divider: As certain part of the project demands a slower operating clock so formaking a suitably slow clock, clock dividers are required.

4. 8 bit Counter2: This counter is used to generate the PWM output.

5. 8 bit Latch: Latch is used the hold the counter1 value so that it can be cleared for the next cycle.

6. 8 bit Comparator: It is needed to compare the values of the latch and the counter and hence its output would be the PWM signal.

Schematic made using EAGLE:



Board Layout:

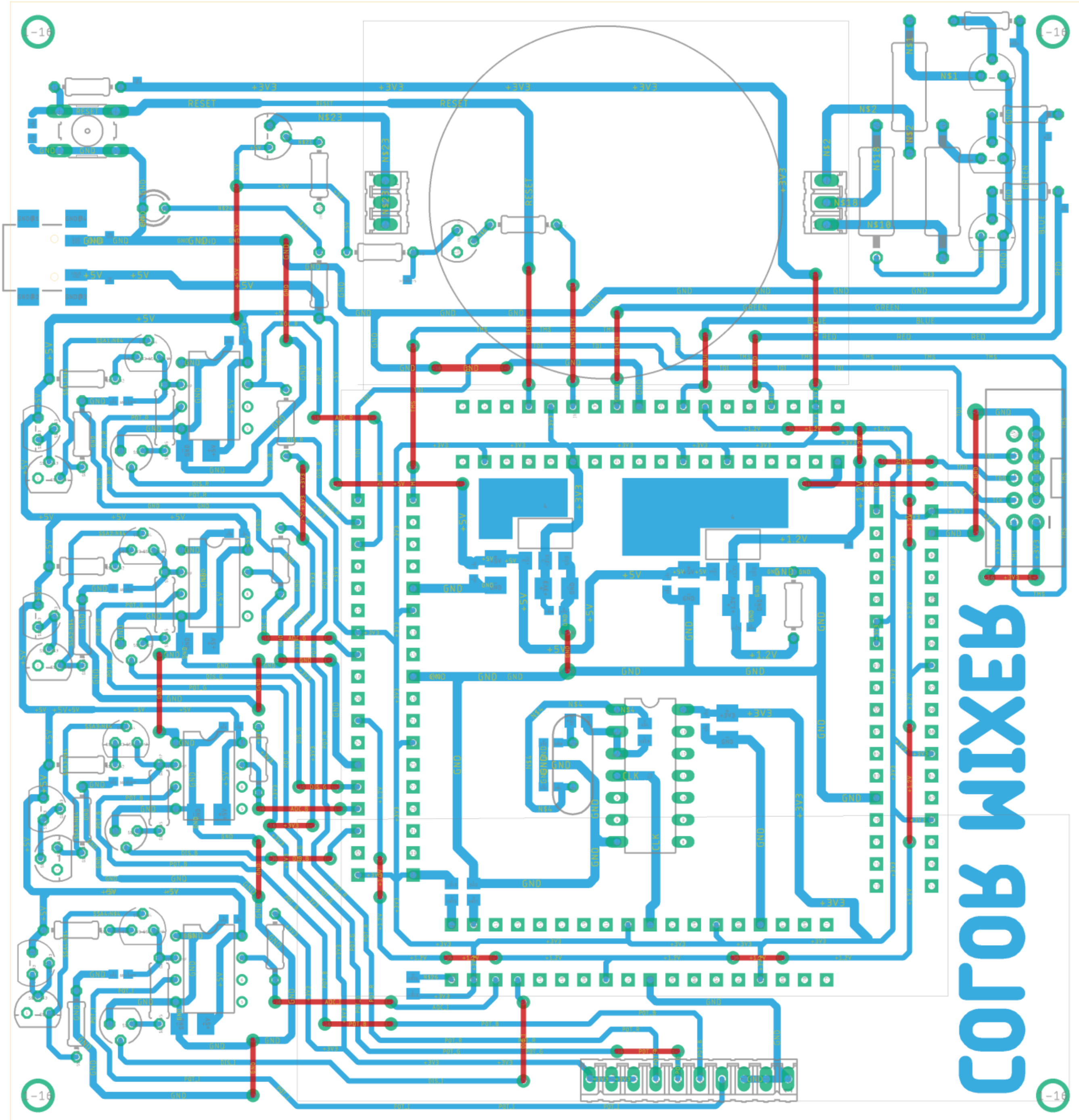


Figure 12: Board Layout

FINAL PCB:

1. Fabricated:

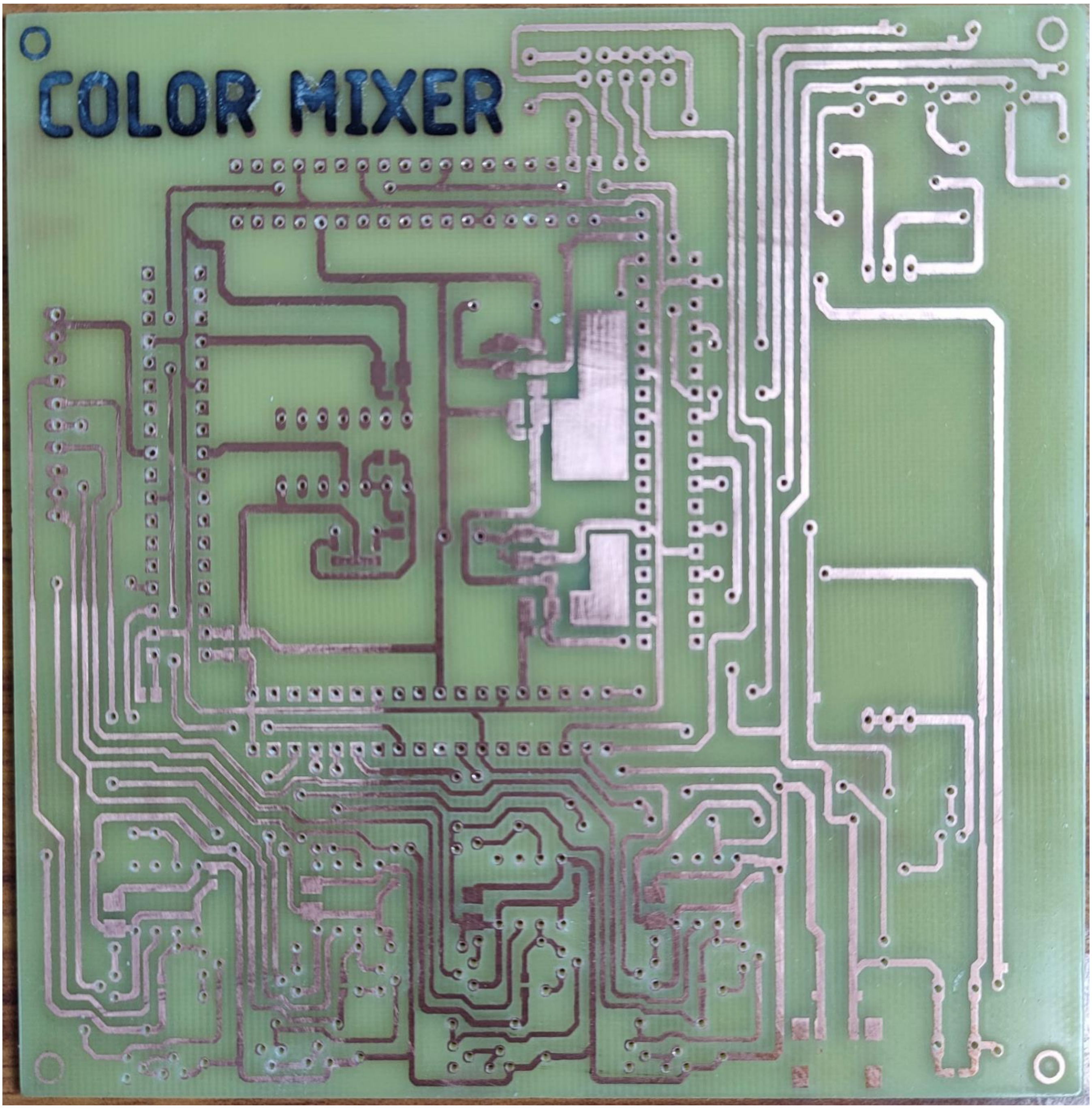


Figure 13: Fabricated PCB

2. Complete PCB with components soldered:

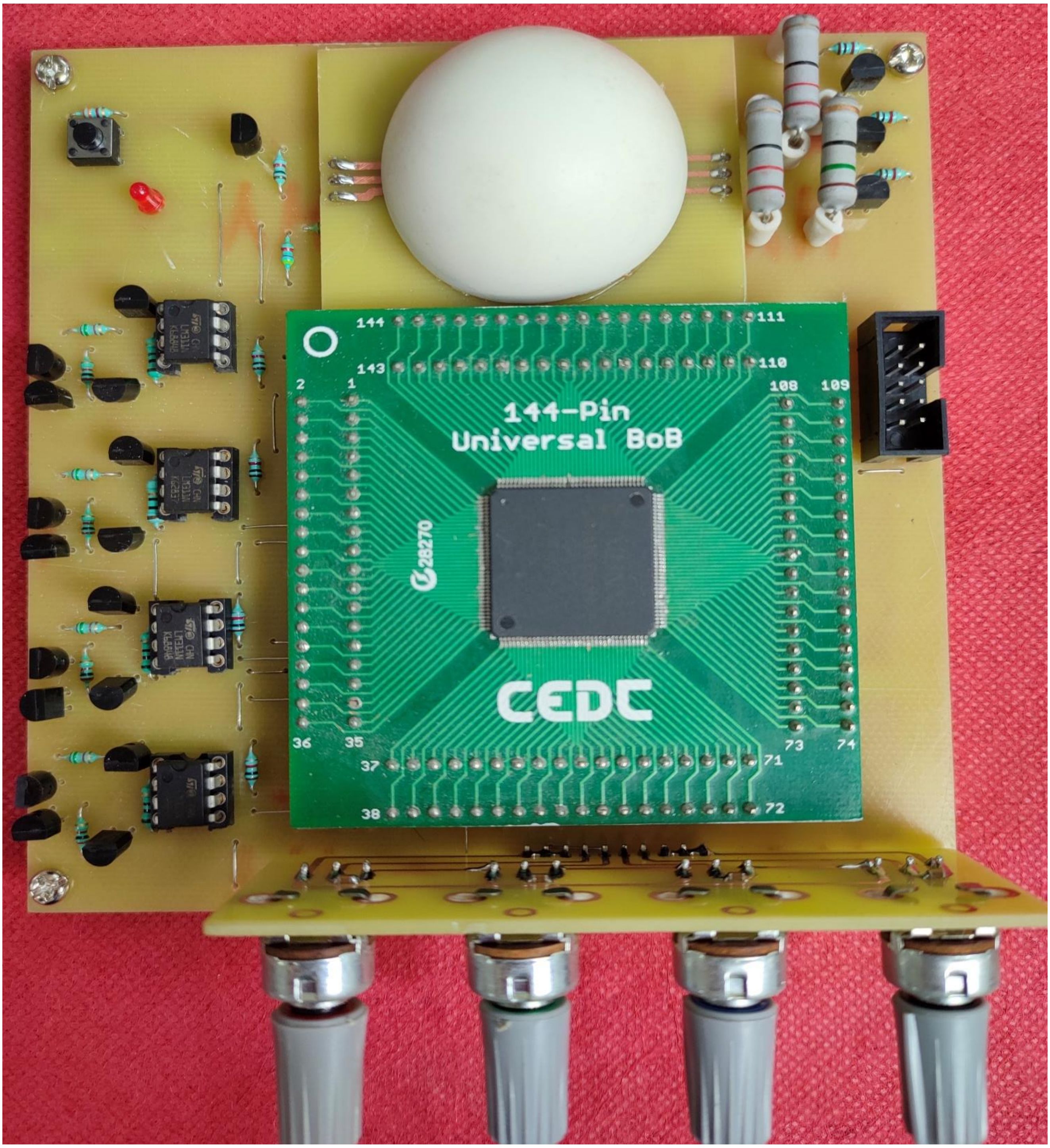


Figure 14: Completely Soldered PCB

References:

- Spartan 3AN XC3S50AN, Datasheet
- LM311, Datasheet
- REG1117, Datasheet
- http://www.circuitstoday.com/understanding-fpga-and-cpld
- https://nptel.ac.in/courses/106/105/106105165/
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