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The Design of High Speed UART

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Abstract-**Universal asynchronous receiver transmitter, abbreviated UART is a integrated circuit used for serial communications over a computer or peripheral device serial port. UARTs are now commonly included in microcontrollers. The universal designation indicates that the data format and transmission speeds are configurable and that the actual electric signaling levels and methods (such as differential signaling etc.) typically are handled by a special driver circuit external to the UART. Baud rate of 20Mbps using clock of 20MHz is used. FIFO (First-In-First Out) is used to store data temporarily during high speed transmission to get synchronization. The design is synthesized in Verilog HDL and reliability of the Verilog HDL implementation of UART is verified by simulated waveforms. We are using Cadence tool for simulation and synthesis.**

Keywords: **UART, FIFO, High speed, Transmitter, Receiver, Baud Rate Generator.**

I. INTRODUCTION

Universal Asynchronous Receiver Transmitter is used to transmit and receive data through a serial port on computer. It converts the data parallel to serial to transmit from computer at transmitter end and converts the serial data received at receiver end into parallel without loss of data at high speed. UART incorporates the transmitter, receiver, baud rate generator and FIFO. Baud rate generator is used to provide clock to transmitter, receiver and FIFO. First-In-First-Out (FIFO) is used at both transmitter and receiver end to store high speed incoming data temporarily to prevent data loss.

To design a circuit at gate level is tedious and consumes large amount of time because the integrated circuit technology is becoming more and more complex day by day. Hence the use of hardware description language such as Verilog HDL and VHDL is becoming popular because it makes it easy to design a circuit of any complexity. So in this paper we are using Verilog HDL to design the circuit. Verilog HDL makes it easy to understand and read the design, simulate, & synthesize the design.

UART is commonly used in conjunction with communication standards such as EIA RS-232, RS-422 or RS-485. The universal designation indicates that the data format and transmission speeds are configurable and that the actual electric signaling levels and methods (such as differential signaling etc.) typically are handled by a special driver circuit external to the UART.

UART requires Baud rate Generator. Baud is a measurement of transmission speed. Traditionally, a Baud Rate represents the number of bits that are actually being sent over the media, not the amount of data that is actually moved from one DTE device to the other. The Baud count includes the overhead bits Start, Stop and Parity that are generated by the sending UART and removed by the receiving UART.

II. UART DATA TRANSMISSION

UART uses Asynchronous serial communication.

Transmission begins with the bit '1' followed by a start bit '0' followed by 8-bit data, followed by parity bit and at last a stop bit '1'. The start signal indicates to the receiver that transmission of data is about to start. Parity bit is used for error detection. Stop bit is used to indicate the end of transmission to the receiver. Each character is placed in between start and stop bits, this is called framing. The start bit is always low and stop bit is always high The LSB of the data word is transmitted first. UART data format and its direction of transmission are shown in fig.1

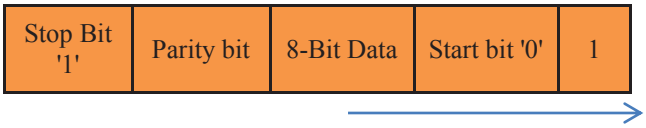

Fig: 1 The UART data format

Suppose the transmitted 8-bit data is 00000101 then the corresponding UART data format is 1000000101.

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III. PROPOSED ARCHITECTURE

The proposed architecture of UART is shown in fig.2. Baud rate generator provides read clock and write clock to both FIFO and a common clock signal to both transmitter and receiver. FIFO depth is calculated as:

FIFO size (depth) = Data frame size – (read frequency/write frequency) * Data frame size.

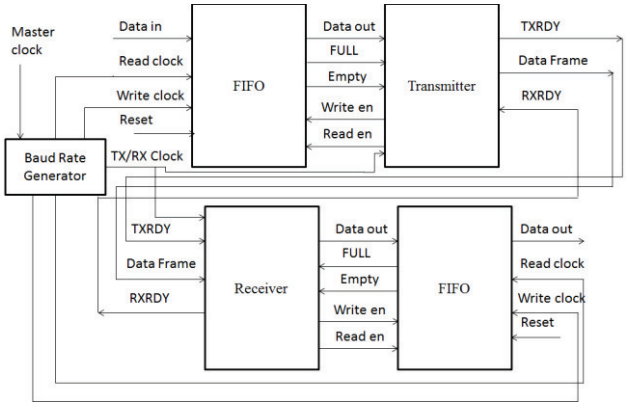

Fig. 2 Proposed architecture of UART

Here TXRDY stands for transmitter ready to transmit and RXRDY stands for receiver ready to receive.
The proposed architecture of baud rate generator is shown in fig3.

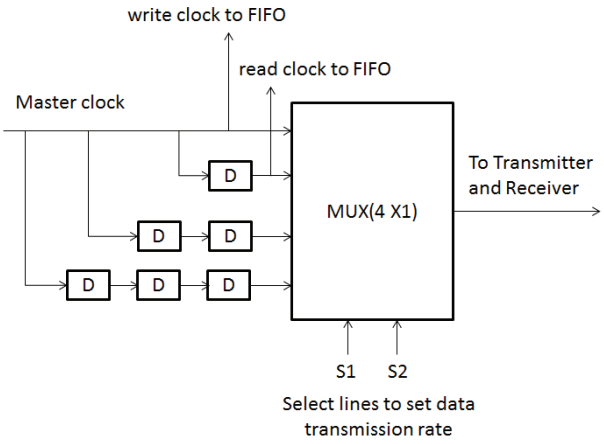

Fig. 3 Proposed architecture of Baud Rate Generator (BGR)

Here D stands for D flip-flop. In our design data frame size is 12.Write and read frequencies are 20MHz and 10MHz respectively.

Thus the FIFO size in our design is:

FIFO size = 12 – (10/20) *12 = 6.

FIFO is implemented as a queue structure. It has a fixed length. If FIFO is empty or is not filled fully then only data can be written in it. If FIFO is full, it sends a signal "FULL" to the transmitter and receiver at respective end. If it is empty, then it sends signal "Empty" to the transmitter and receiver at respective end. FIFO is used for synchronization purpose between transmitter and CPU at one end and also between receiver and CPU at other end to prevent the loss of data if speed of CPU doesn't match with the transmission between transmitter and receiver.

IV. SIMULATION

The proposed architecture is implemented in Verilog HDL. The simulated waveform is shown in fig4.If receiver clock and receive ready signals are making transition to logic high the data is captured by receiver which stored in FIF and finally to CPU or data bus.

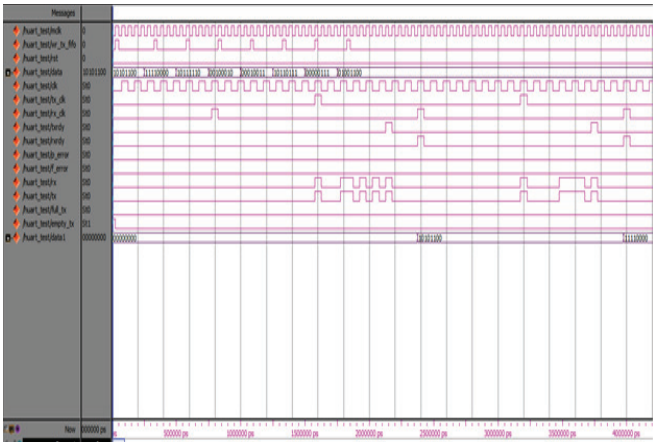

Fig4: UART output simulated waveform

V. CONCLUSION

A UART is the microchip with programming that controls a computer's interface to its attached serial devices. The UART is successfully implemented by using Verilog HDL. Compilation, elaboration, simulation and synthesis are performed by using Cadence Tool. The high speed serial data transmits at the rate of 20Mbps by using 20MHz master clock rate. The UART speed is limited only by transmission media between transmitter and receiver and also by CPU speed. The modification in architecture according to speed is required only in baud rate generator.

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VI. REFERENCE

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