Haixin Yu

me@hai-hs.in · +86 151-0113-5718 · Hai-Hsin · blog.hai-hs.in

Education

Beijing University of Posts and Telecommunications, Master of Computer Technology 2021 – 2024

- Major: Computer Technology, *School of Computer Science*

Beijing University of Posts and Telecommunications, Bachelor's Degree 2017 – 2021

- Major: Computer Science and Technology , *School of Computer Science*, GPA: 3.50

Work Experience

Alibaba Cloud 05/2023 – 09/2023

Virtualization Engineer Intern, *X-Dragon Team, ECS*

- Participated in DragonFly Hypervisor development for Alibaba Cloud ECS on ARM64 architecture.
- Implemented the ARMv8 RAS virtualization under DragonFly, improving VM availability under hardware errors.
- Investigated and fixed online issues. Analyzed and optimized virtualization performance overhead.

ByteDance 09/2021 – 04/2023

Rust R&D Intern, *Lark Cross Platform Infrastructure*

- Collaborated in the development of the cross-platform Rust SDK for Lark Messenger's client application.
- Provided security components for Lark Messenger to ensure the security of messages.
- Maintained storage component of Lark Messenger, including:
  - Developed *squam*, a SQL toolkit based on sqlite3 focused on binary size and performance optimization. Comes with a better binary footprint compared to `diesel`.
  - Introduced type-checking for SQL queries to detect most bugs at compile-time.
  - Tuned SQLite performance, maintained database CI, and assisted business teams in troubleshooting database issues.
- Maintain the stability of *Lark Messenger*. Troubleshoot *panics* and *crashes*. Discovered bugs and design flaws in foundational libraries such as `libunwind`, `rust std` and `darwin`.

ByteDance 04/2020 – 07/2020

iOS R&D Intern, *Lark iOS*

- Participated in the development of Lark iOS app.
- Implemented multiple feature enhancements, including adding support for selecting all group members when buzzing, etc.
- Fixed various layout issues in i18n scenarios, thereby improving user experience.

Research Institute for Information Technology, Tsinghua University 10/2019 – 04/2020

Research Intern, *NSLab*

- Explored the hardening of distributed graph database *nebula* with Intel SGX.
- Leveraged `avx2` to accelerate the aggregation step of federated learning with SGX.

Portfolios

- **Sirius** : An in-order **dual-issue** microprocessor core that runs on FPGA. Additionally, a complete SoC has been built based on this processor, supporting peripherals such as Ethernet and serial ports. The uCore teaching operating system can run on the SoC, and it's theoretically capable of running a complete Linux operating system.
- **SpinalHDL** : A new hardware description language for FPGA and ASIC design. Implemented support for using two industrial simulation suites, VCS and Xilinx Vivado, as testing backends, which has received widespread praise.

Honors and Awards

ByteDance 2022 Q3 **Spot Bonus** October 2022
First Prize of the Third National Student Computer System Capability Challenge August 2019
Several scholarships of Beijing Univ. of Posts and Telecommunications 2018 – 2022

Skills

- **Languages**: passed CET-6, can handle daily communication and document reading in English.
- **Programming Languages**: not limited to any specific language, but experienced in Rust/C/C++/Chisel, comfortable with Python/Swift/Go/Assembly.
- **Development Skills**: familiar with client side native development(C/C++/Rust) and virtualization(KVM/QEMU/LibVirt). **extremely** good at problem analysis and investigation.
- **Open-source Contributions**: contributed to **rust-lang/rust**, **SpinalHDL** etc.