

# HAIXIN YU

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## EDUCATION

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**Beijing University of Posts and Telecommunications**, Master of Computer Technology 2021 – 2024

- Major: Computer Technology, *School of Computer Science*

**Beijing University of Posts and Telecommunications**, Bachelor's Degree 2017 – 2021

- Major: Computer Science and Technology, *School of Computer Science*, GPA: 3.50

## WORK EXPERIENCE

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**ByteDance**, Beijing, China 09/2021 – Now

(**Lark Cross Platform Infrastructure**) R&D Intern, Rust

- Collaborated in the development of the cross-platform Rust SDK for Lark Messenger's client application.
- Provided security components for Lark Messenger to ensure the security of messages.
- Maintained storage component of Lark Messenger, including:
  - Developed *squam*, a SQL toolkit based on *sqlite3* focused on binary size and performance optimization. Comes with a better binary footprint compared to *diesel*.
  - Built an asynchronous *sqlite* connection pool that has higher throughput than *r2d2*.
  - Introduced type-checking for SQL queries to detect most bugs at compile-time.
  - Tuned *SQLite* performance, maintained database-related CI, and assisted business teams in troubleshooting database issues.
- Responsible for the stability of the Lark Messenger. Troubleshoot *panics* and *crashes*. Discovered bugs and design flaws in foundational libraries such as *libunwind*, *rust std* and *darwin*.
- Refactored flow log uploading module in Lark Messenger, improving code quality and readability.

**ByteDance**, Beijing, China 04/2020 – 07/2020

(**Lark iOS**) R&D Intern, iOS

- Participated in the development of Lark iOS app.
- Implemented multiple feature enhancements, including adding support for selecting all group members when buzzing, etc.
- Fixed various layout issues in *i18n* scenarios, thereby improving user experience.

**Research Institute for Information Technology**, Tsinghua University 10/2019 – 04/2020

(**NSLab**) Research Intern

- Explored the hardening of distributed graph database *nebula* with Intel SGX.
- Leveraged *avx2* to accelerate the aggregation step of federated learning with SGX.

## PORTFOLIOS

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- **Sirius**: An in-order **dual-issue** microprocessor core that runs on FPGA. Additionally, a complete SoC has been built based on this processor, supporting peripherals such as Ethernet and serial ports. The uCore teaching operating system can run on the SoC, and it's theoretically capable of running a complete Linux operating system.
- **Muddy DNS**: A DNS relay server with DNS forwarding and malicious website blocking, implemented in Go. It parses DNS packet headers according to RFC 1035, and operates on the packet based on *thr* rules. Supports high concurrency.
- **SpinalHDL**: A new hardware description language for FPGA and ASIC design. Implemented support for using two industrial simulation suites, VCS and Xilinx Vivado, as testing backends, which has received widespread praise.

## HONORS AND AWARDS

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ByteDance 2022 Q3 **Spot Bonus** October 2022

**First Prize** of the Third National Student Computer System Capability Challenge August 2019

## SKILLS

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- **Programming Languages**: not limited to any specific language, but experienced in Rust/C/C++/Chisel, comfortable with Python/Swift/Go/Assembly.
- **Languages**: Passed CET-6, can handle daily communication and document reading in English.
- **Developing Tools**: experienced in Linux programming, have experience with collaboration tools like Git, etc.
- **Open-source Contributions**: contributed to **rust-lang/rust**, **SpinalHDL** etc.