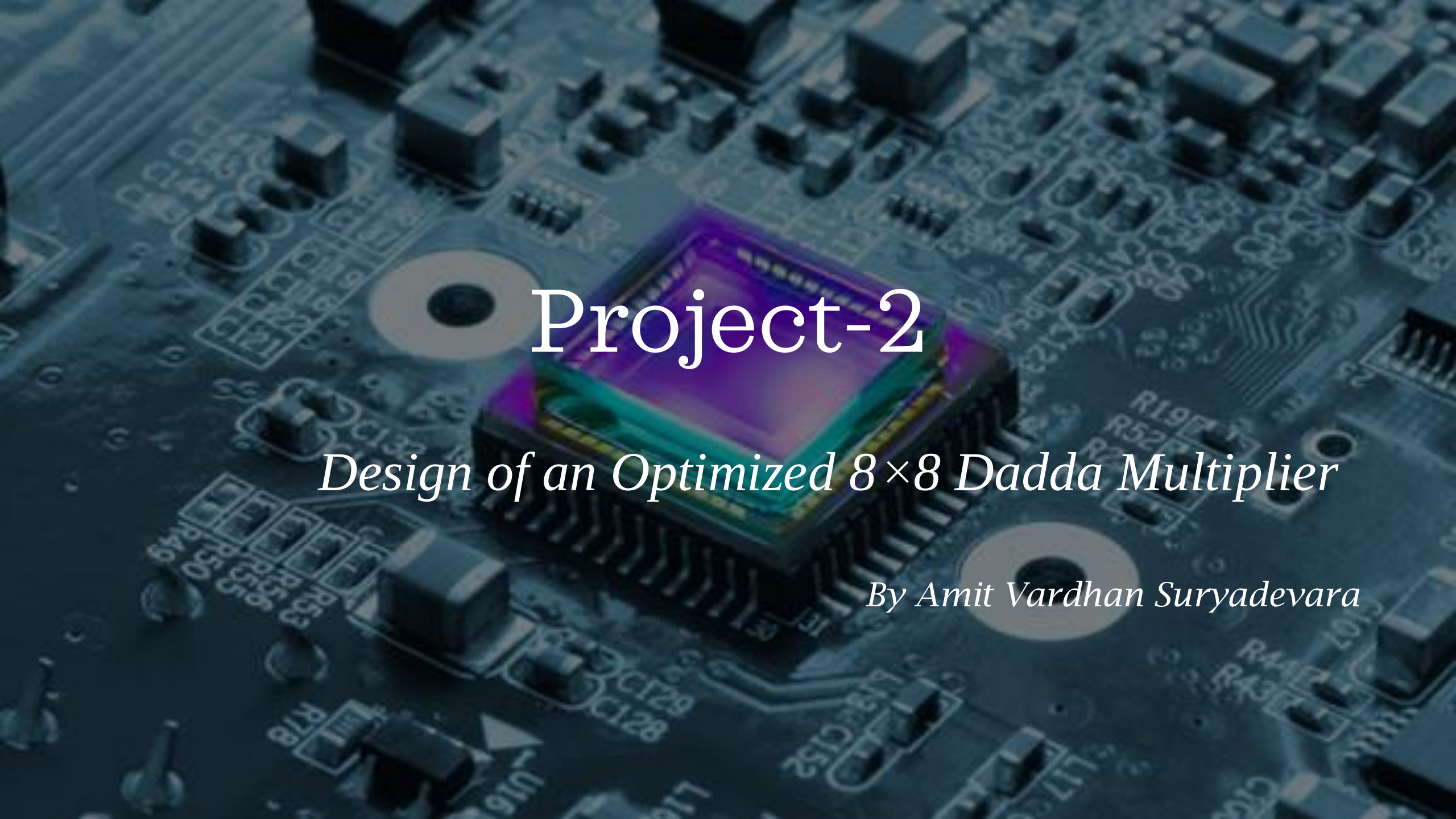


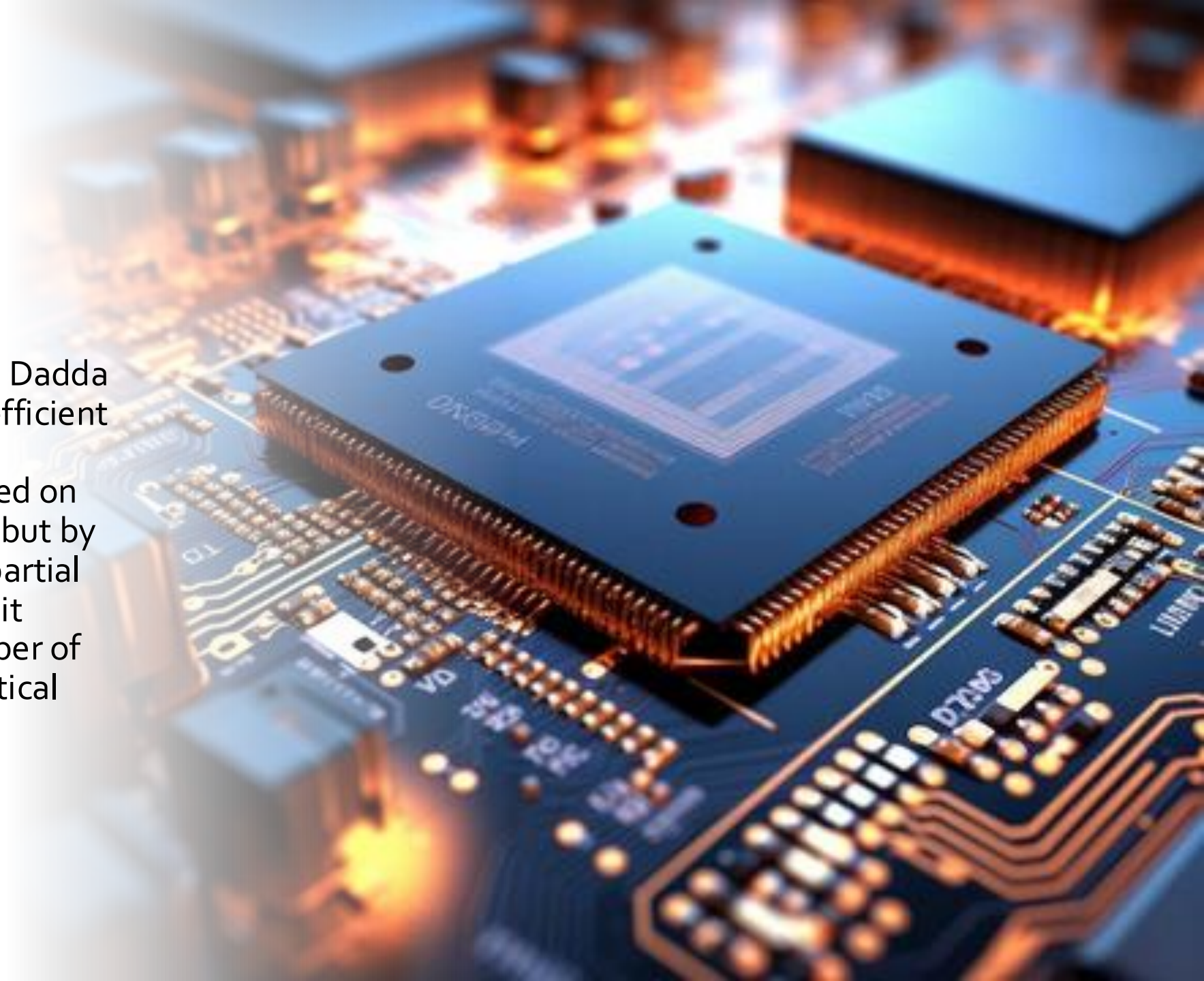
Project-2

Design of an Optimized 8×8 Dadda Multiplier

By Amit Vardhan Suryadevara

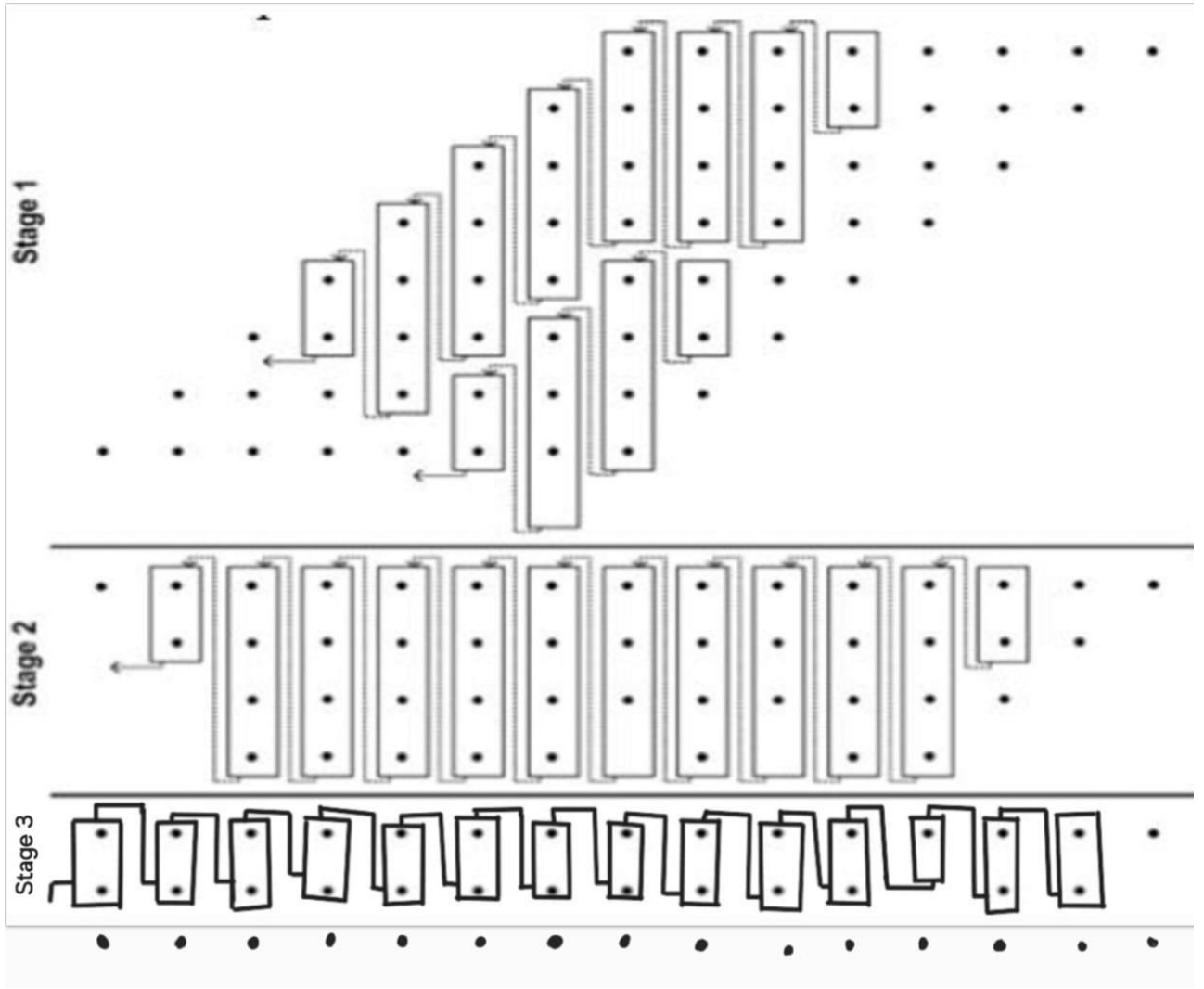
History of Dadda Multiplier

Luigi Dadda introduced the Dadda multiplier, a fast and area-efficient hardware multiplication technique, in 1965. It is based on the Wallace tree approach, but by carefully reorganizing the partial product reduction process, it further minimizes the number of hardware resources and critical path time.

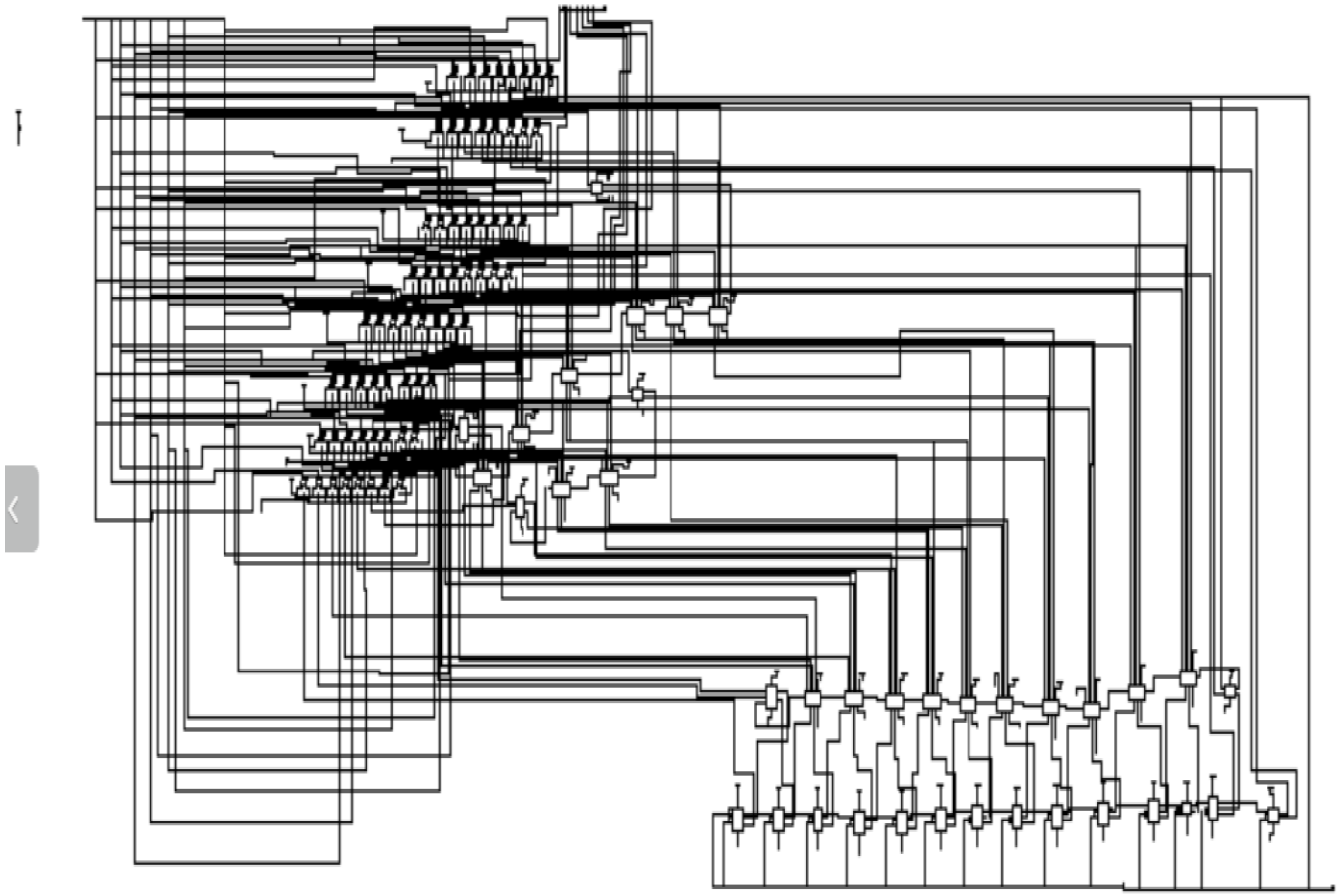


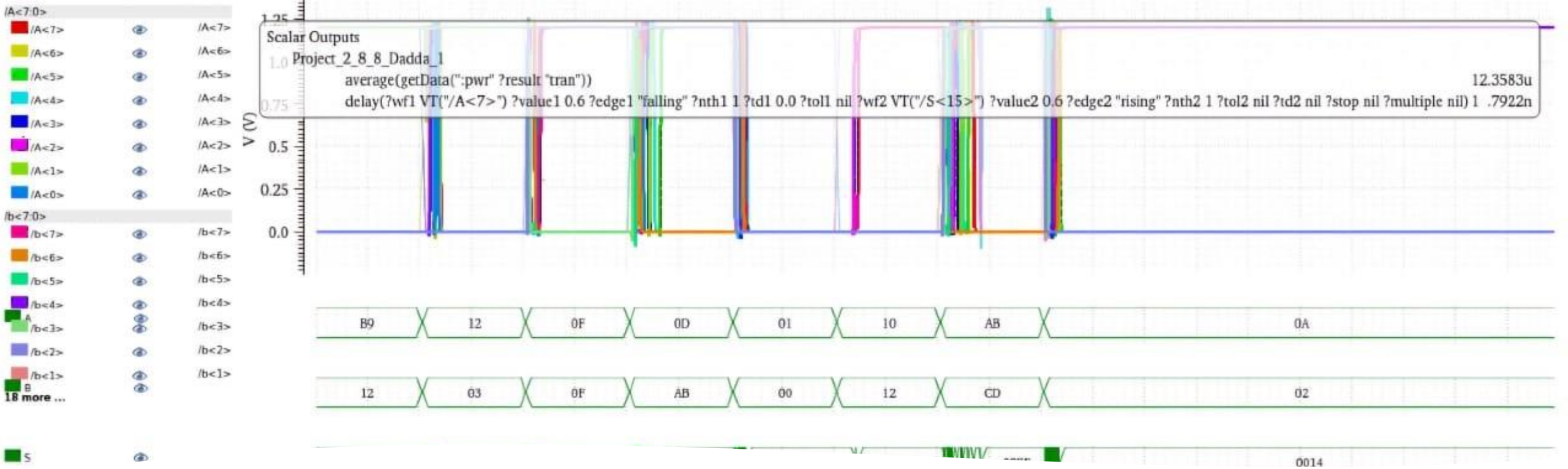
8*8 DADDA MULTIPLIER ARCHITECTURE

- Similar to Wallace tree multipliers, the Dadda multiplier generates all partial products first (using AND gates) and then reduces them in stages using compressors and adders(e.g., 4:2 compressors, full adders, half adders).
- The reduction stages are optimized to keep the total number of rows as close as possible to the powers of two, minimizing unnecessary addition operations.
- Once reduced to two rows of partial products, a series of FA and Half adders are used to generate final result.



The 8*8 Dadda architecture uses The final schematic contains 18 Compressors, 15 FA, 5 HA.
The output is generated in the 3 stages followed by the final stage





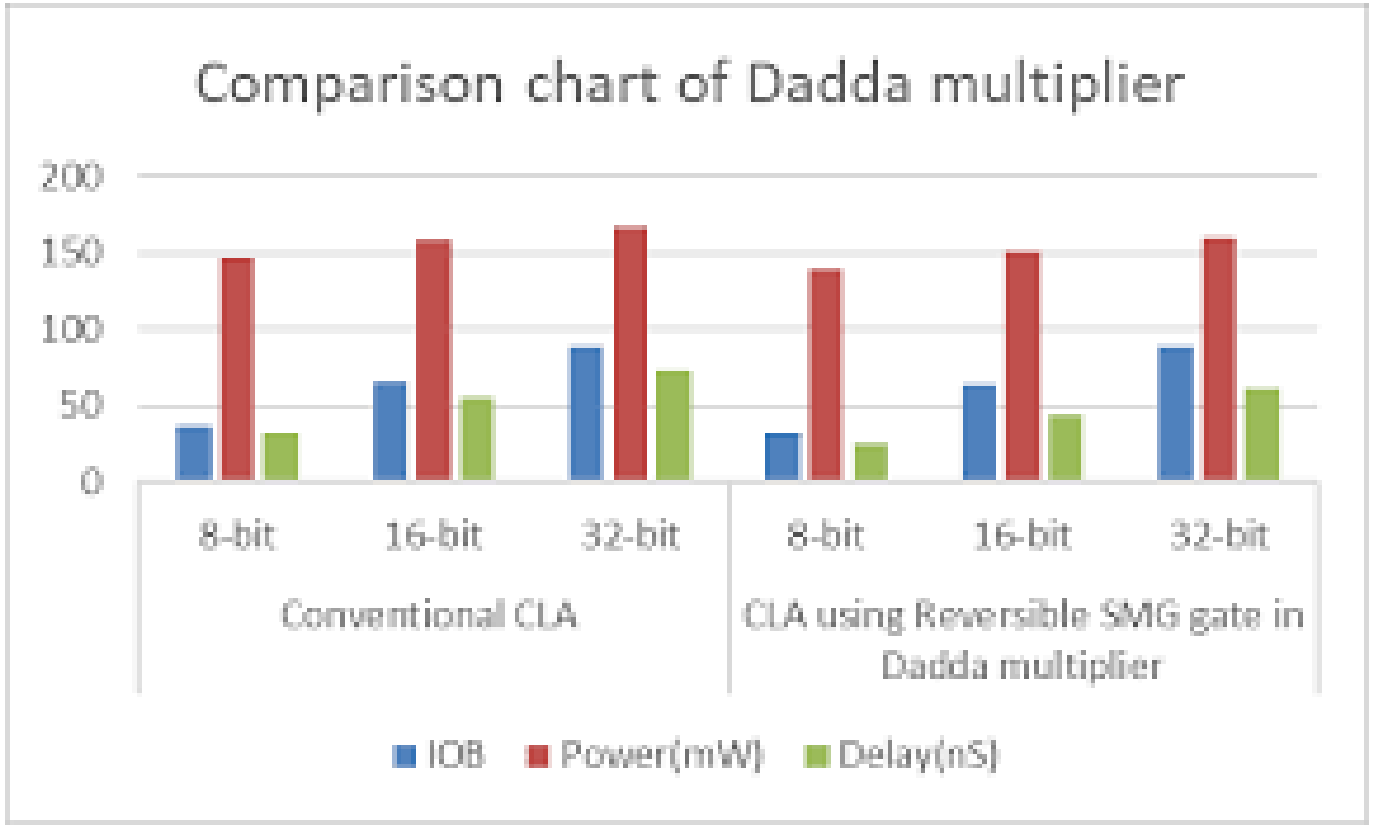
The waveform of the **8x8 Dadda multiplier**, running at a clock period of **2 ns** (equivalent to a frequency of **500 MHz**), demonstrates effective output generation for the specified **8-input series**. Minor transient disturbances are visible in the waveform, primarily caused by the circuit's inherent **propagation delay**. The measured delay of approximately **1.7 ns** is minimal compared to the clock period, allowing the multiplier to function efficiently within its timing requirements while producing stable and accurate outputs.

Power dissipation and Delay

- The **average power dissipation** in Dadda multipliers, in general, is approximately **90 µW**, making them relatively power-efficient compared to other multiplication architectures. However, in this specific 8x8 Dadda multiplier design, the calculated power dissipation is significantly lower at **12 µW**, highlighting the effectiveness of the implemented design and optimizations in reducing power consumption.
- The **propagation delay** of the multiplier is measured to be **1.7 ns**, which is exceptionally small compared to the clock period (2 ns). This negligible delay ensures that the circuit operates well within its timing constraints, supporting high-speed multiplication at a frequency of **500 MHz**.

Architectures

- The **Wallace Tree Multiplier** is faster due to active reduction of partial products at every level but consumes more power and area, making it suitable for high-speed applications like microprocessors and FPGAs.
- The **Dadda Multiplier** balances speed, power, and area by reducing partial products only when necessary, resulting in fewer adders and stages, making it ideal for low-power and embedded systems.
- The **Array Multiplier** is simpler to implement but slower and less efficient in terms of power and area, making it appropriate for low-performance or less resource-sensitive applications.



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Thank You