

# Amit Vardhan Suryadevara

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## Objective

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Motivated Electrical and VLSI Engineer with a passion for designing and building innovative hardware systems. Skilled in prototyping, circuit design, and electromechanical integration, with a drive to deliver solutions that enhance performance, reliability, and energy efficiency. I aim to contribute my technical expertise and creative problem-solving abilities to forward-thinking projects that push the boundaries of technology and have a meaningful impact.

## Education

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<b>Purdue University</b> <i>BS in Electrical Engineering</i> <i>MS in Electrical Engineering</i> <i>(Specialization in VLSI)</i>	<i>CGPA</i> <i>3.43/4</i> <i>4/4</i>	Indianapolis, IN <i>May 2025</i> <i>Graduating May 2026</i>
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## Honors and Awards

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### Dave & Marsha Meyer ECE Undergraduate Teaching Assistant Award (2024–2025)

Received for being one of the most hardworking, dependable, and approachable Undergraduate Teaching Assistants (UTA) for Courses Signals and Systems, Fundamentals of Electrical Engineering, and Introduction to Electrical Circuits, Sensors and Motors Lab.

## Relevant Skills

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- **Analog Circuit Design & Layout:** Cadence Virtuoso, SPICE simulation, Electromigration, IR drop analysis, layout optimization
- **Programming Languages:** Python, Shell, C/C++, Verilog, ModelSim, LABVIEW
- **CAD Tools:** Exposure to AutoCAD, SolidWorks for circuit design and modeling
- **Simulation Analysis:** LTSpice, MATLAB, Multisim, KiCAD, PSpice, Altium Designer
- **Simulation & Layout:** Layout design, parasitic extraction, DRC/LVS checks
- **Digital Circuit Design & Verification:** Proficient in Verilog/VHDL for ASIC and FPGA development
- **Protocols & Interfaces:** I2C, SPI, UART, SCPI
- **Hardware Prototyping:** PCB Soldering, Breadboarding, Circuit Debugging, Oscilloscopes, signal generators

## Experience

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### Electromechanical Engineering Intern – Modine Manufacturing

*June 2024 – Aug 2024*

- Optimized capacitor designs for electromechanical systems, improving energy efficiency by 15% and lifespan by 20%.
- Conducted detailed analysis and development of bypass and regular capacitors for electromechanical systems, ensuring optimal performance and compliance with design specifications.
- Conducted failure mode analysis and proposed solutions for power distribution components.

## Teaching Assistant – Electrical Systems

*Aug 2024 – May 2025*

- Assisted students in designing and analyzing electrical circuits, covering fundamental topics such as voltage, current, resistance, and power.
- Supervised and guided students through laboratory experiments involving sensors, motors, and basic electronic components to strengthen practical understanding of electrical systems.
- Provided technical support to students by troubleshooting circuit issues and helping them debug errors in sensor and motor-based systems.

## Projects

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### 8×8 Dadda Multiplier Design | Cadence Virtuoso

- Designed an 8×8 Dadda multiplier in 45nm CMOS technology for high-performance RISC processors using Cadence Virtuoso.
- Utilized 4:2 compressors, full adders, and half adders to optimize speed and area efficiency.
- Validated transistor-level design and ensured readiness for next-generation chip tape-out.
- Performed extensive post-layout simulations and power analysis to ensure minimal delay and power consumption, optimizing the design for energy-efficient computation.

### Hand Gesture-Controlled Car | Arduino, AUTOCAD, Visual Studio

- Built a fully wireless car controlled by MPU6050-based hand gestures transmitted via NRF24L01+ modules.
- Developed Arduino firmware for interpreting sensor data and translating it into precise PWM signals.
- Implemented autonomous obstacle avoidance using servo-mounted ultrasonic sensors and LIDAR.
- Added real-time feedback with LEDs, emergency stop conditions, and gesture recovery logic.

### Neuromorphic Computing Hardware Modeling | Research Thesis

- Modeled memristor behavior using TCAD synopsis and studied the limitations in voltage thresholds and switching time.
- Implemented Hebbian learning and STDP algorithms to simulate synaptic plasticity in neural networks.
- Evaluated Von Neumann bottleneck challenges and proposed memory-logic co-located architectures for FinFET-based devices.
- Applied TCAD simulation to analyze device-level characteristics of emerging memory elements for neuromorphic hardware.

### STM32-Based Hardware Design and Development | KiCad 6, STM32CubeIDE, JLCPCB, ST-Link

- Designed and developed a custom STM32F103C8-based PCB using KiCad 6, including schematic capture, PCB layout, and manufacturing file generation.
- Configured microcontroller peripherals, pinout, and clocks in STM32CubeIDE to enable USB and GPIO functionality.
- Utilized ST-Link debug probes for hardware programming, debugging, and live variable monitoring, enhancing firmware development and testing.
- Coordinated PCB fabrication and assembly through JLCPCB, applying manufacturer design rules and verifying production files with Gerber viewer.

## Leadership and Involvement

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- Member, IEEE Purdue Student Chapter