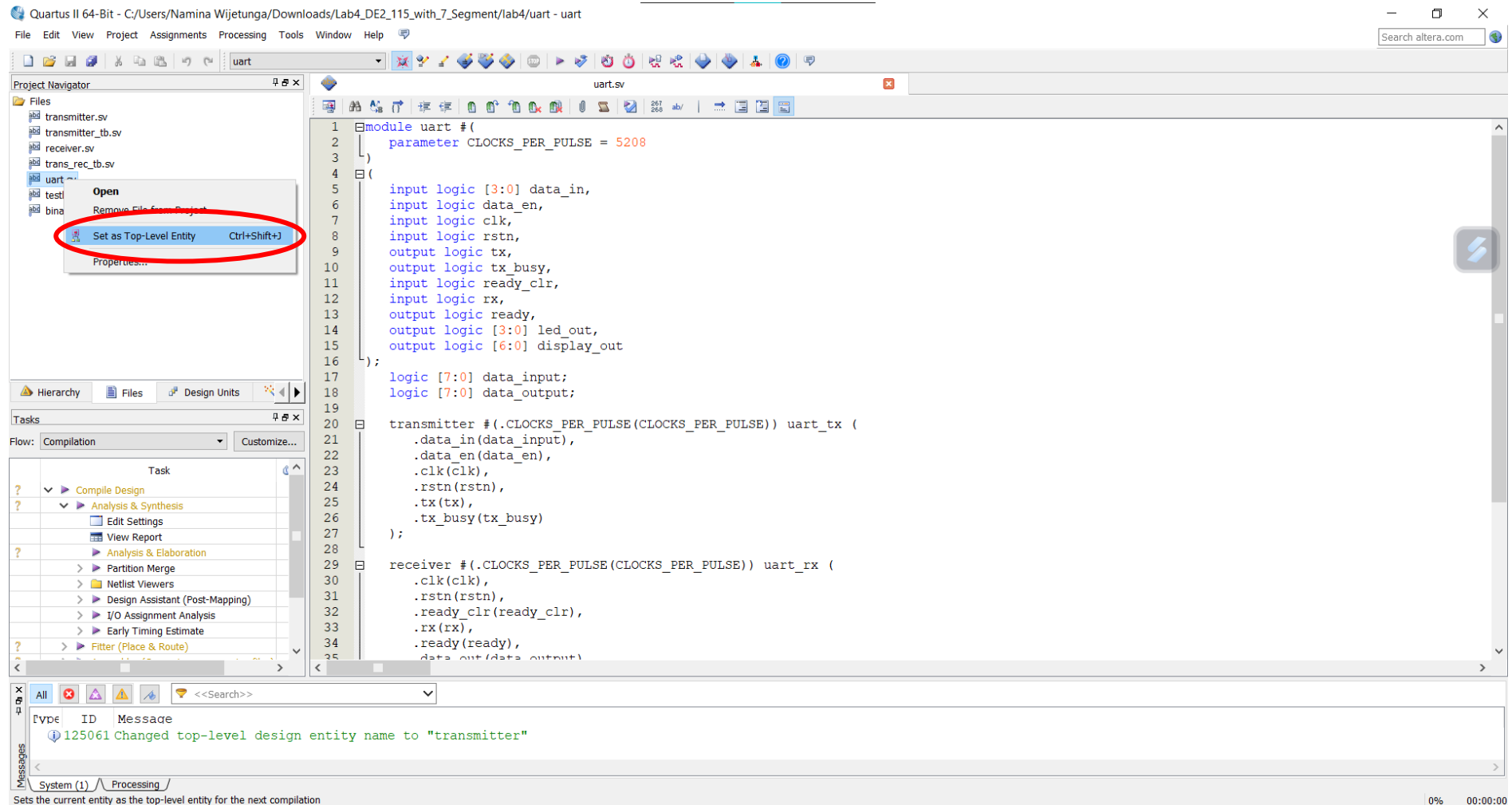


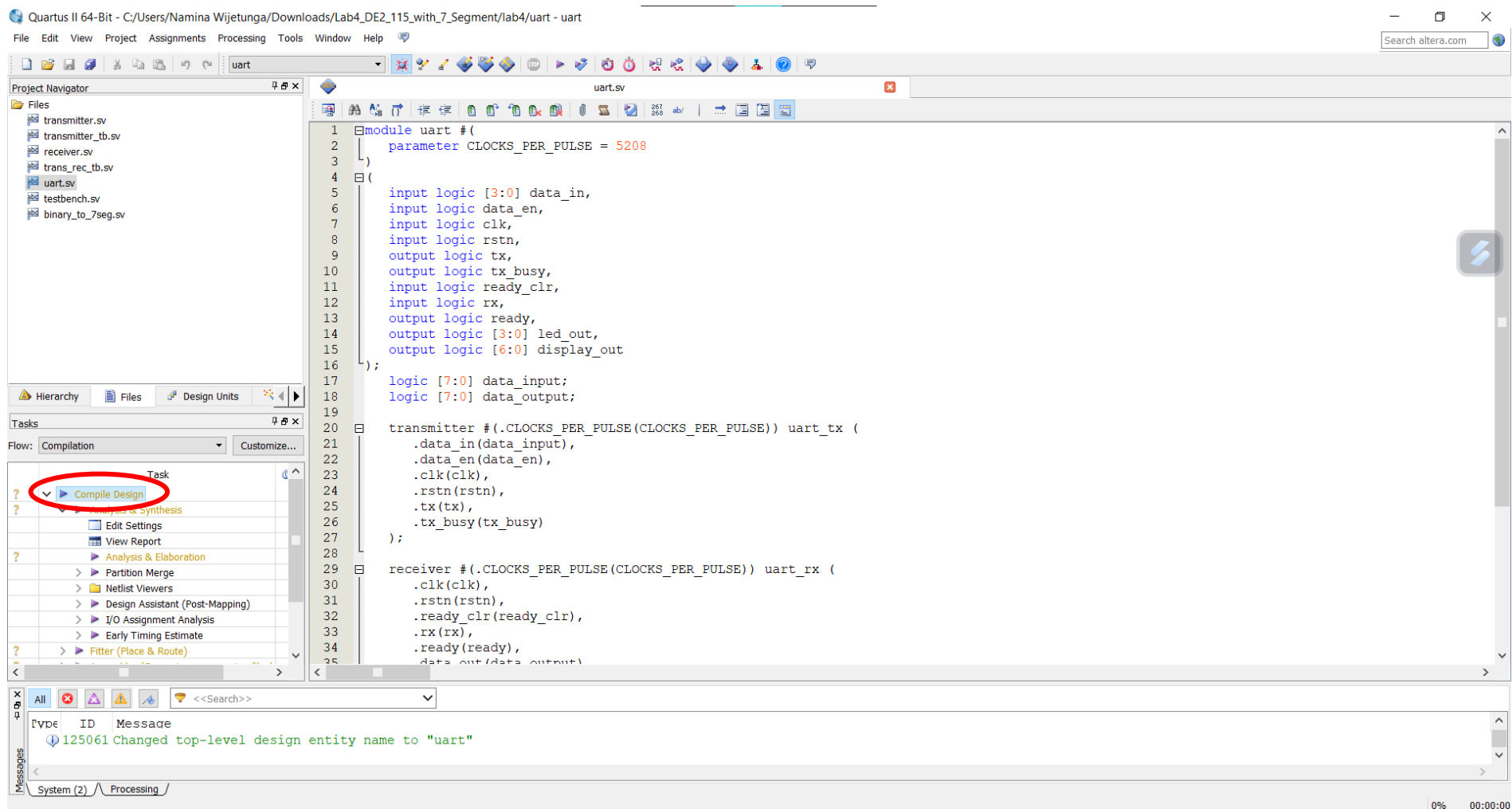
# Uploading and Operating Guidelines

**Altera DE2-115**

# Select uart.lv file as the Top-Level Entity.



# Double click on the “Compile Design” button.



# If the compilation is successful, the window will look like this.

The screenshot displays the Quartus II 64-bit IDE interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The toolbar contains various icons for file operations and compilation. The Project Navigator on the left shows a list of files: transmitter.v, transmitter\_tb.v, receiver.v, trans\_rec\_tb.v, uart.v, testbench.v, and binary\_to\_7seg.v. The central pane shows the 'uart.v' file with a 'Table of Contents' on the left and a 'Flow Summary' on the right. The 'Flow Summary' table provides details about the compilation process, including the flow status, version, revision name, top-level entity name, family, device, timing models, and resource usage. The bottom pane shows the 'Messages' window with a green message indicating a successful compilation.

Quartus II 64-Bit - C:/Users/Namina Wijetunga/Downloads/Lab4\_DE2\_115\_with\_7\_Segment/lab4/uart - uart

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Files

- transmitter.v
- transmitter\_tb.v
- receiver.v
- trans\_rec\_tb.v
- uart.v
- testbench.v
- binary\_to\_7seg.v

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- TimeQuest Timing Analyzer
- EDA Netlist Writer
- Flow Messages
- Flow Suppressed Messages

Flow Summary

|                                    |  |
|------------------------------------|--|
| Flow Status                        | Successful - Tue Jun 13 02:47:21 2023      |
| Quartus II 64-Bit Version          | 13.1.0 Build 162 10/23/2013 SJ Web Edition |
| Revision Name                      | uart                                       |
| Top-level Entity Name              | uart                                       |
| Family                             | Cyclone IV E                               |
| Device                             | EP4CE115F29C7                              |
| Timing Models                      | Final                                      |
| Total logic elements               | 88 / 114,480 ( < 1 % )                     |
| Total combinational functions      | 86 / 114,480 ( < 1 % )                     |
| Dedicated logic registers          | 47 / 114,480 ( < 1 % )                     |
| Total registers                    | 47   |
| Total pins                         | 23 / 529 ( 4 % )                           |
| Total virtual pins                 | 0  |
| Total memory bits                  | 0 / 3,981,312 ( 0 % )                      |
| Embedded Multiplier 9-bit elements | 0 / 532 ( 0 % )                            |
| Total PLLs                         | 0 / 4 ( 0 % )                              |

Tasks

Flow: Compilation Customize...

| Task                            | Progress |
|---------------------------------|----------|
| Compile Design                  | 00       |
| Analysis & Synthesis            | 00       |
| Edit Settings                   |          |
| View Report                     |          |
| Analysis & Elaboration          |          |
| Partition Merge                 |          |
| Netlist Viewers                 |          |
| Design Assistant (Post-Mapping) |          |
| I/O Assignment Analysis         |          |
| Early Timing Estimate           |          |
| Fitter (Place & Route)          | 00       |

Messages

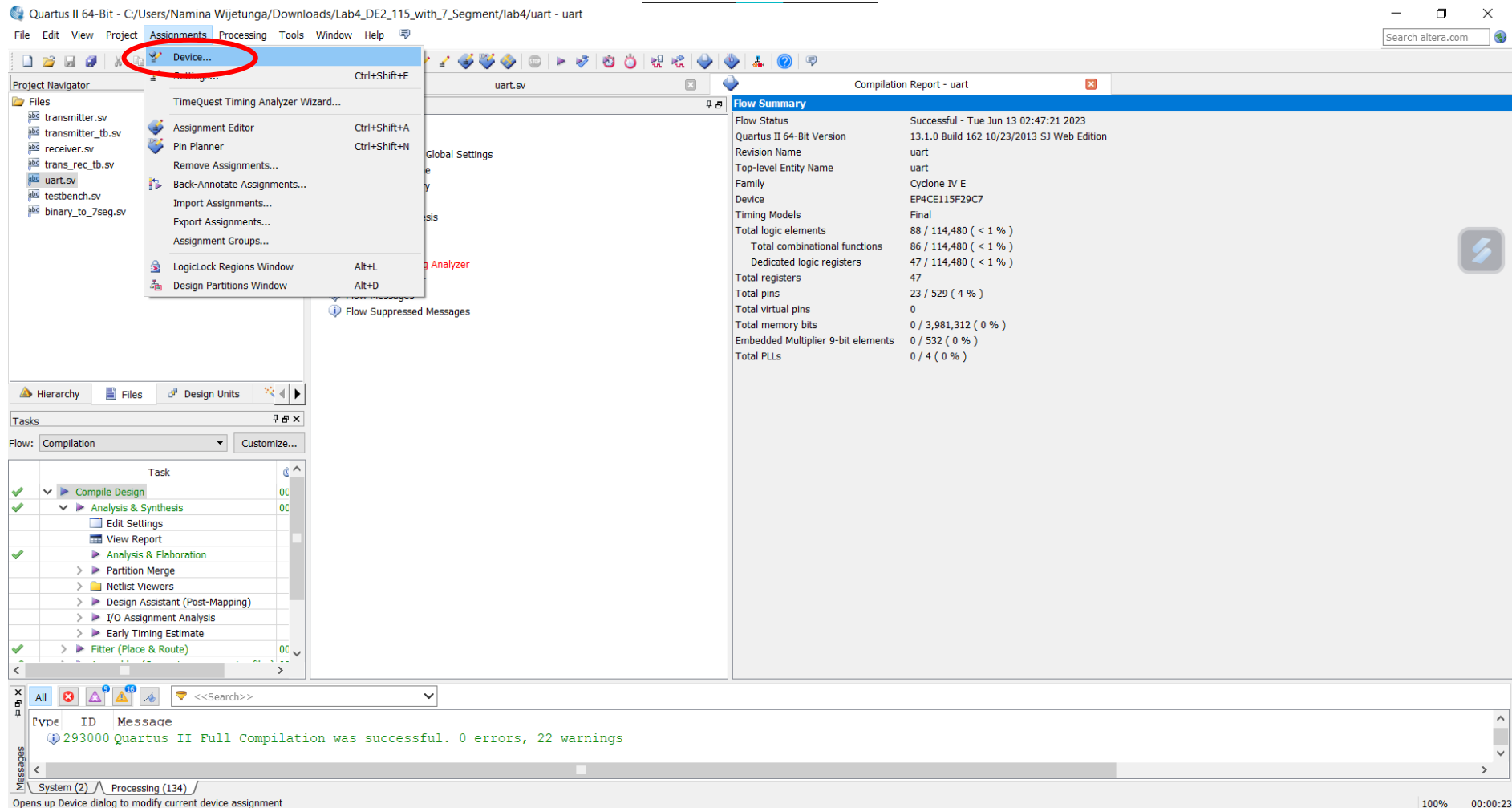
Type ID Message

293000 Quartus II Full Compilation was successful. 0 errors, 22 warnings

System (2) Processing (134)

100% 00:00:23

# Go to “Assignments” tab and select “Device”.



# Make sure the device and family are selected correctly.

Quartus II 64-Bit - C:/Users/Namina Wijetunga/Downloads/Lab4\_DE2\_115\_with\_7\_Segment/lab4/uart - uart

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

- Files
  - transmitter.v
  - transmitter\_tb.v
  - receiver.v
  - trans\_rec\_tb.v
  - uart.v
  - testbench.v
  - binary\_to\_7seg.v

Table of Contents

- Flow Summary
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- EDA Netlist Writer
- Flow Messages
- Flow Suppressed Messages

Flow Summary

|                               |  |
|-------------------------------|--|
| Flow Status                   | Successful - Tue Jun 13 02:47:21 2023      |
| Quartus II 64-Bit Version     | 13.1.0 Build 162 10/23/2013 SJ Web Edition |
| Revision Name                 | uart                                       |
| Top-level Entity Name         | uart                                       |
| Family                        | Cyclone IV E                               |
| Device                        | EP4CE115F29C7                              |
| Timing Models                 | Final                                      |
| Total logic elements          | 88 / 114,480 ( < 1 % )                     |
| Total combinational functions | 86 / 114,480 ( < 1 % )                     |

Device

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

Device family: Cyclone IV E

Target device:

- ☐ Auto device selected by the Fitter
- ☒ Specific device selected in 'Available devices' list
- ☐ Other: n/a

Available devices:

| Name          | Core Voltage | LEs    | User I/Os | Memory Bits | Embedded multiplier |
|---------------|--------------|--------|-----------|-------------|---------------------|
| EP4CE115F29C7 | 1.2V         | 114480 | 529       | 3981312     | 532                 |

Migration Devices... 0 migration devices selected

Buy Software OK Cancel Help

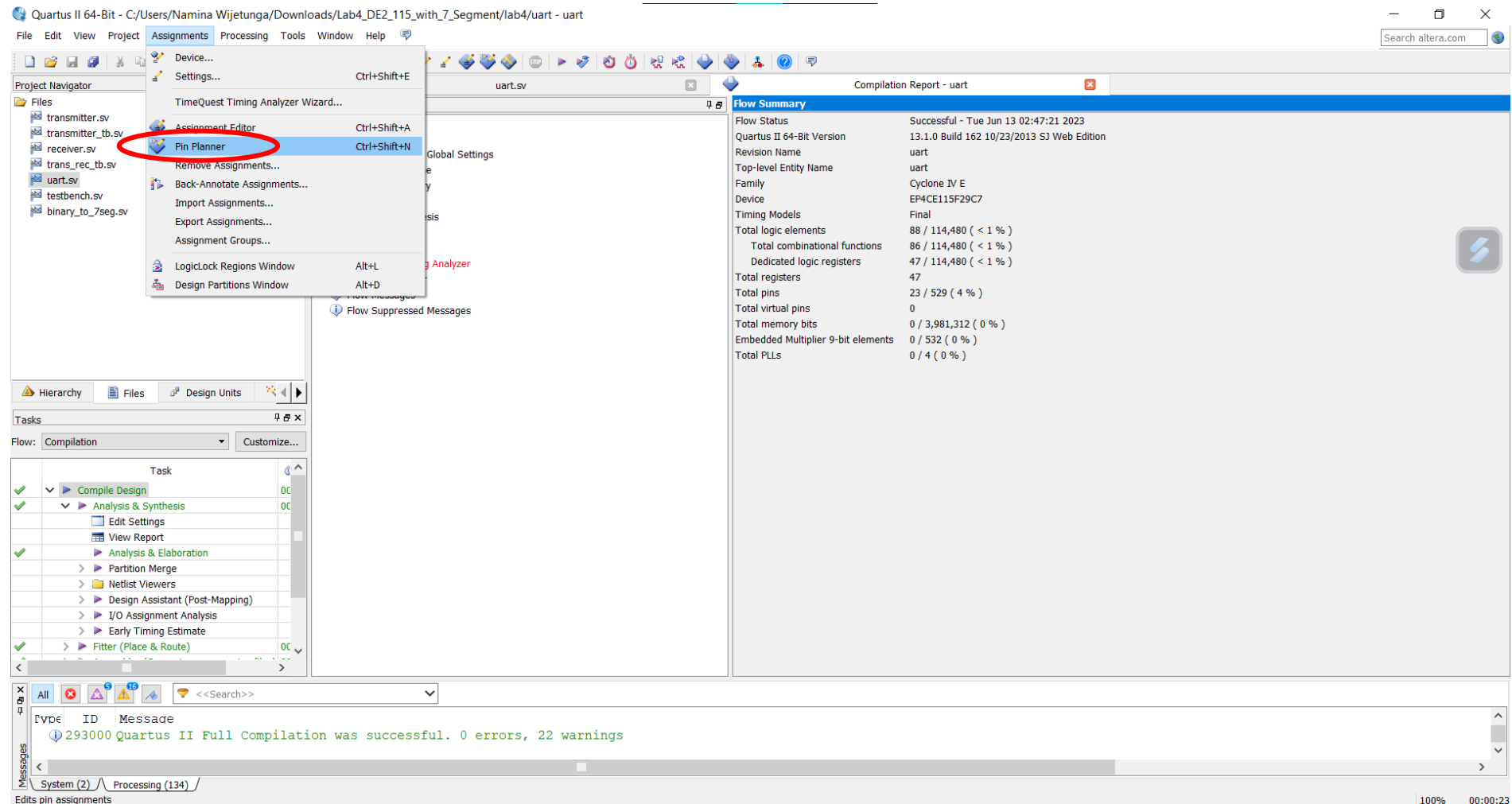
Messages

| Type | ID     | Message   |
|------|--------|---|
| Info | 293000 | Quartus II Full Compilation was successful. 0 errors. |

System (2) / Processing (134)

100% 00:00:23

# After successful completion of the device selection, go to “Pin Planner” under the same tab.



# Assign the pins as follows.

Pin Planner - C:/Users/Namina Wijetunga/Downloads/Lab4\_DE2\_115\_with\_7\_Segment/lab4/uart - uart

File Edit View Processing Tools Window Help

Search altera.com

Symbol Pin Type

- User I/O
- User assigned...
- Fitter assigne...

Report

Report not available

Groups Report

Tasks

- Early Pin Planning
  - Early Pin Planning...
  - Run I/O Assignment Analysis
  - Export Pin Assignments...

Top View - Wire Bond  
Cyclone IV E - EP4CE115F28C7

Named: \* Edit: [X] [Y] [Z]

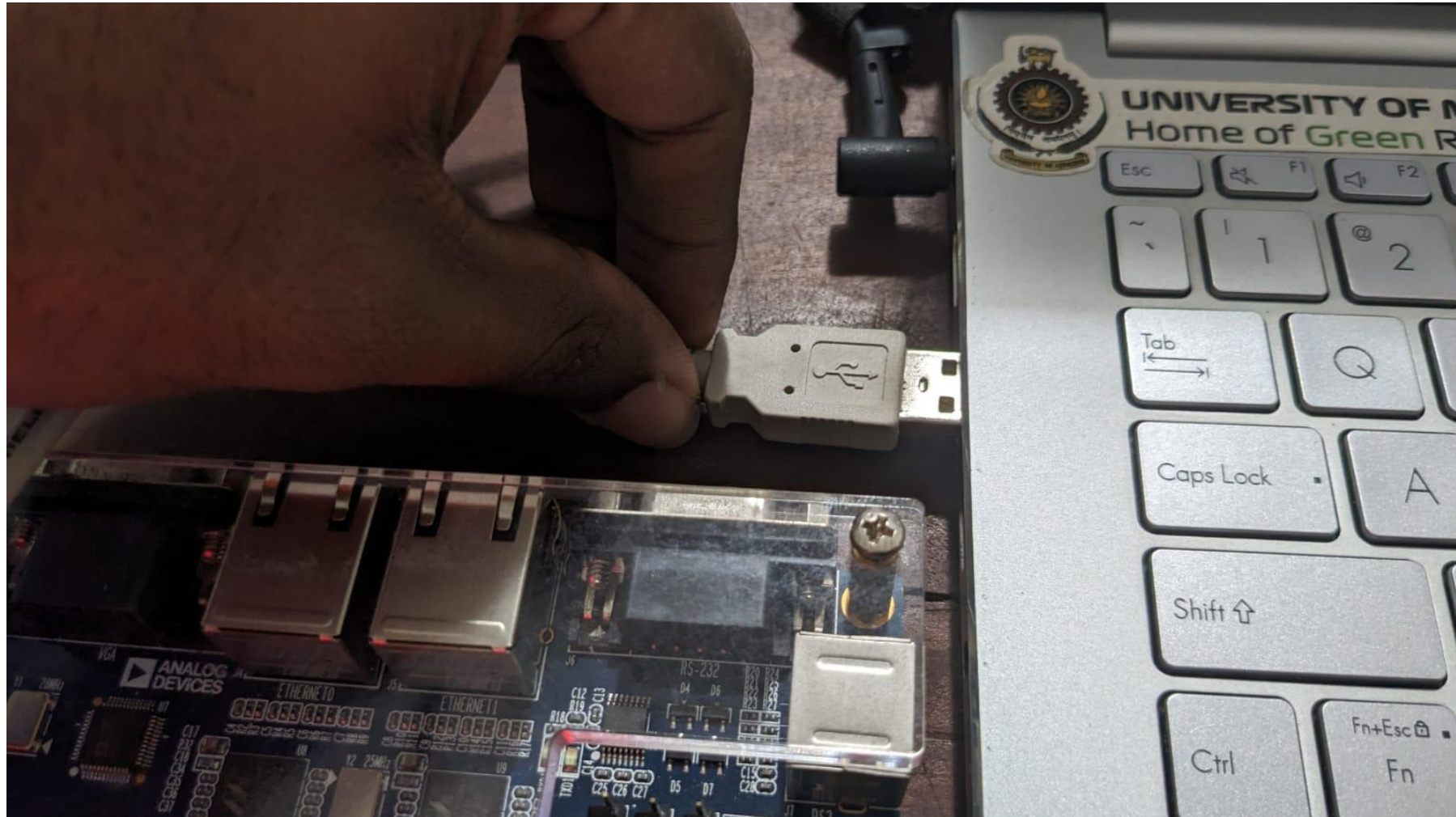
Filter: Pins: all

| Node Name      | Direction | Location | I/O Bank | VREF Group | Fitter Location | I/O Standard    | Reserved | Current Strength | Slew Rate   | Differential Pair |
|----------------|-----------|----------|----------|------------|-----------------|-----------------|----------|------------------|-------------|-------------------|
| clk            | Input     | PIN_Y2   | 2        | B2_N0      | PIN_Y2          | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |
| data_en        | Input     | PIN_M21  | 6        | B6_N1      | PIN_M21         | 2.5 V           |          | 8mA (default)    |             |                   |
| data_in[3]     | Input     | PIN_AD27 | 5        | B5_N2      | PIN_AD27        | 2.5 V           |          | 8mA (default)    |             |                   |
| data_in[2]     | Input     | PIN_AC27 | 5        | B5_N2      | PIN_AC27        | 2.5 V           |          | 8mA (default)    |             |                   |
| data_in[1]     | Input     | PIN_AC28 | 5        | B5_N2      | PIN_AC28        | 2.5 V           |          | 8mA (default)    |             |                   |
| data_in[0]     | Input     | PIN_AB28 | 5        | B5_N1      | PIN_AB28        | 2.5 V           |          | 8mA (default)    |             |                   |
| display_out[6] | Output    | PIN_H22  | 6        | B6_N0      | PIN_H22         | 2.5 V (default) |          | 8mA (default)    | 2 (default) |                   |
| display_out[5] | Output    | PIN_J22  | 6        | B6_N0      | PIN_J22         | 2.5 V (default) |          | 8mA (default)    | 2 (default) |                   |
| display_out[4] | Output    | PIN_L25  | 6        | B6_N1      | PIN_L25         | 2.5 V (default) |          | 8mA (default)    | 2 (default) |                   |
| display_out[3] | Output    | PIN_L26  | 6        | B6_N1      | PIN_L26         | 2.5 V (default) |          | 8mA (default)    | 2 (default) |                   |
| display_out[2] | Output    | PIN_E17  | 7        | B7_N2      | PIN_E17         | 2.5 V (default) |          | 8mA (default)    | 2 (default) |                   |
| display_out[1] | Output    | PIN_F22  | 7        | B7_N0      | PIN_F22         | 2.5 V (default) |          | 8mA (default)    | 2 (default) |                   |
| display_out[0] | Output    | PIN_G18  | 7        | B7_N2      | PIN_G18         | 2.5 V (default) |          | 8mA (default)    | 2 (default) |                   |
| led_out[3]     | Output    | PIN_F21  | 7        | B7_N0      | PIN_F21         | 2.5 V           |          | 8mA (default)    | 2 (default) |                   |
| led_out[2]     | Output    | PIN_E19  | 7        | B7_N0      | PIN_E19         | 2.5 V           |          | 8mA (default)    | 2 (default) |                   |
| led_out[1]     | Output    | PIN_F19  | 7        | B7_N0      | PIN_F19         | 2.5 V           |          | 8mA (default)    | 2 (default) |                   |
| led_out[0]     | Output    | PIN_G19  | 7        | B7_N2      | PIN_G19         | 2.5 V           |          | 8mA (default)    | 2 (default) |                   |
| ready          | Output    | PIN_E22  | 7        | B7_N0      | PIN_E22         | 2.5 V           |          | 8mA (default)    | 2 (default) |                   |
| ready_clr      | Input     | PIN_N21  | 6        | B6_N2      | PIN_N21         | 2.5 V           |          | 8mA (default)    |             |                   |
| rstn           | Input     | PIN_M23  | 6        | B6_N2      | PIN_M23         | 2.5 V           |          | 8mA (default)    |             |                   |
| rx             | Input     | PIN_AC15 | 4        | B4_N2      | PIN_AC15        | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |
| tx             | Output    | PIN_AB22 | 4        | B4_N0      | PIN_AB22        | 3.3-V LVTTTL    |          | 8mA (default)    | 2 (default) |                   |
| tx_busy        | Output    | PIN_E21  | 7        | B7_N0      | PIN_E21         | 2.5 V           |          | 8mA (default)    | 2 (default) |                   |
| data_in[7]     | Unknown   |          |          |            |                 | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |
| data_in[6]     | Unknown   |          |          |            |                 | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |
| data_in[5]     | Unknown   |          |          |            |                 | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |
| data_in[4]     | Unknown   |          |          |            |                 | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |
| data_out[7]    | Unknown   |          |          |            |                 | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |
| data_out[6]    | Unknown   |          |          |            |                 | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |
| data_out[5]    | Unknown   |          |          |            |                 | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |
| data_out[4]    | Unknown   |          |          |            |                 | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |
| data_out[3]    | Unknown   |          |          |            |                 | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |
| data_out[2]    | Unknown   |          |          |            |                 | 3.3-V LVTTTL    |          | 8mA (default)    |             |                   |

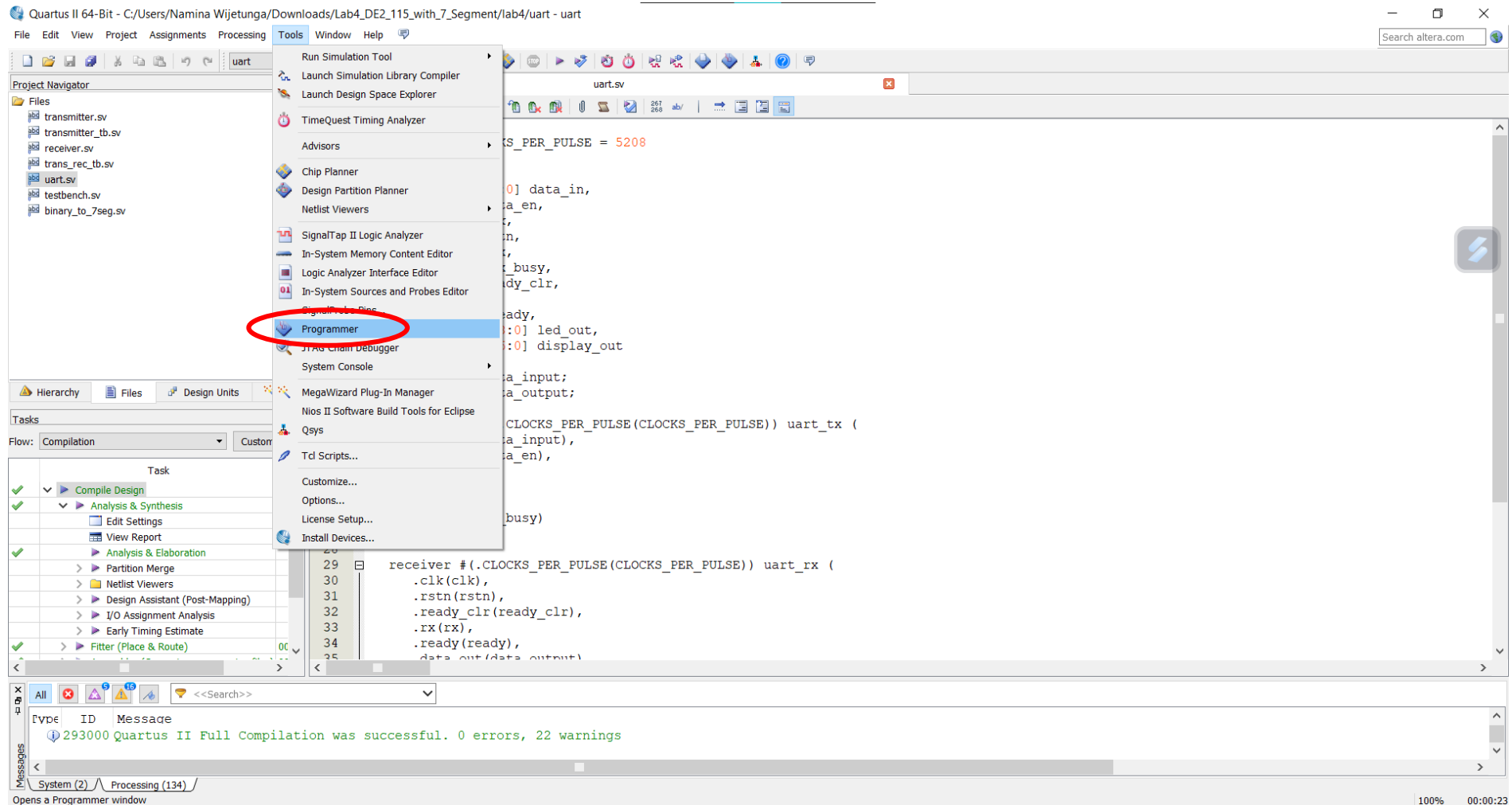
0% 00:00:00



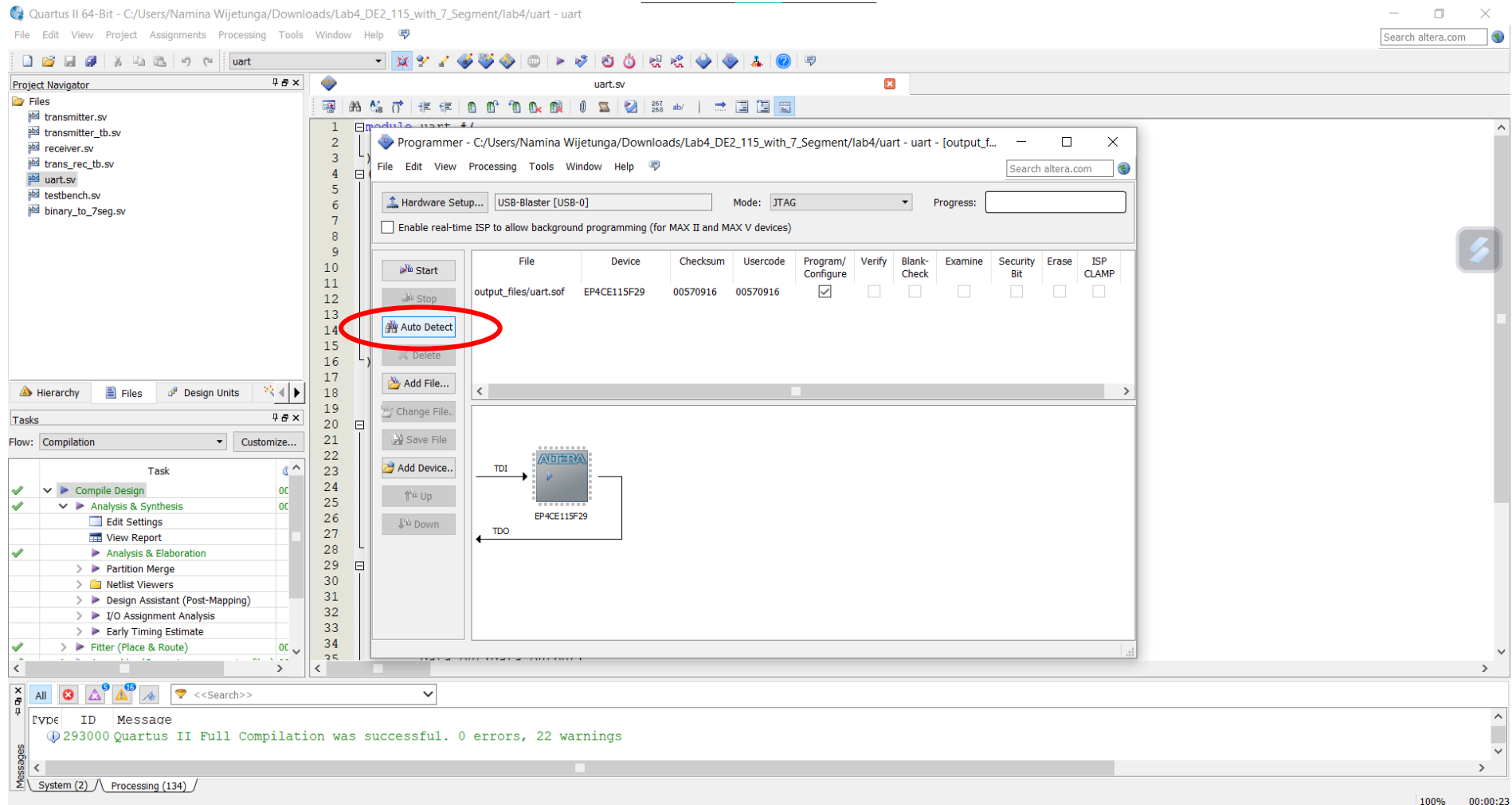
# Connect the DE2-115 board to the PC.



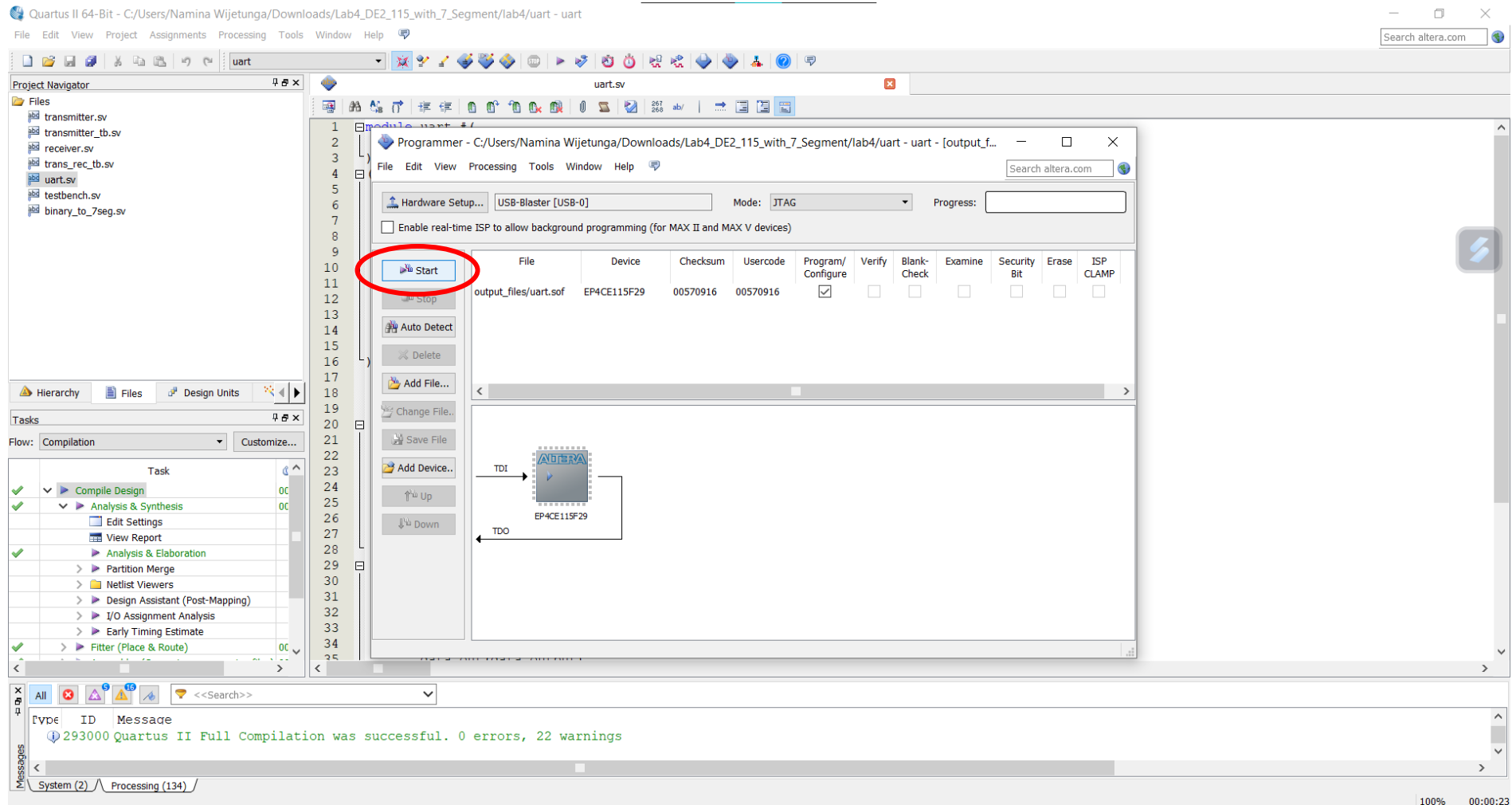
# Go to “Tools” tab and select “Programmer”.



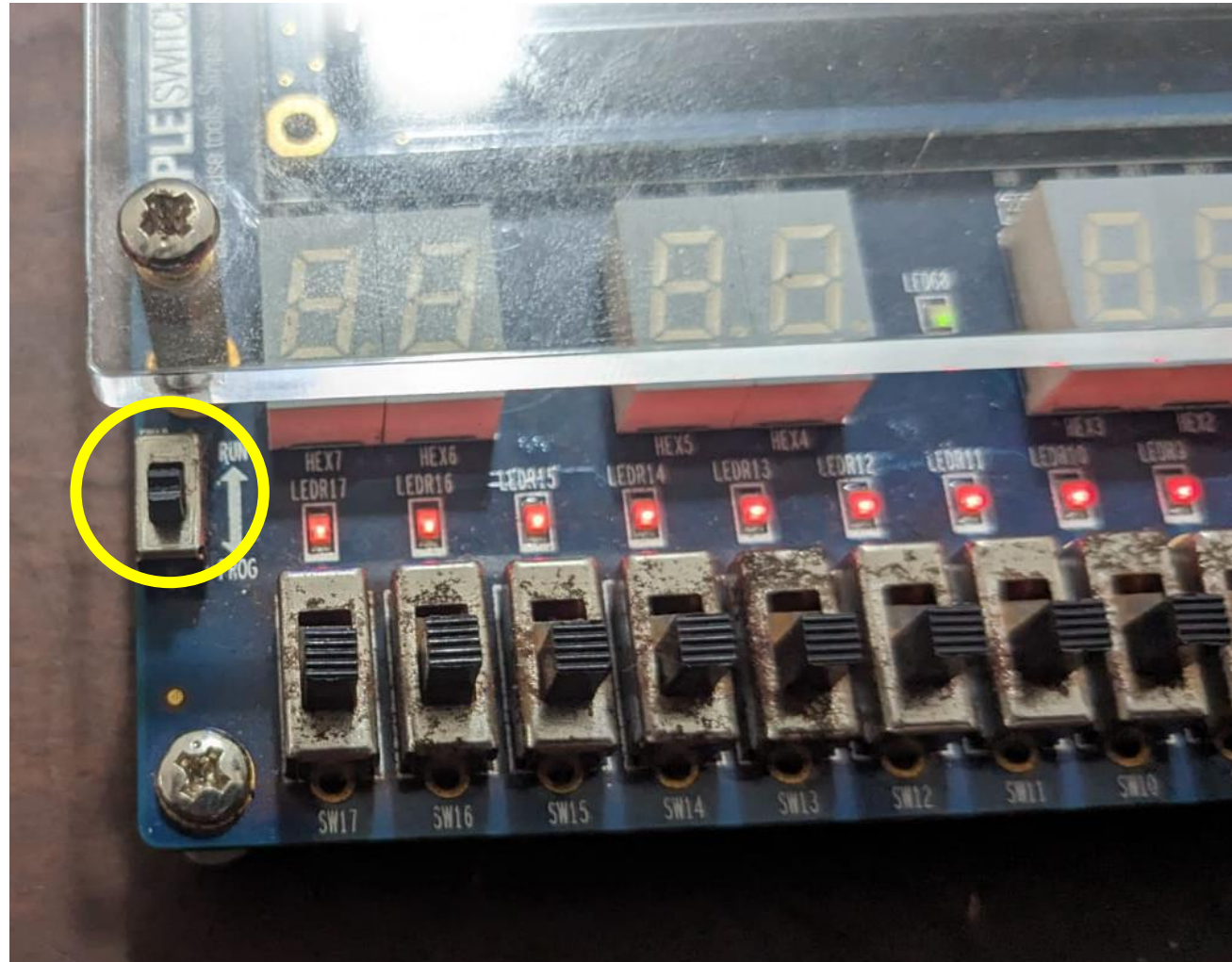
# Select “Auto Detect” if the board is NOT correctly selected.



# After selecting the board correctly, click “Start” to start uploading.



If the upload fails and this pin is in “PROG” mode, change it to “RUN” mode and press “Start”.

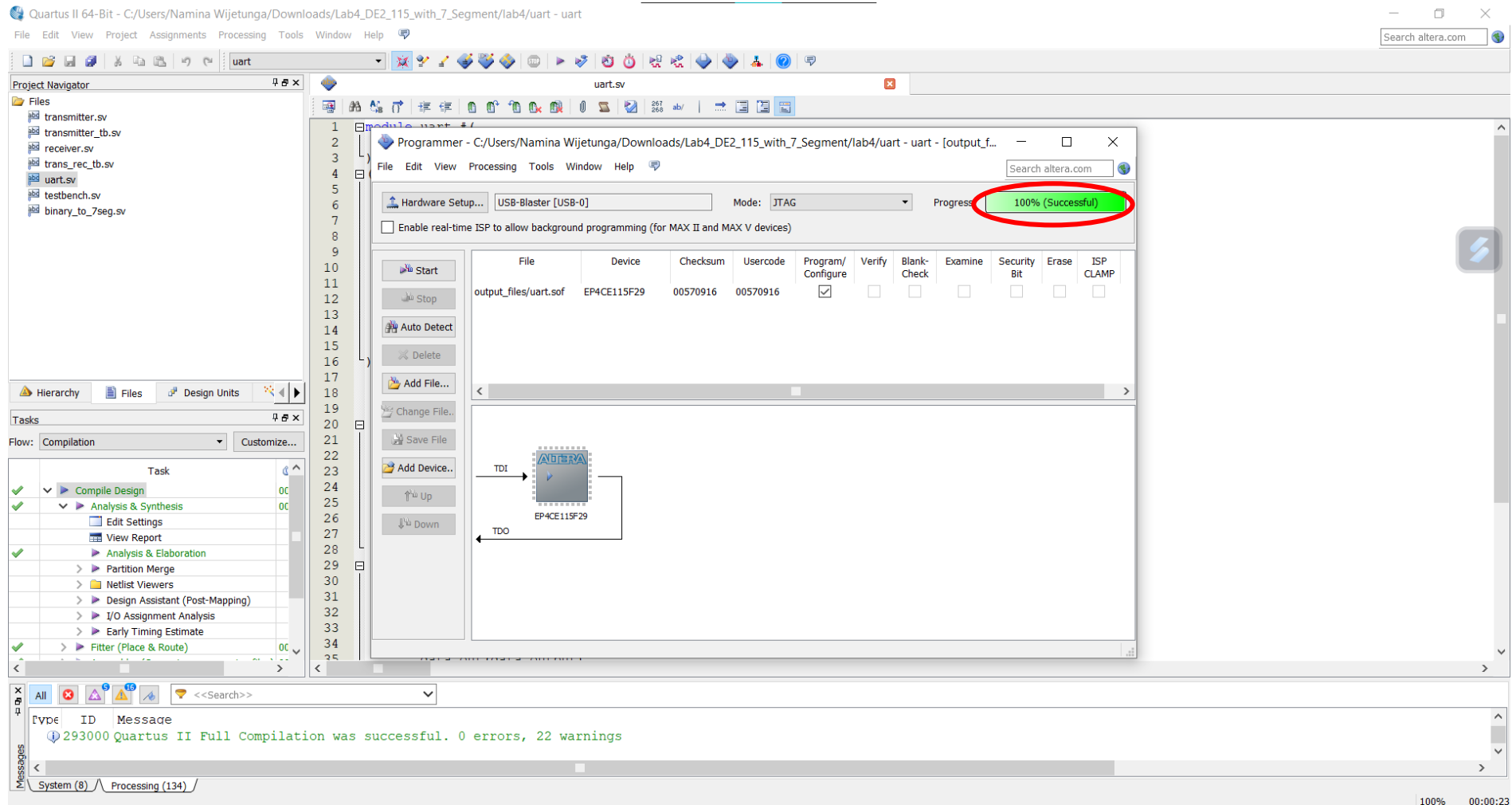




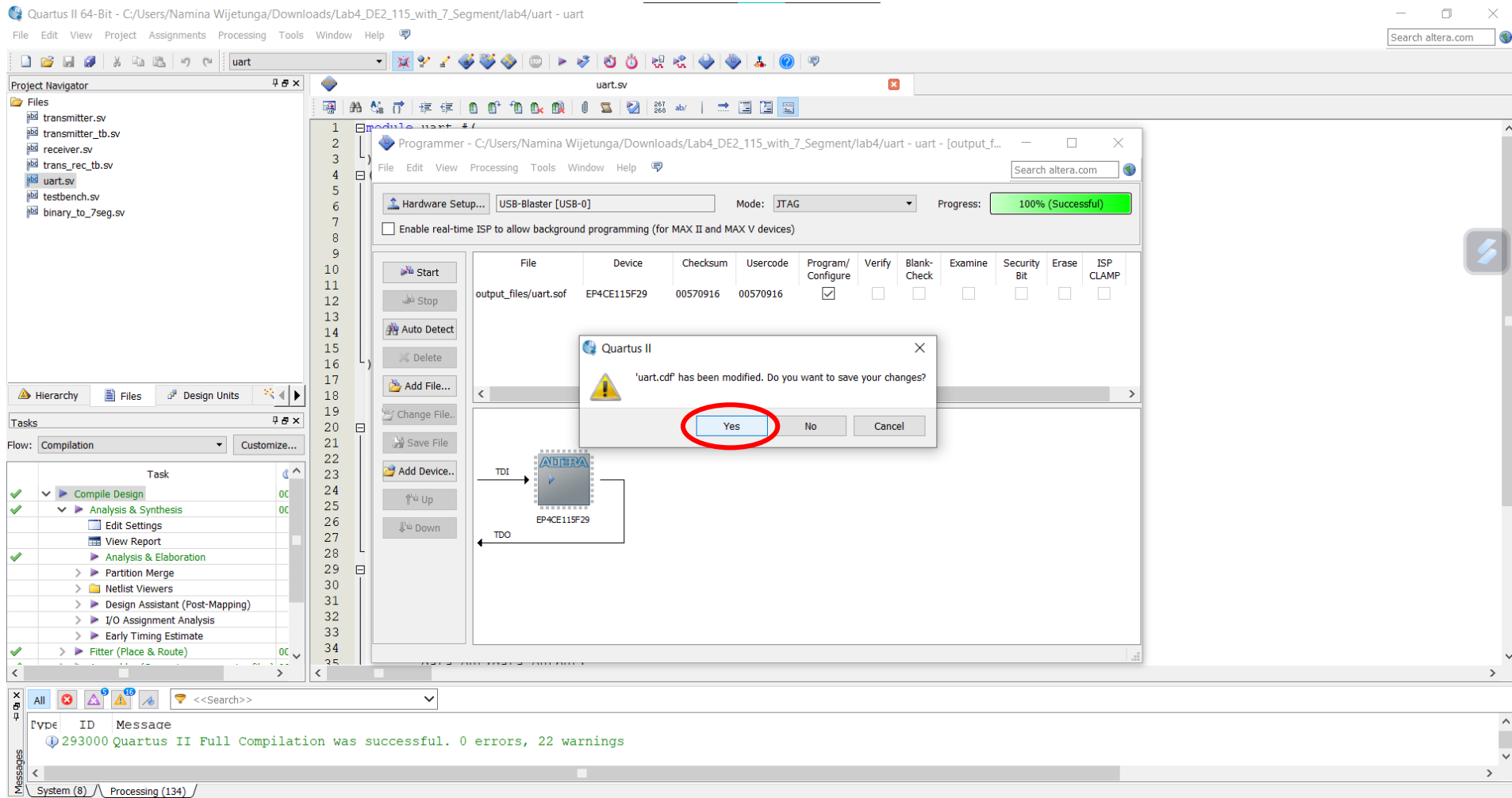
When uploading, the green LED near the blue power LED will glow.



# Once the upload is successful, the window will look like this.

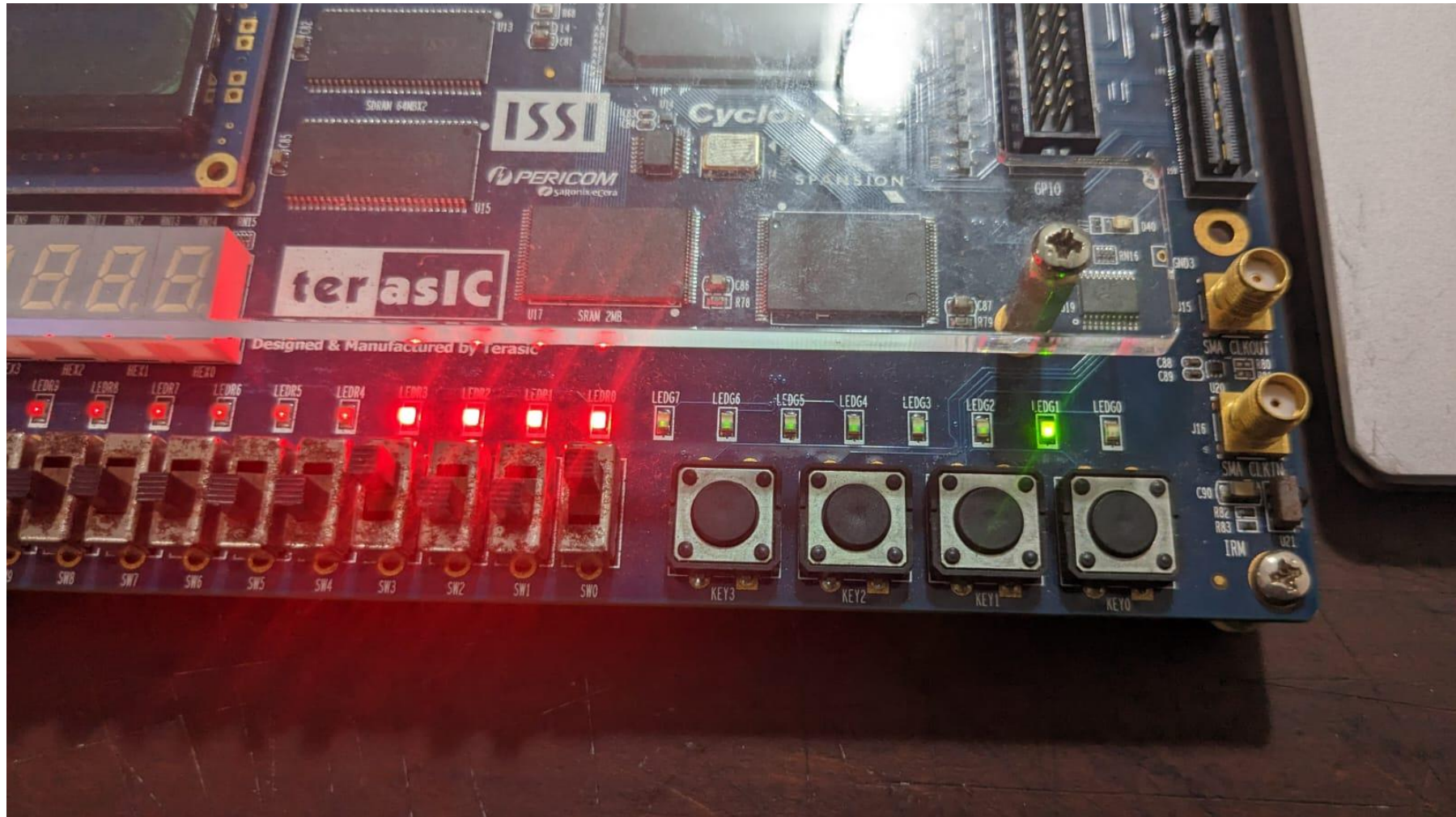


# Click “Yes”.

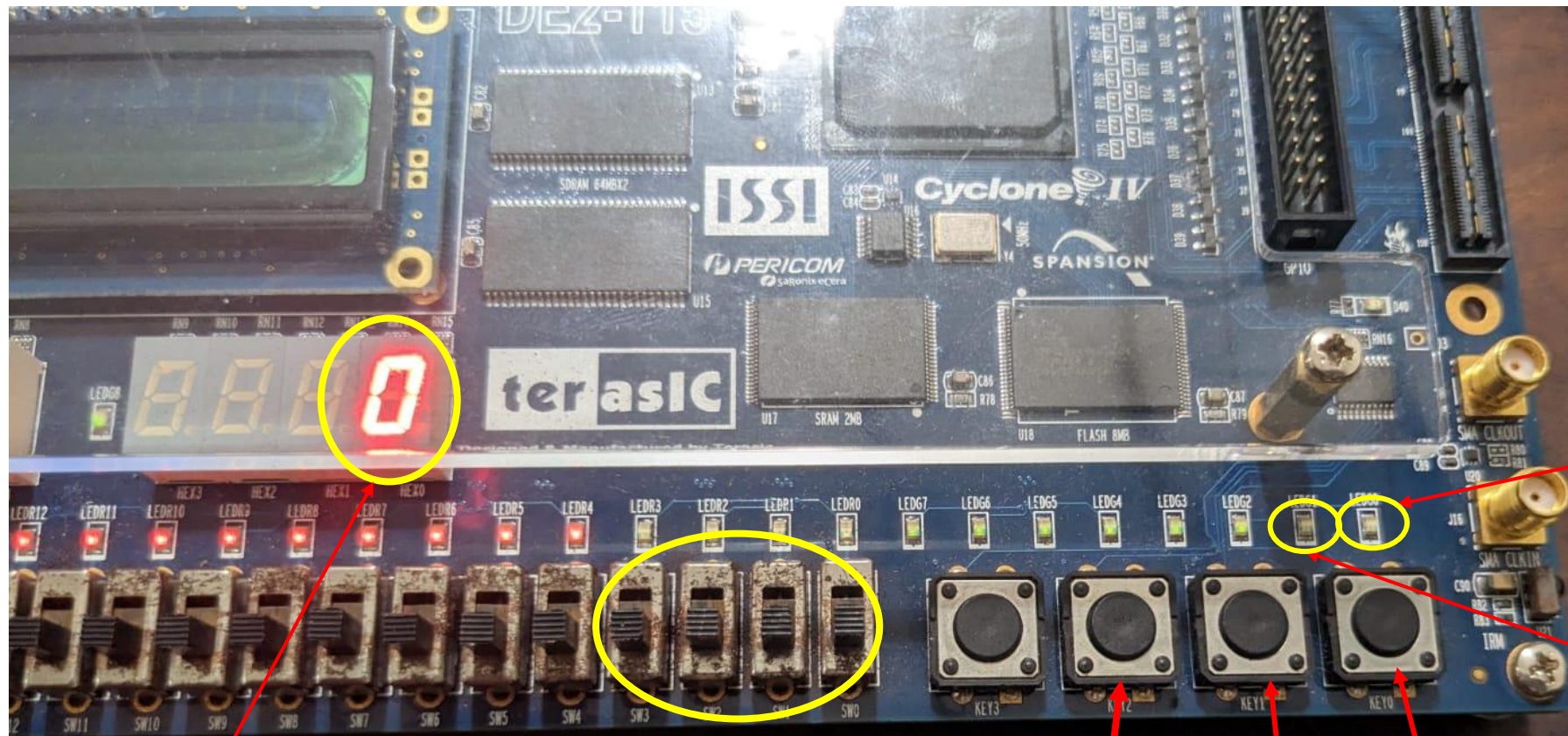




The Initial state of the board is as follows.



# Useful Buttons and Displays



7 Segment Display

SW3 SW2 SW1 SW0  
 $2^3$   $2^2$   $2^1$   $2^0$

Ready  
clear

Data  
Enable

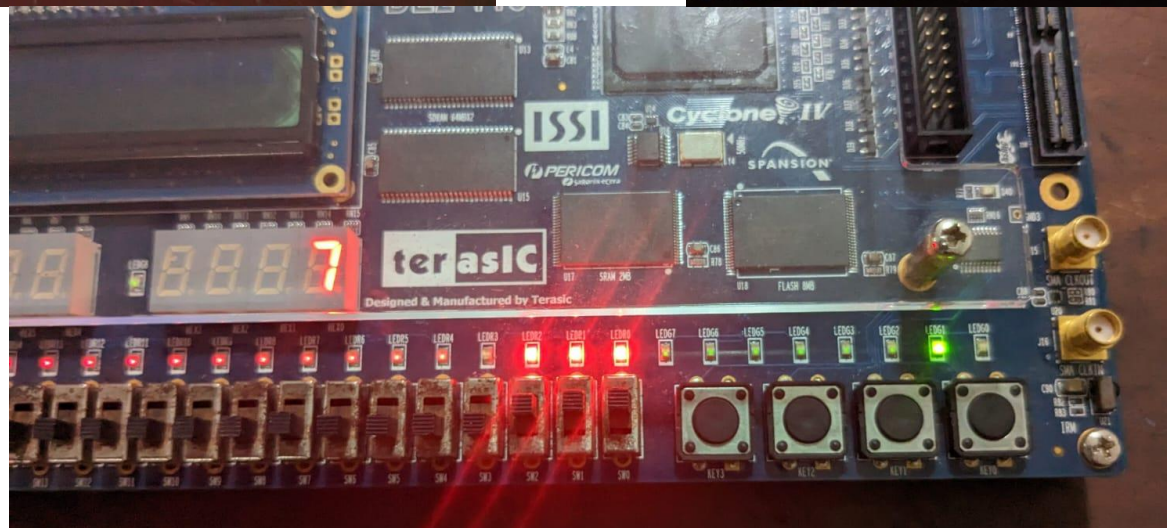
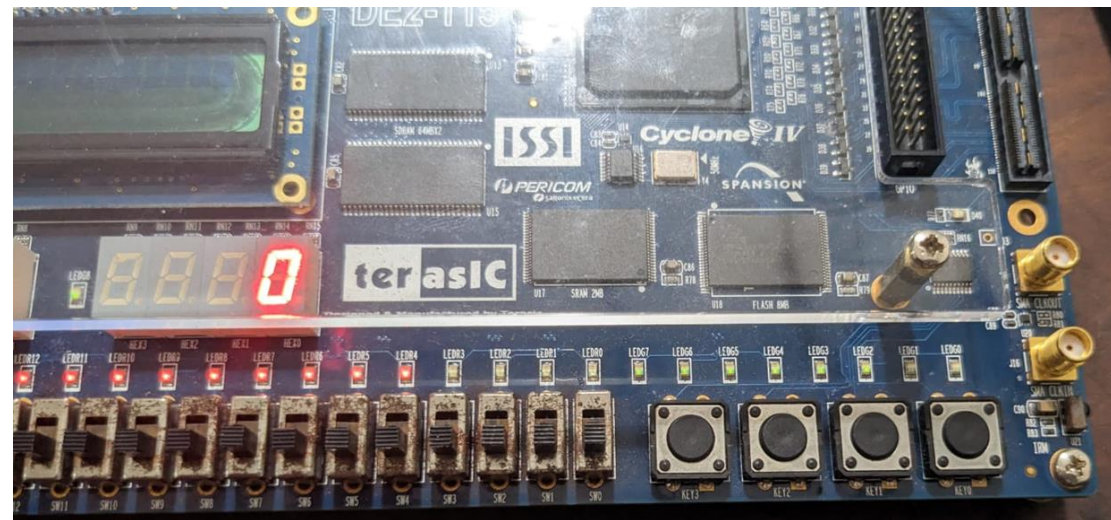
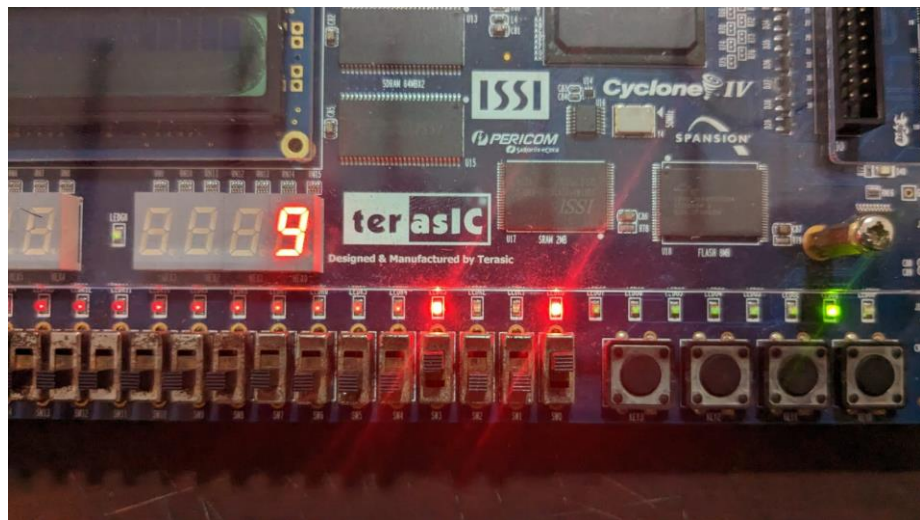
Reset

Tx busy

Output  
data  
valid



# Results



Thank You!