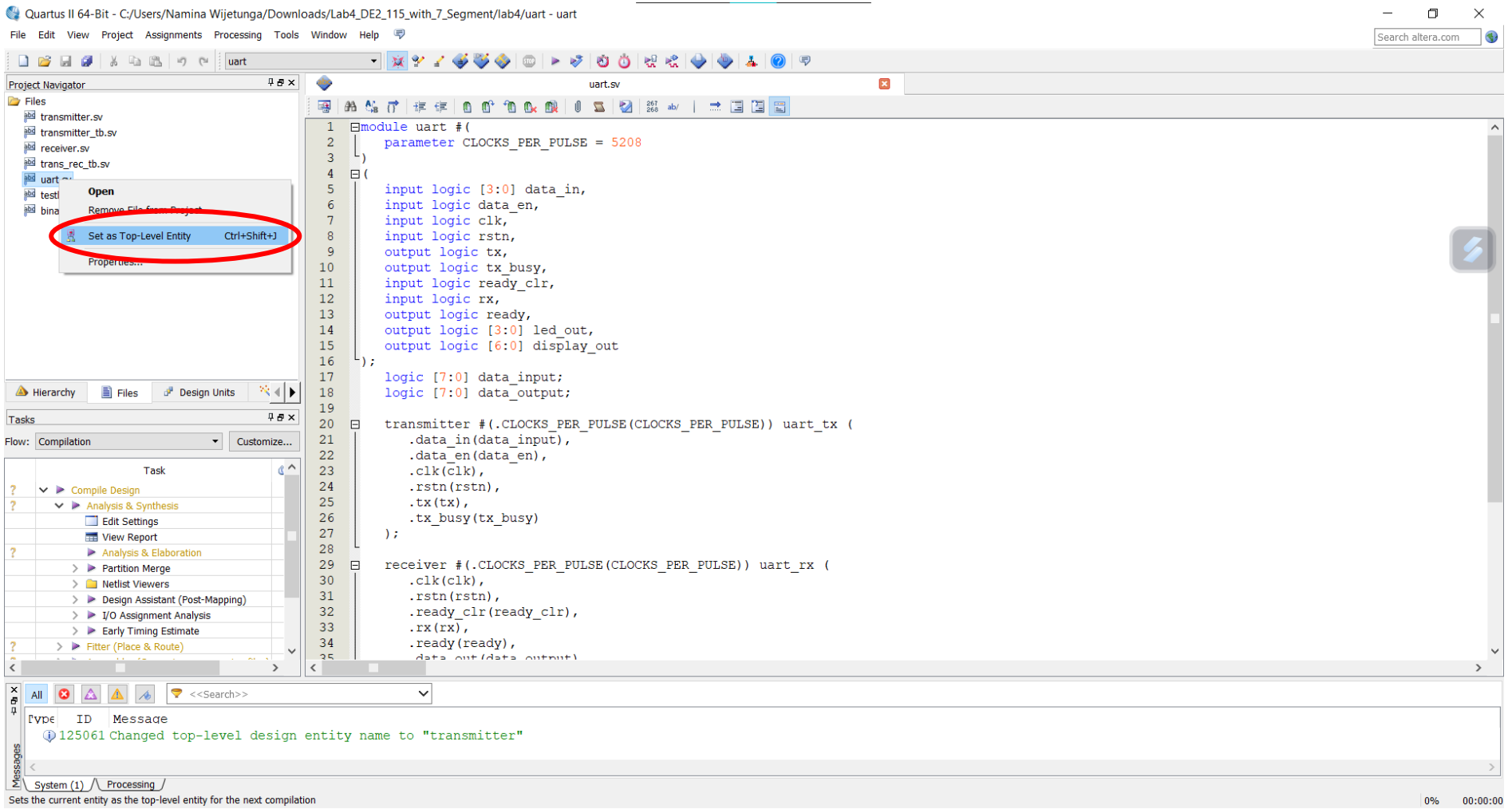
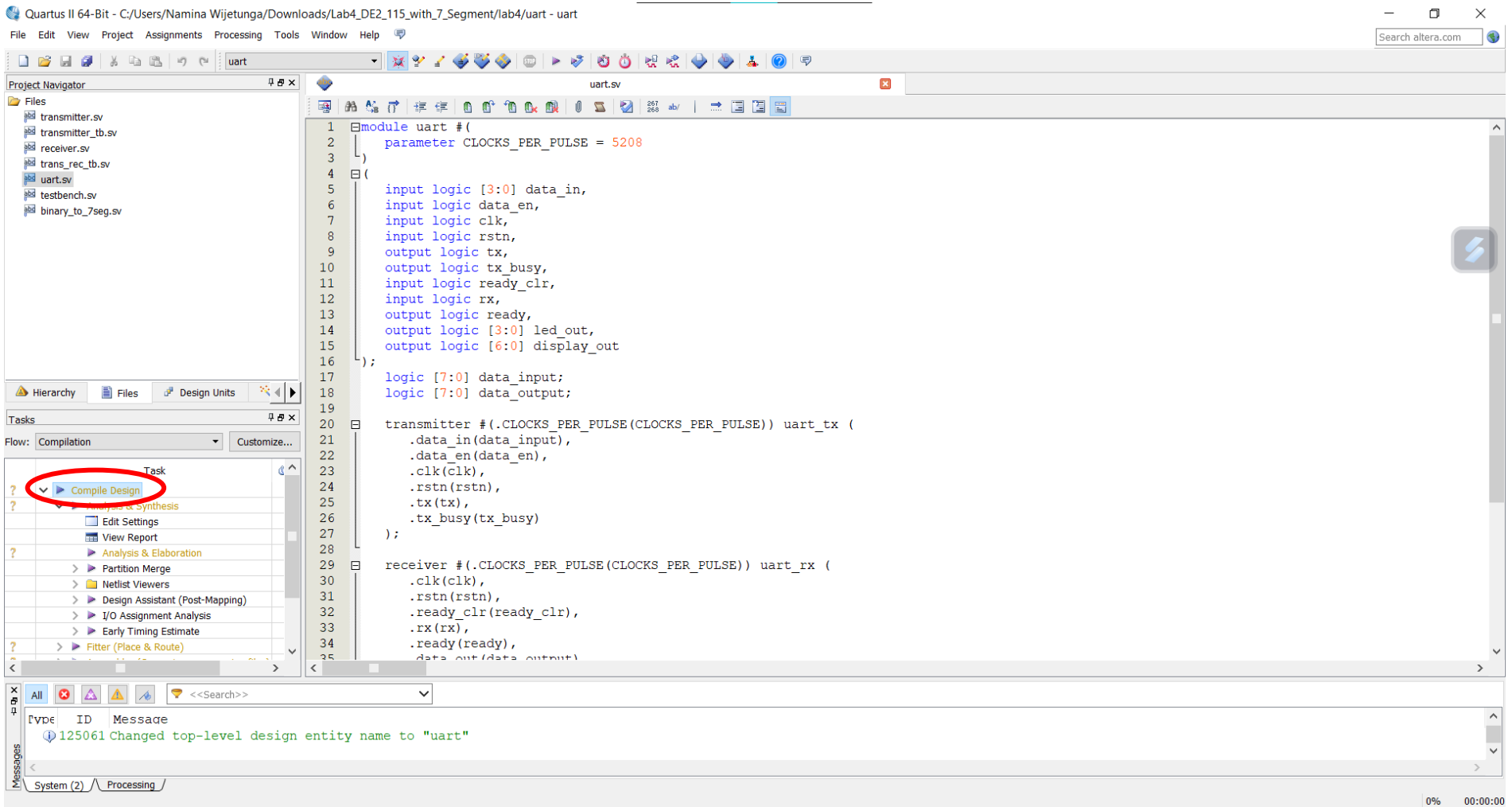
Uploading and Operating Guidelines

Altera DE2-115

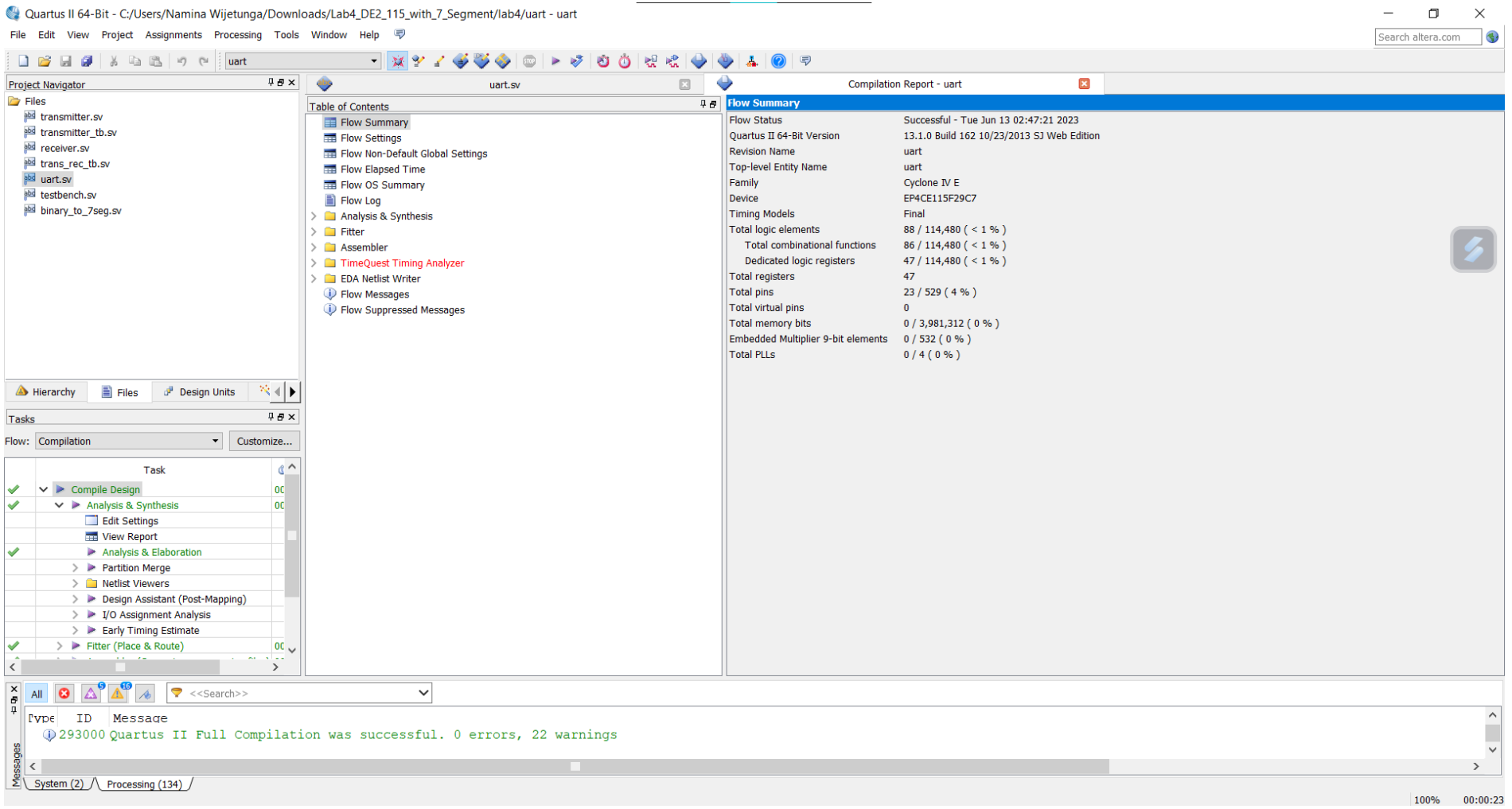
Select uart.sv file as the Top-Level Entity.



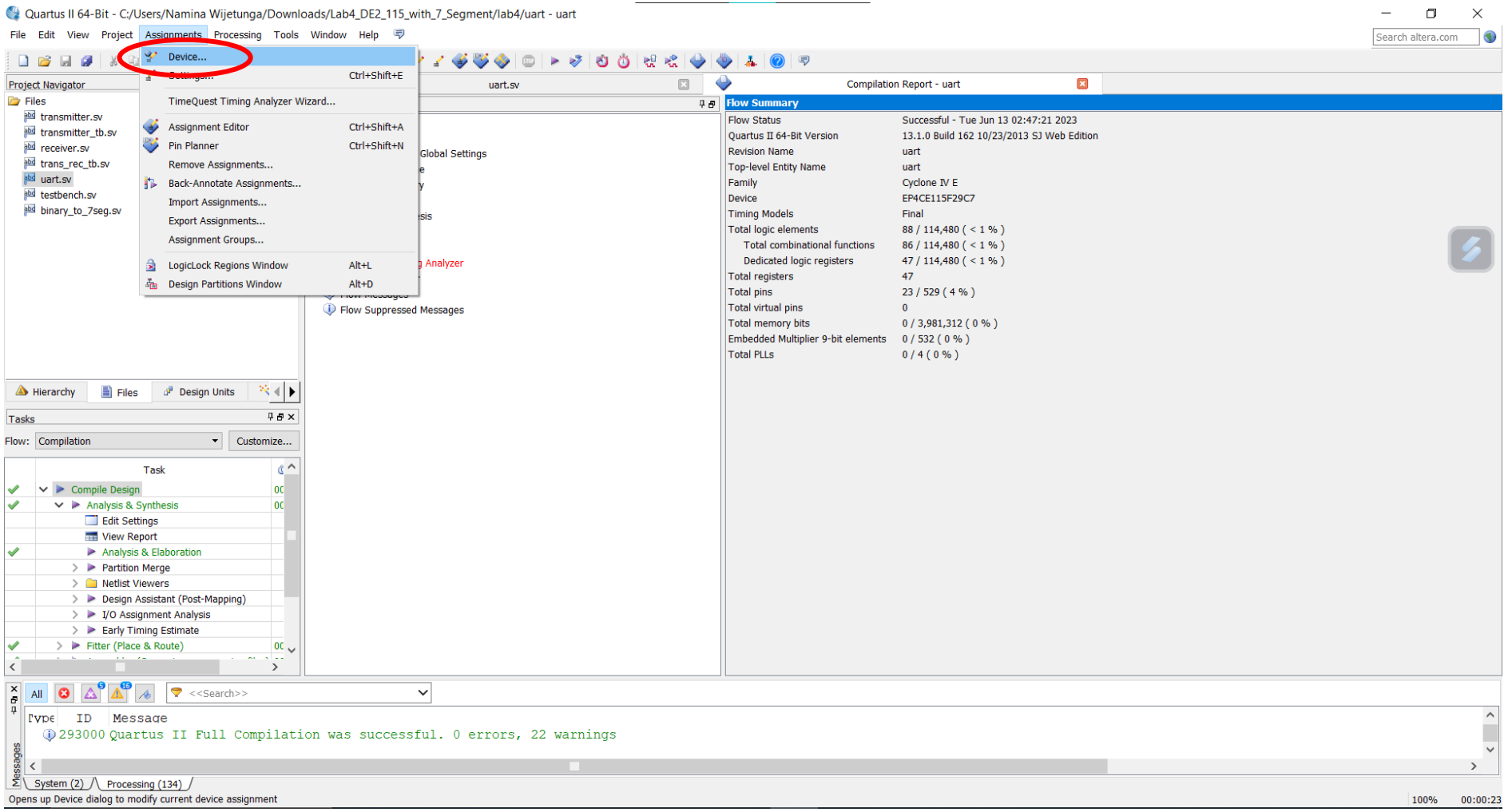
Double click on the “Compile Design” button.



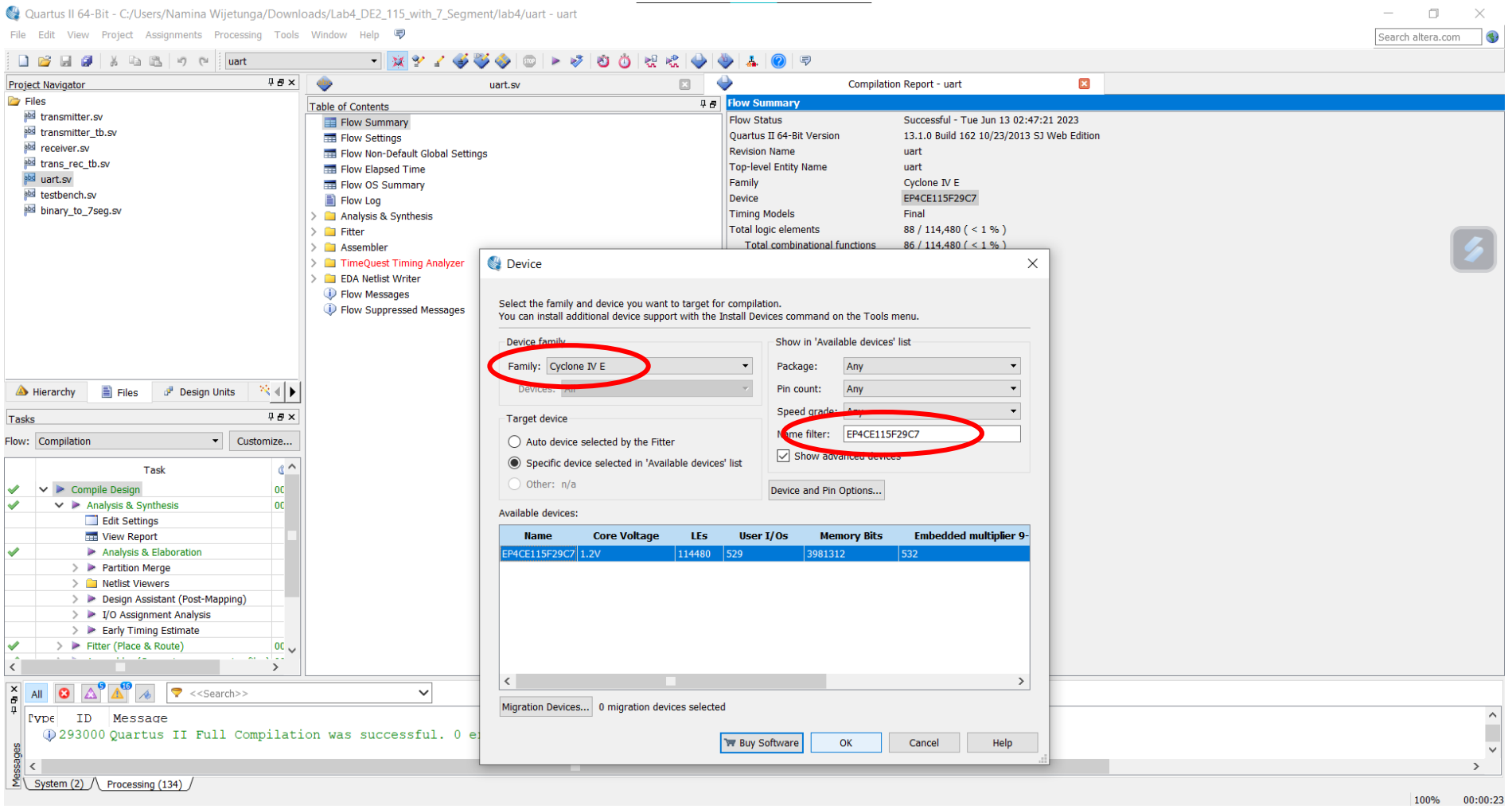
If the compilation is successful, the window will look like this.



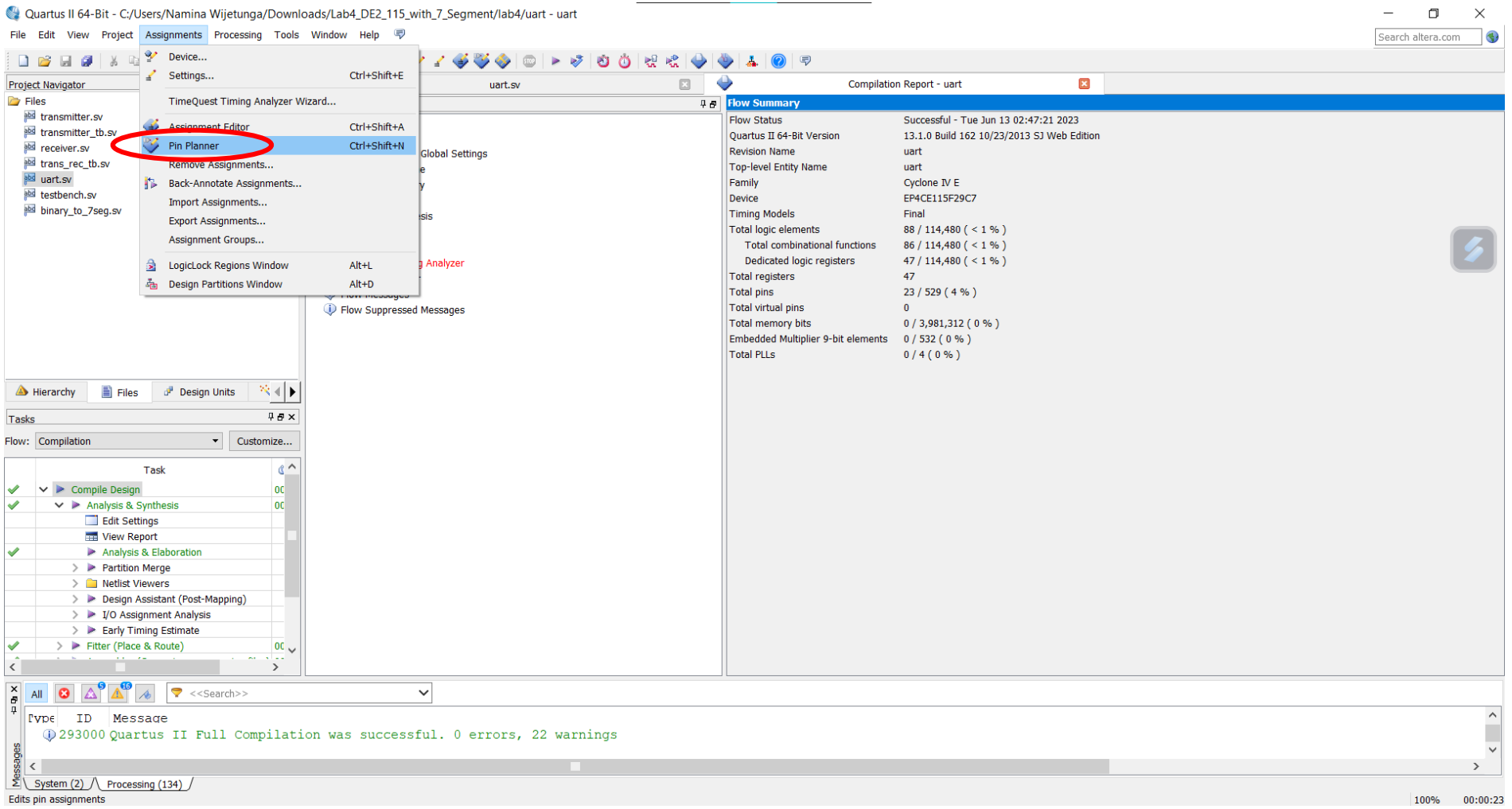
Go to “Assignments” tab and select “Device”.



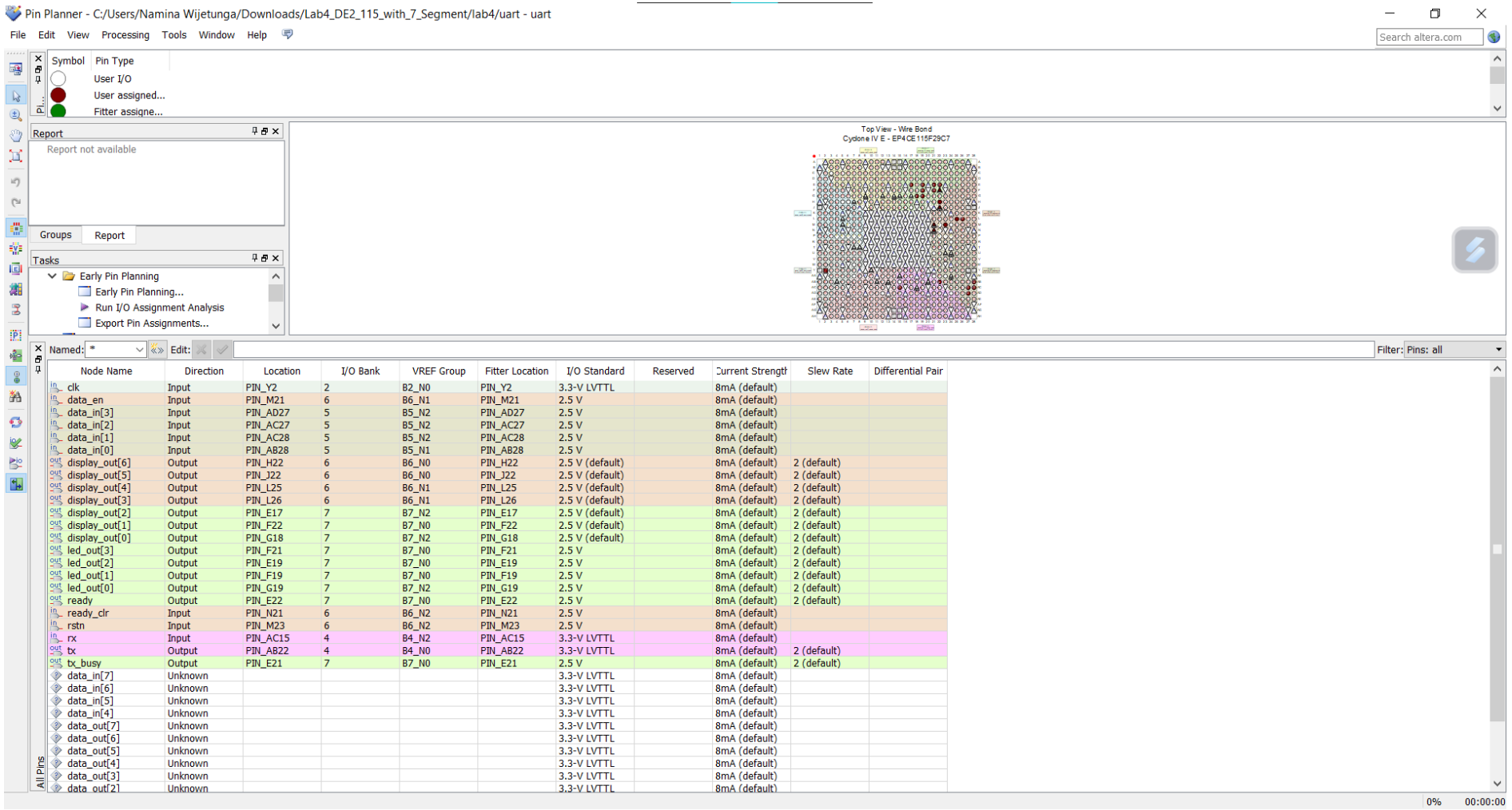
Make sure the device and family are selected correctly.



After successful completion of the device selection, go to “Pin Planner” under the same tab.

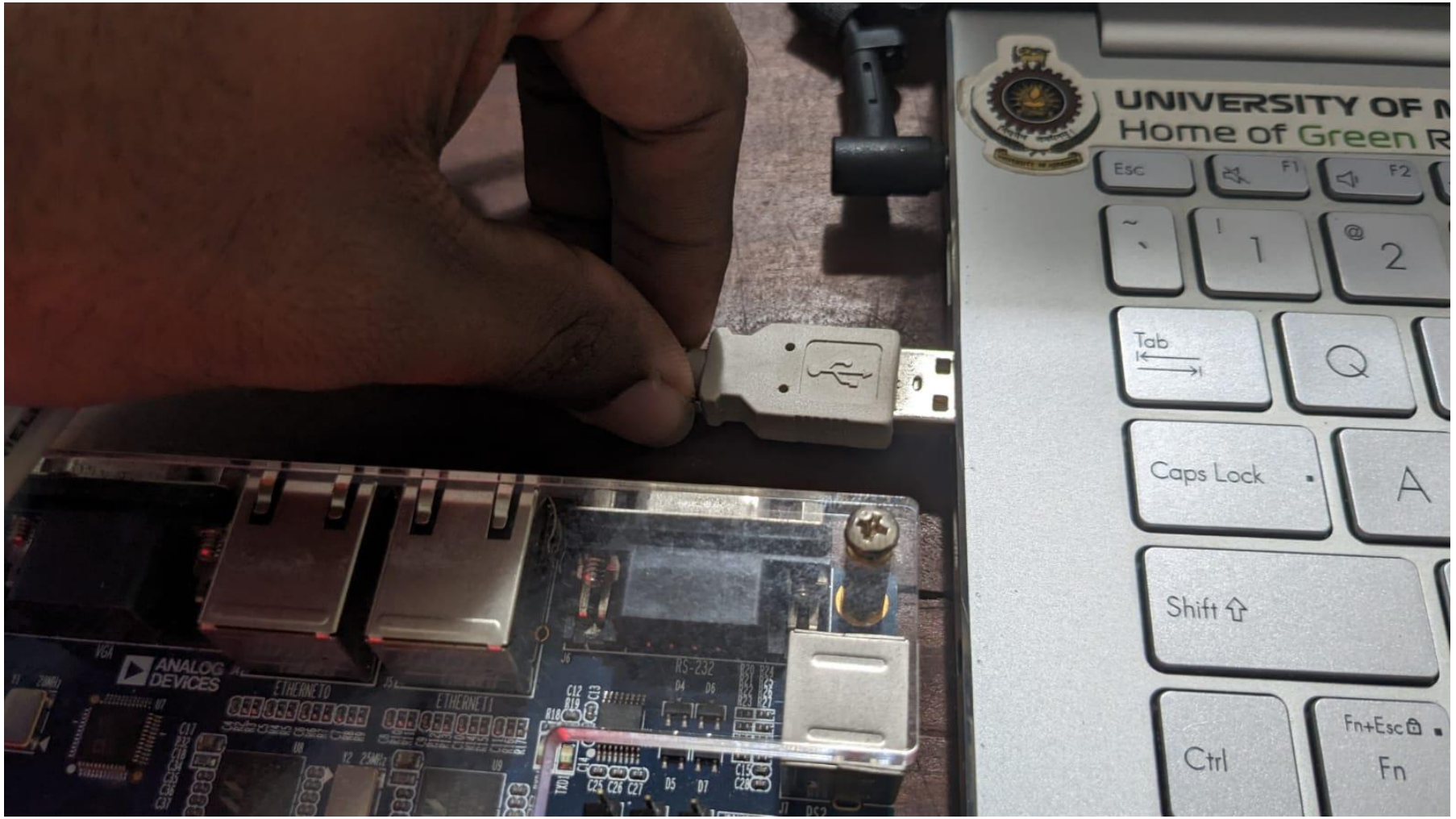


Assign the pins as follows.

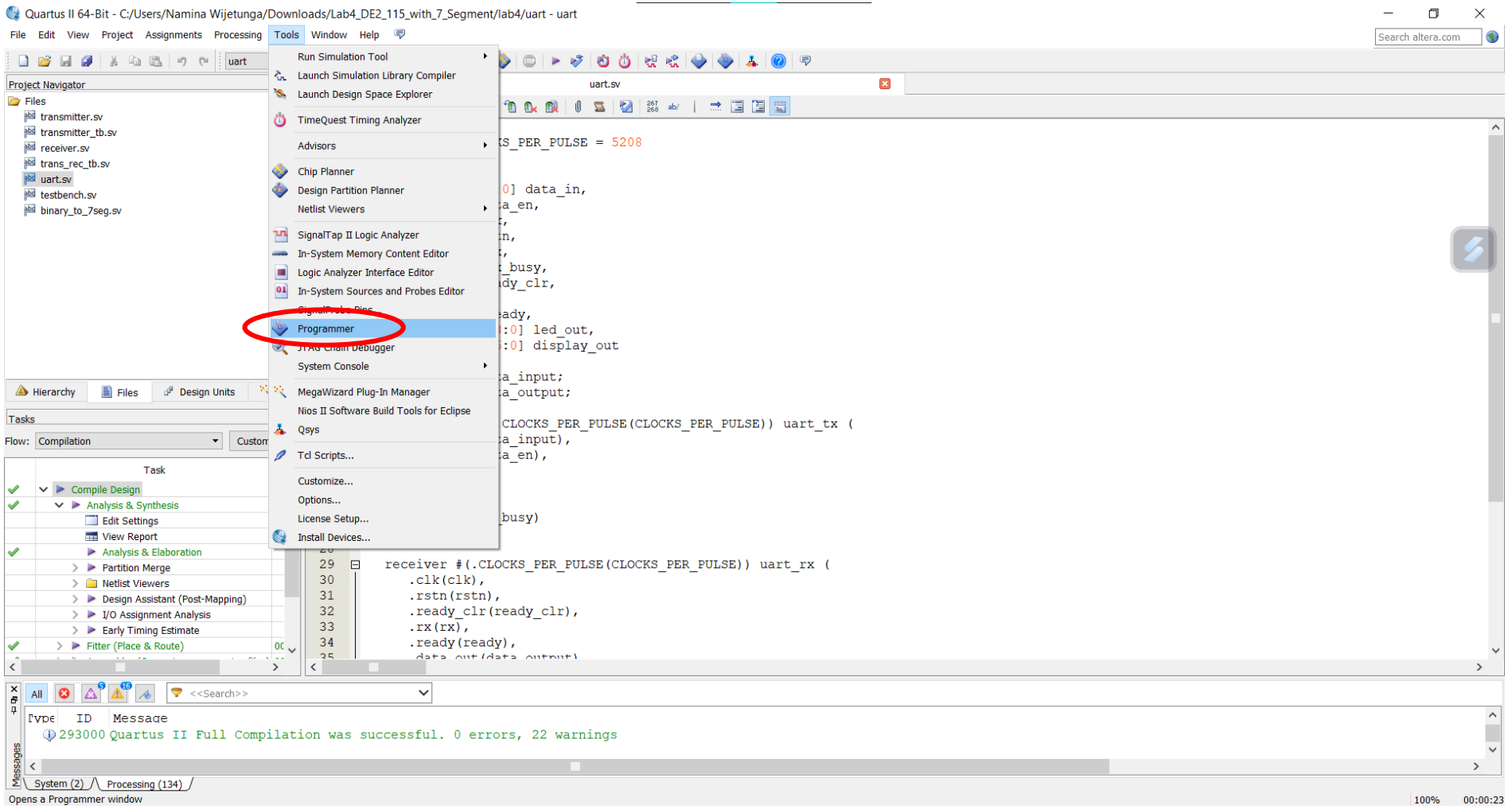


Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair
clk	Input	PIN_Y2	2	B2_N0	PIN_Y2	3.3-V LVTTL		8mA (default)		
data_en	Input	PIN_M21	6	B6_N1	PIN_M21	2.5 V		8mA (default)		
data_in[3]	Input	PIN_AD27	5	B5_N2	PIN_AD27	2.5 V		8mA (default)		
data_in[2]	Input	PIN_AC27	5	B5_N2	PIN_AC27	2.5 V		8mA (default)		
data_in[1]	Input	PIN_AC28	5	B5_N2	PIN_AC28	2.5 V		8mA (default)		
data_in[0]	Input	PIN_AB28	5	B5_N1	PIN_AB28	2.5 V		8mA (default)		
display_out[6]	Output	PIN_H22	6	B6_N0	PIN_H22	2.5 V (default)		8mA (default)	2 (default)	
display_out[5]	Output	PIN_J22	6	B6_N0	PIN_J22	2.5 V (default)		8mA (default)	2 (default)	
display_out[4]	Output	PIN_L25	6	B6_N1	PIN_L25	2.5 V (default)		8mA (default)	2 (default)	
display_out[3]	Output	PIN_L26	6	B6_N1	PIN_L26	2.5 V (default)		8mA (default)	2 (default)	
display_out[2]	Output	PIN_E17	7	B7_N2	PIN_E17	2.5 V (default)		8mA (default)	2 (default)	
display_out[1]	Output	PIN_F22	7	B7_N0	PIN_F22	2.5 V (default)		8mA (default)	2 (default)	
display_out[0]	Output	PIN_G18	7	B7_N2	PIN_G18	2.5 V (default)		8mA (default)	2 (default)	
led_out[3]	Output	PIN_F21	7	B7_N0	PIN_F21	2.5 V		8mA (default)	2 (default)	
led_out[2]	Output	PIN_E19	7	B7_N0	PIN_E19	2.5 V		8mA (default)	2 (default)	
led_out[1]	Output	PIN_F19	7	B7_N0	PIN_F19	2.5 V		8mA (default)	2 (default)	
led_out[0]	Output	PIN_G19	7	B7_N2	PIN_G19	2.5 V		8mA (default)	2 (default)	
ready	Output	PIN_E22	7	B7_N0	PIN_E22	2.5 V		8mA (default)	2 (default)	
ready_clr	Input	PIN_N21	6	B6_N2	PIN_N21	2.5 V		8mA (default)		
rstn	Input	PIN_M23	6	B6_N2	PIN_M23	2.5 V		8mA (default)		
rx	Input	PIN_AC15	4	B4_N2	PIN_AC15	3.3-V LVTTL		8mA (default)		
tx	Output	PIN_AB22	4	B4_N0	PIN_AB22	3.3-V LVTTL		8mA (default)	2 (default)	
tx_busy	Output	PIN_E21	7	B7_N0	PIN_E21	2.5 V		8mA (default)	2 (default)	
data_in[7]	Unknown					3.3-V LVTTL		8mA (default)		
data_in[6]	Unknown					3.3-V LVTTL		8mA (default)		
data_in[5]	Unknown					3.3-V LVTTL		8mA (default)		
data_in[4]	Unknown					3.3-V LVTTL		8mA (default)		
data_out[7]	Unknown					3.3-V LVTTL		8mA (default)		
data_out[6]	Unknown					3.3-V LVTTL		8mA (default)		
data_out[5]	Unknown					3.3-V LVTTL		8mA (default)		
data_out[4]	Unknown					3.3-V LVTTL		8mA (default)		
data_out[3]	Unknown					3.3-V LVTTL		8mA (default)		
data_out[2]	Unknown					3.3-V LVTTL		8mA (default)		

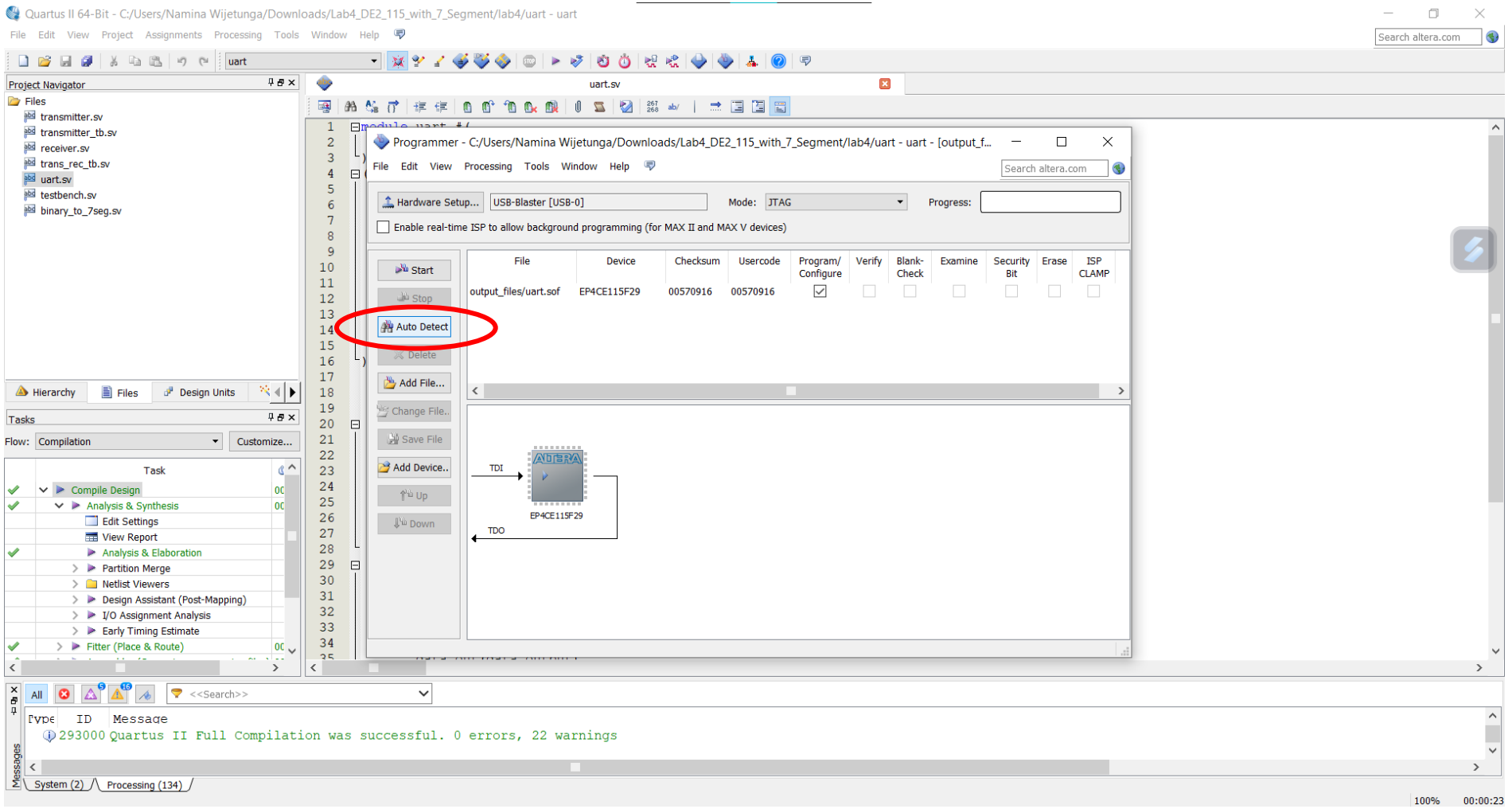
Connect the DE2-115 board to the PC.



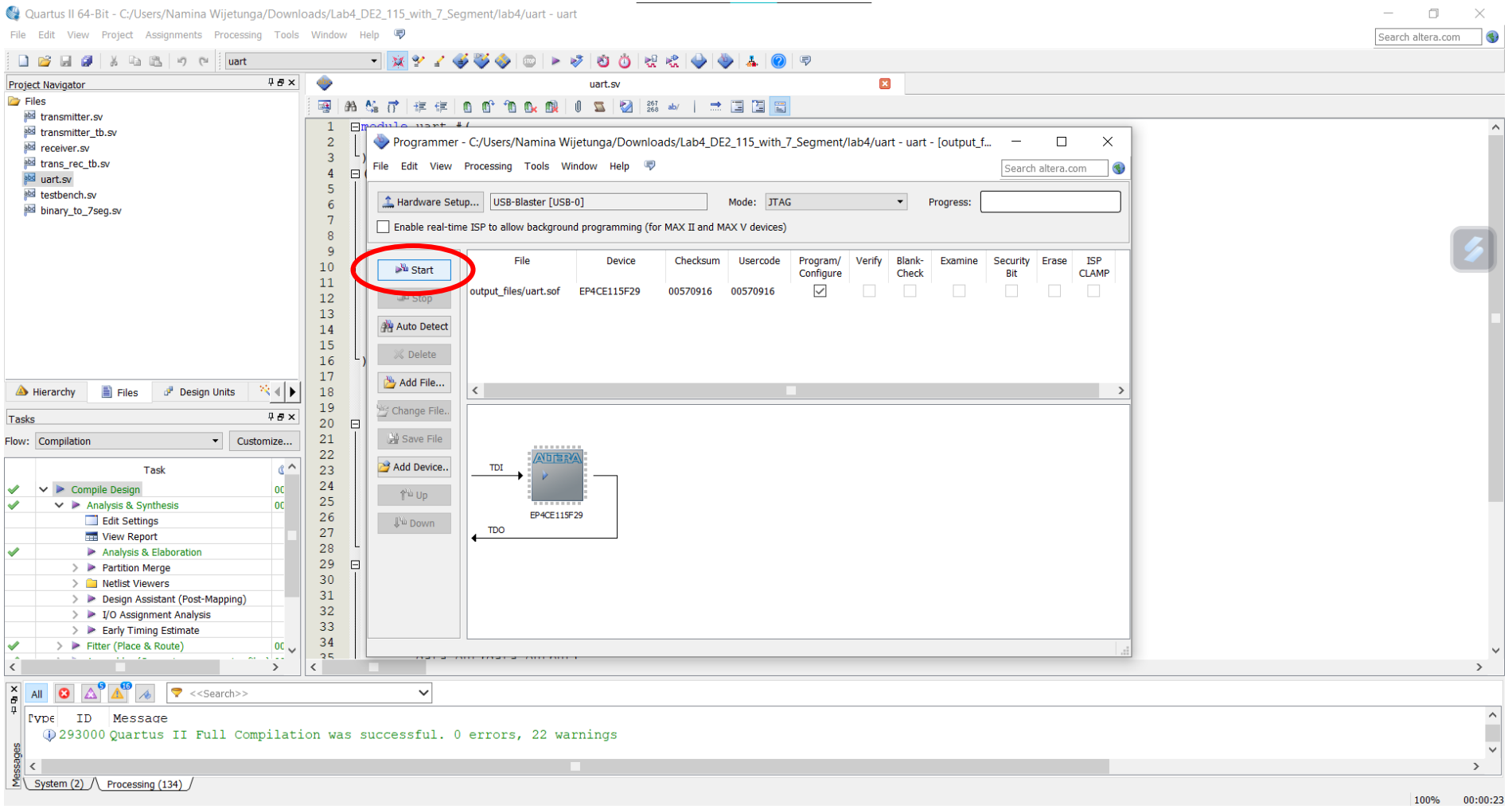
Go to “Tools” tab and select “Programmer”.



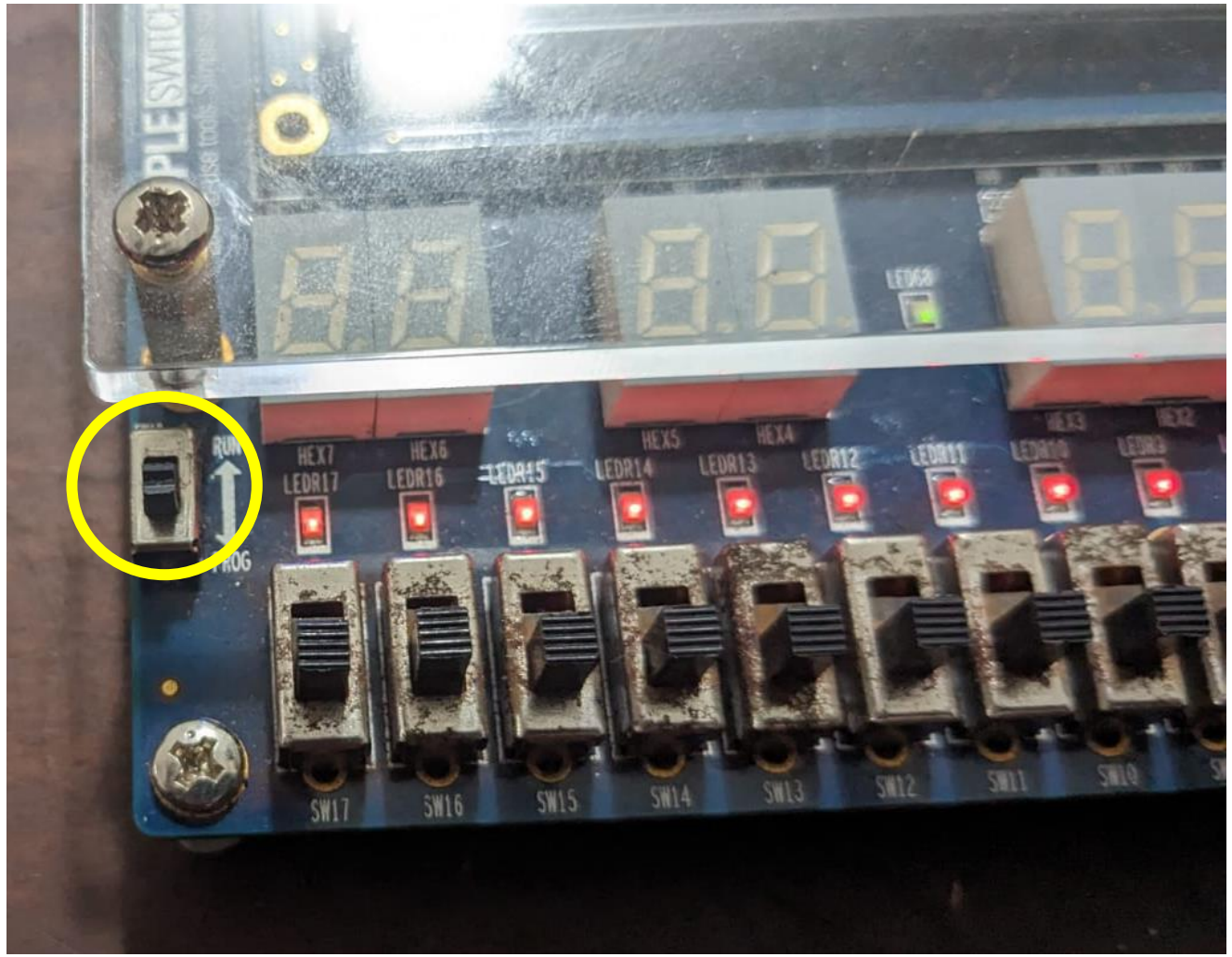
Select “Auto Detect” if the board is NOT correctly selected.



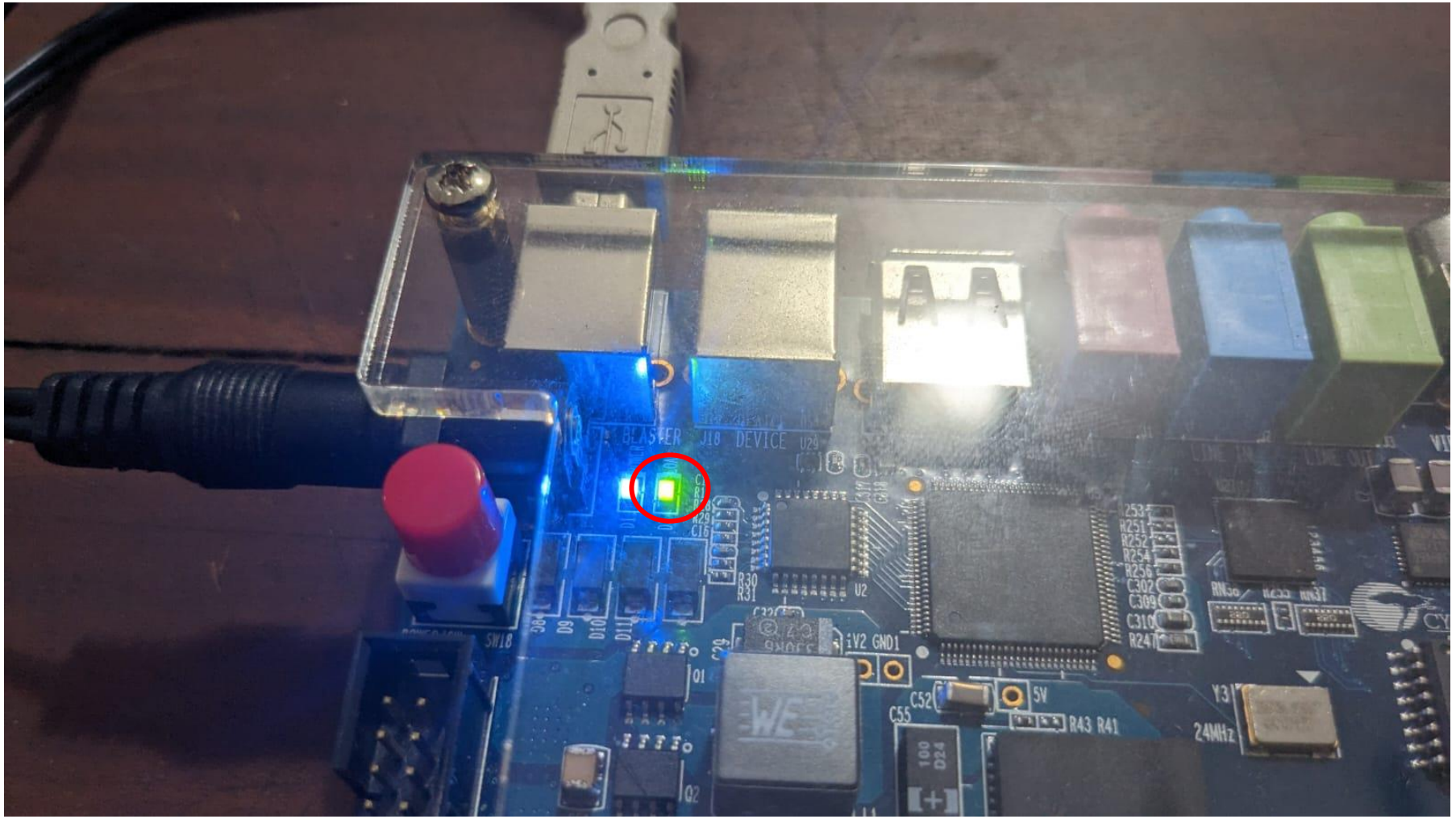
After selecting the board correctly, click “Start” to start uploading.



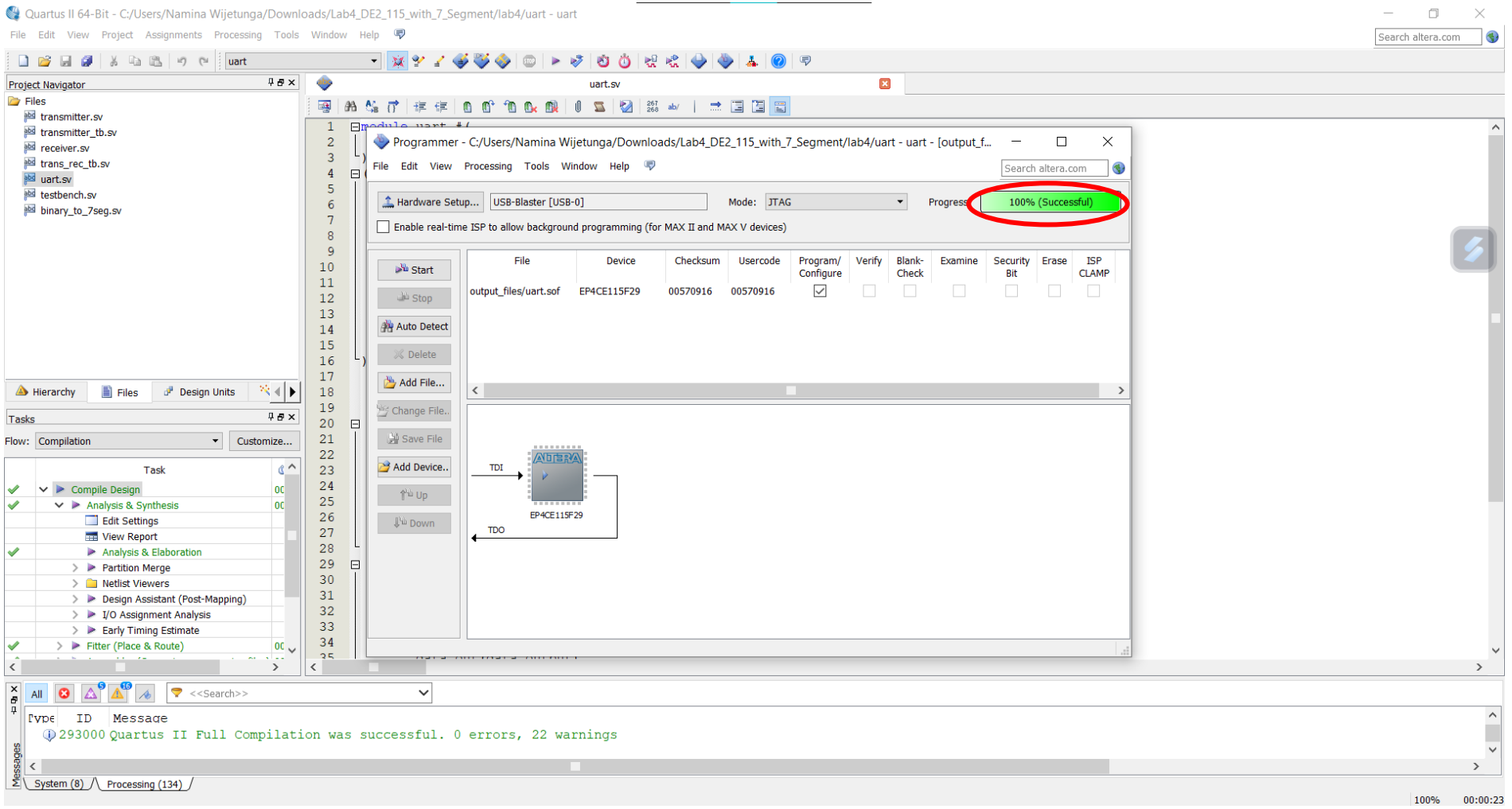
If the upload fails and this pin is in “PROG” mode, change it to “RUN” mode and press “Start”.



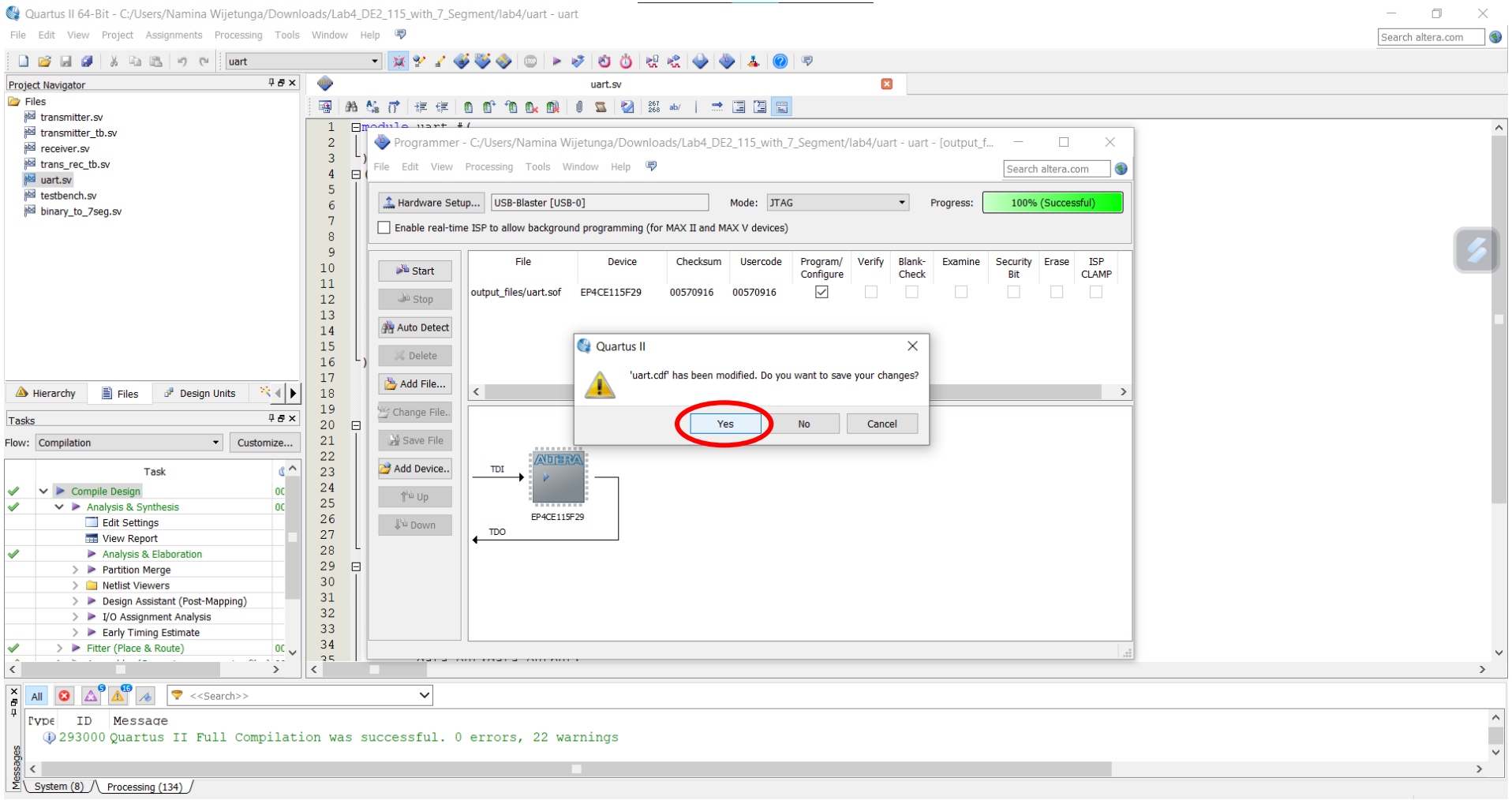
When uploading, the green LED near the blue power LED will glow.



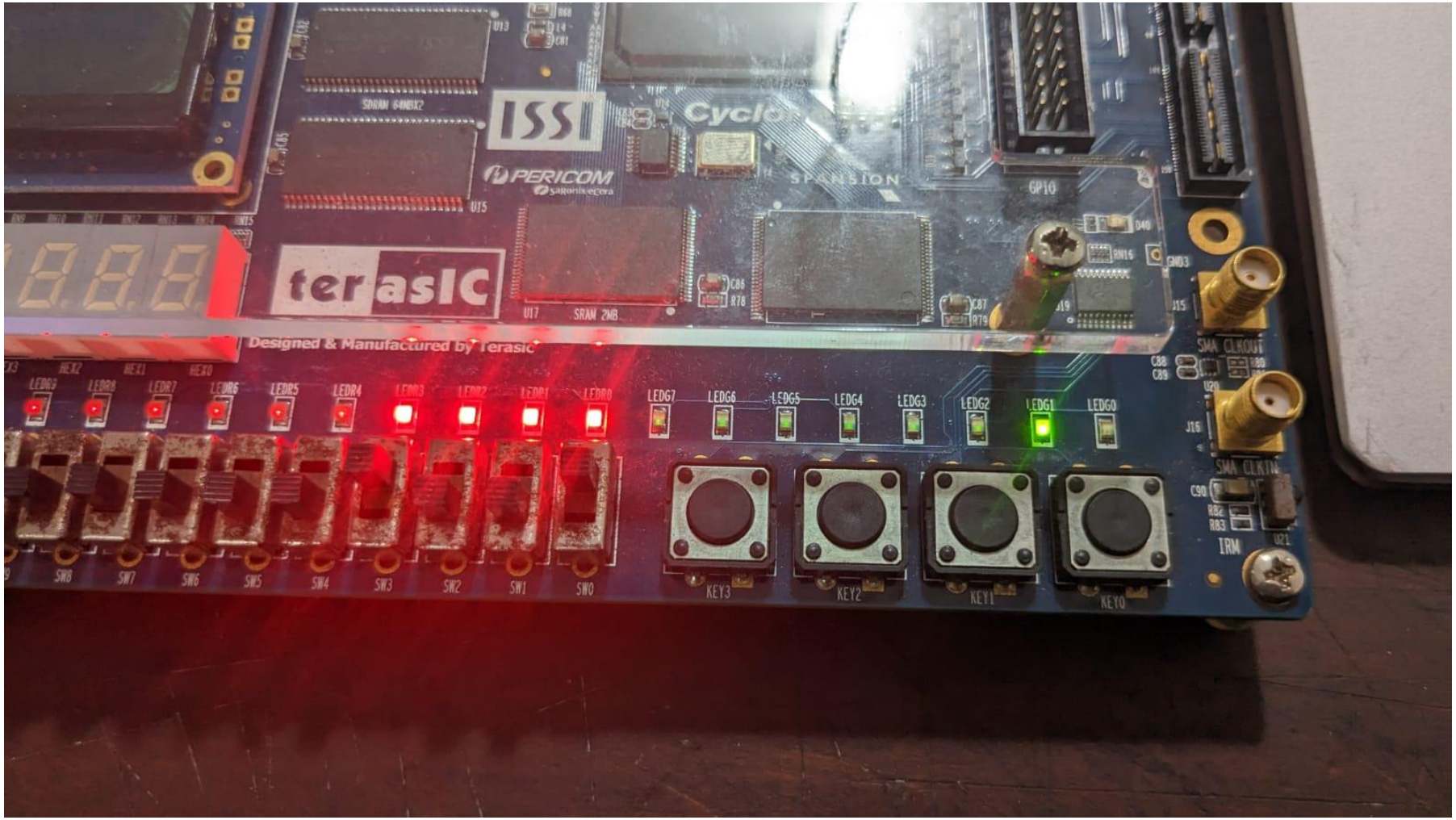
Once the upload is successful, the window will look like this.



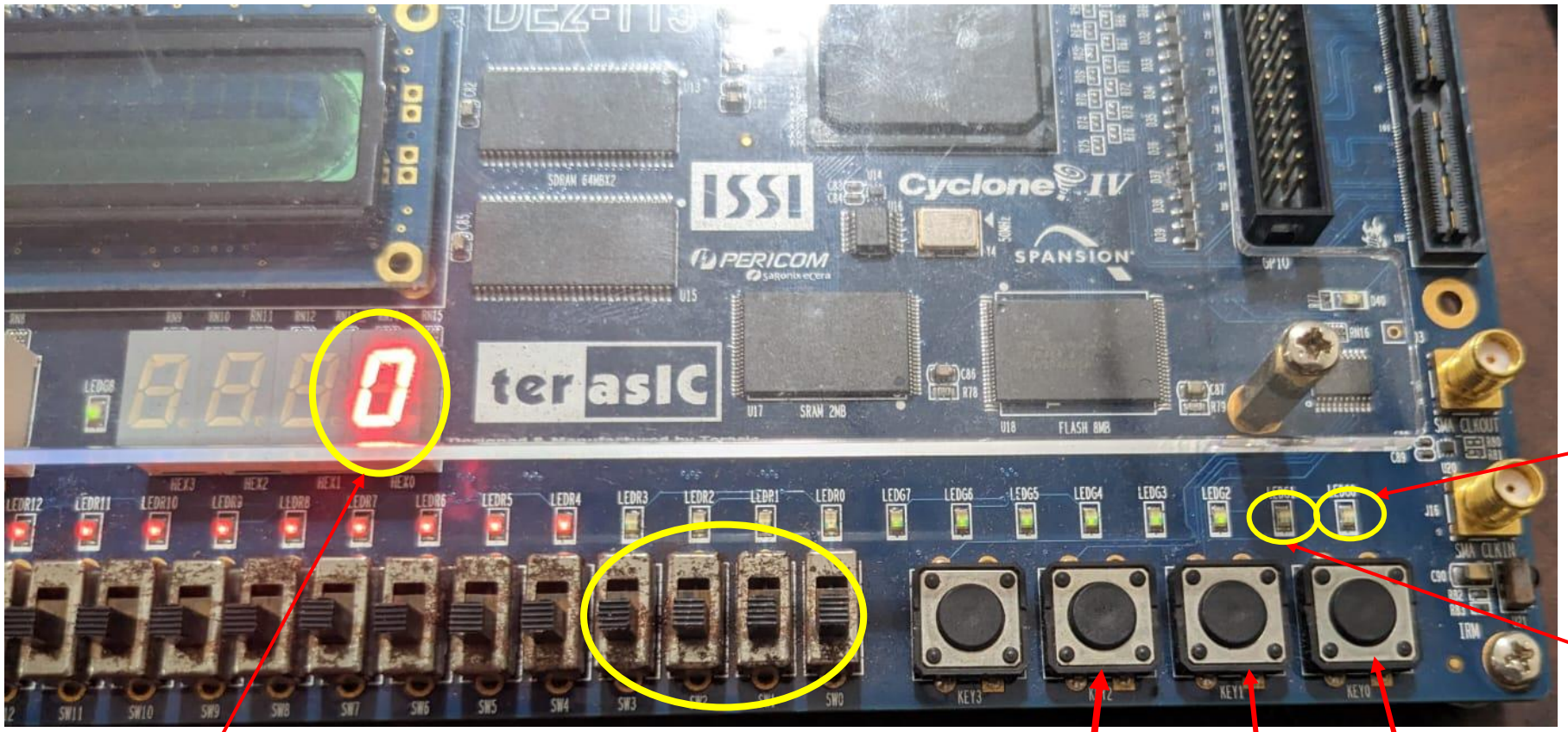
Click “Yes”.


Quartus II 64-Bit - C:/Users/Namina Wijetunga/Downloads/Lab4_DE2_115_with_7_Segment/lab4/uart - uart
Programmer - C:/Users/Namina Wijetunga/Downloads/Lab4_DE2_115_with_7_Segment/lab4/uart - uart - [output_f...
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
100% (Successful)
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
Erase
ISP CLAMP
output_files/uart.sof
EP4CE115F29
00570916
00570916
Quartus II
'uart.cdf' has been modified. Do you want to save your changes?
Yes
No
Cancel
TDI
TDO
EP4CE115F29
Project Navigator
Files
transmitter.sv
transmitter_tb.sv
receiver.sv
trans_rec_tb.sv
uart.sv
testbench.sv
binary_to_7seg.sv
Tasks
Flow: Compilation
Customize...
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
Design Assistant (Post-Mapping)
I/O Assignment Analysis
Early Timing Estimate
Fitter (Place & Route)
293000 Quartus II Full Compilation was successful. 0 errors, 22 warnings
System (8)
Processing (134)

The Initial state of the board is as follows.



Useful Buttons and Displays



Tx busy

Output data valid

7 Segment Display

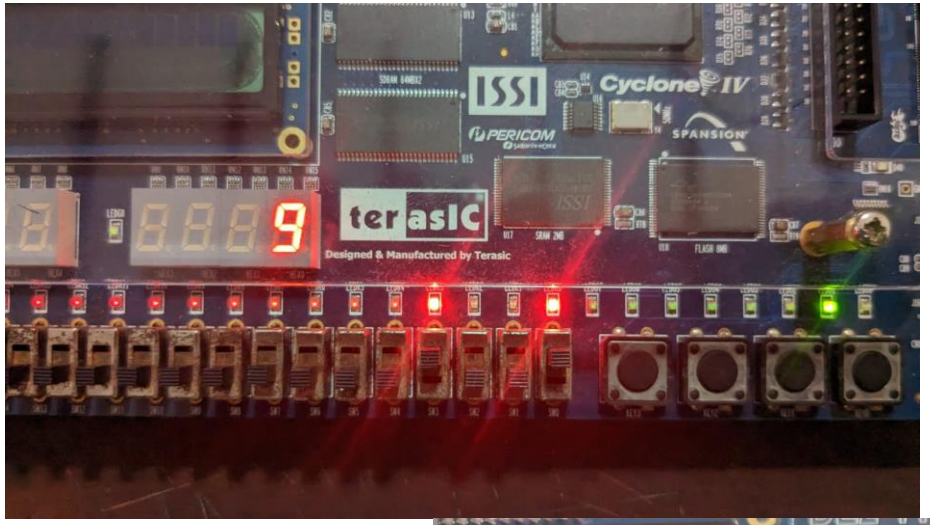
SW3 SW2 SW1 SW0
2^3 2^2 2^1 2^0

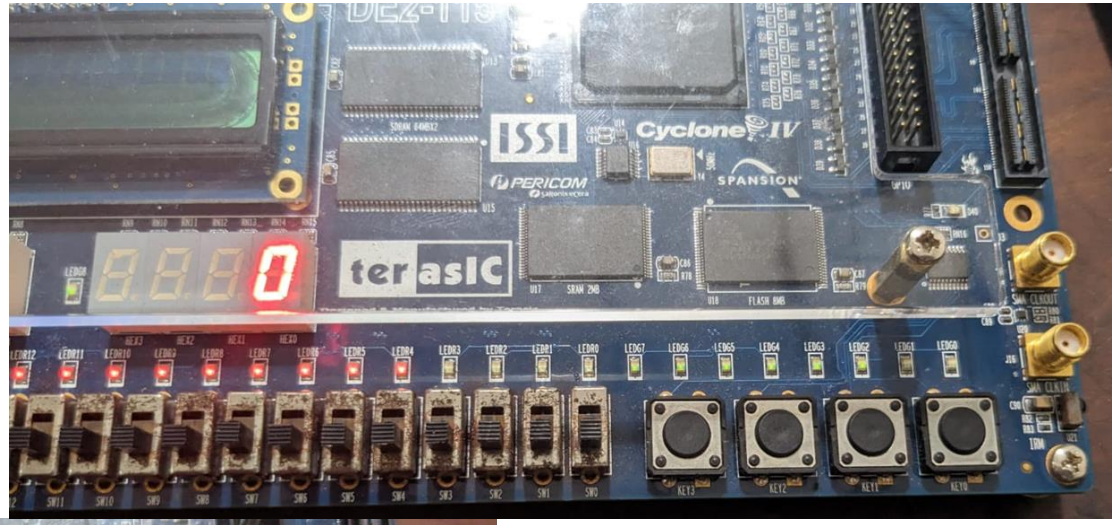
Ready clear

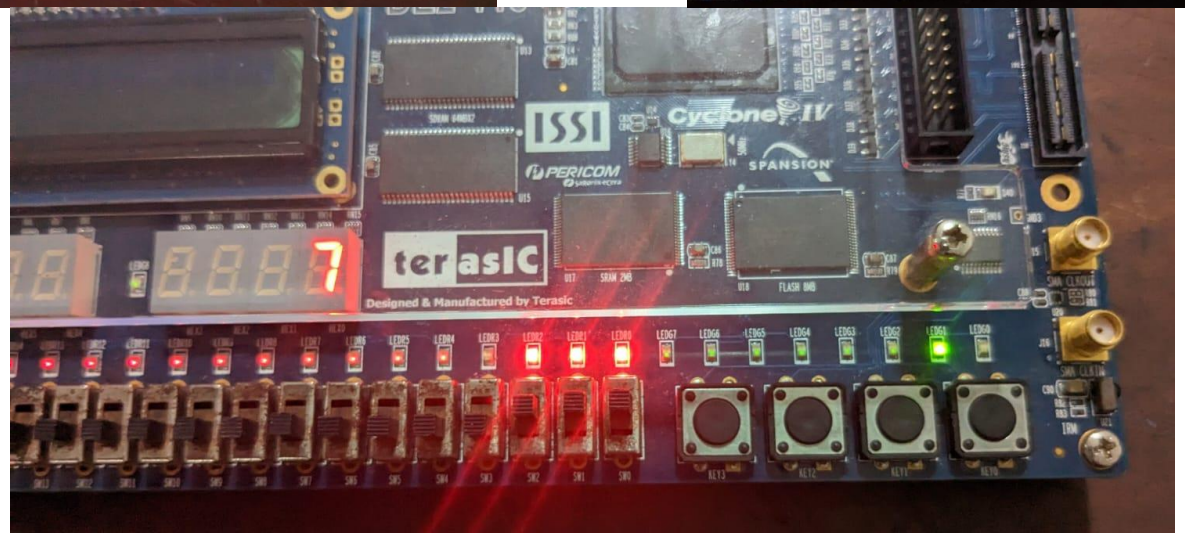
Data Enable

Reset

Results


ISSI
Cyclone IV
PERICOM
SPANSION
terasIC
Designed & Manufactured by Terasic
9


ISSI
Cyclone IV
PERICOM
SPANSION
terasIC
0


ISSI
Cyclone IV
PERICOM
SPANSION
terasIC
Designed & Manufactured by Terasic
7

Thank You!