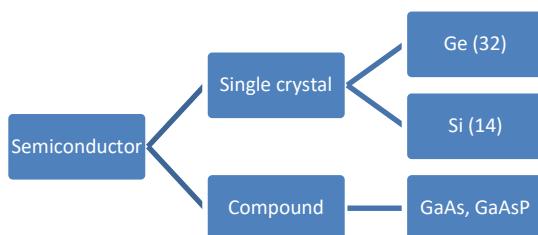


Course Teacher: Hafiz Al Mahmud

Lecture-01

Semiconductor Materials:

Conductor	Insulator	Semiconductor
Any material that will support a generous flow of charge when a voltage source of limited magnitude is applied across its terminals	An insulator is a material that offers a very low level of conductivity under pressure from an applied voltage source	A material that has a conductivity level somewhere between the extremes of an insulator and a conductor
e.g. silver (Ag), copper (Cu), aluminum (Al) etc	e.g. ceramic, plastic, rubber, dry wood etc	e.g. germanium (Ge), silicon (Si), Gallium arsenide (GaAs), Gallium arsenide phosphide (GaAsP) etc



Covalent Bonding and Intrinsic Materials:

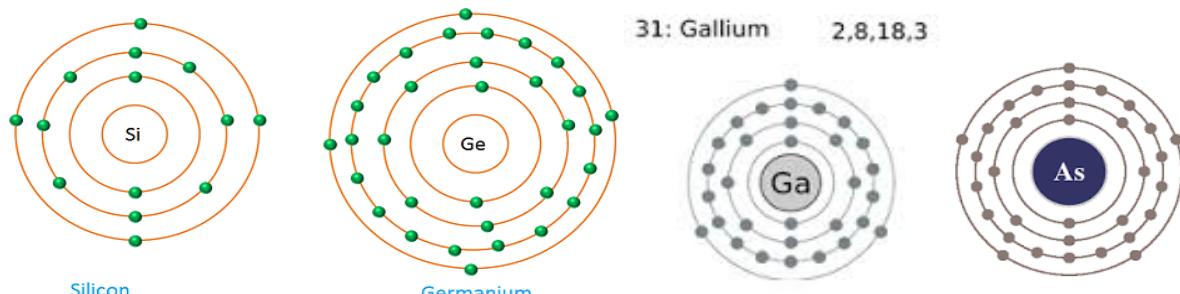


Fig. 1. Atomic structure of silicon, germanium, gallium (three valence electrons) and arsenic (five valence electrons)

A bonding of atoms, strengthened by the sharing of electrons, is called covalent bonding.

Intrinsic Semiconductor:

An intrinsic semiconductor material is chemically very pure and possesses poor conductivity. It has equal numbers of negative carriers (electrons) and positive carriers (holes).

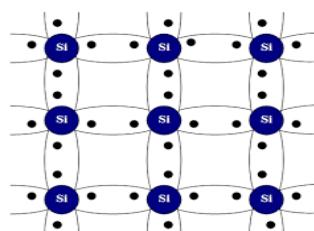
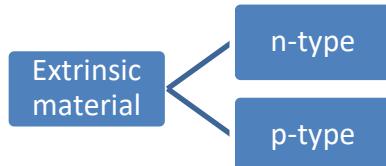


Fig. 2. Covalent bonding of the silicon atom

At room temperature there are approximately 1.5×10^{10} free carriers in a cubic centimeter of intrinsic silicon material.

Extrinsic Materials:

A semiconductor material that has been subjected to the doping process is called an **extrinsic material**.



n-Type Material:

The n-type is created by introducing those impurity elements that have five valence electrons (pentavalent), such as antimony (Sb), arsenic (As), and phosphorus (P).

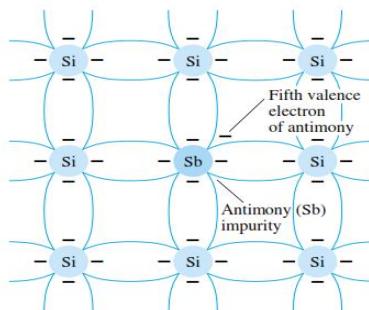


Fig. 3. Antimony impurity in n-type material

Diffused impurities with **five** valence electrons are called **donor** atoms.

p-Type Material:

The p-type material is formed by doping a pure germanium or silicon crystal with impurity atoms having three valence electrons.

The elements most frequently used for this purpose are boron (B), gallium (Ga), and indium (In).

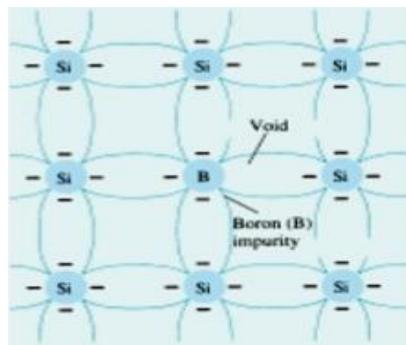


Fig. 4. Boron impurity in p-type material

Here an insufficient number of electrons to complete the covalent bonds of the newly formed lattice. The resulting vacancy is called a **hole** and is represented by a small circle or positive sign due to the absence of a negative charge.

The diffused impurities with **three** valence electrons are called **acceptor** atoms.

Majority and Minority Carriers:

In an n-type material (Fig. 3) the electron is called the majority carrier and the hole the minority carrier.

In a p-type material (Fig. 4) the hole is the majority carrier and the electron is the minority carrier.

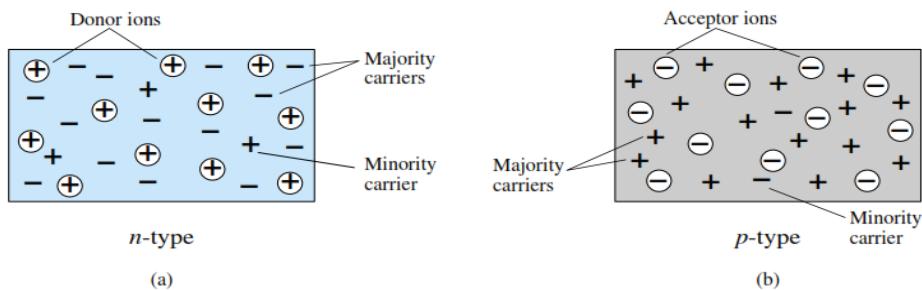


Fig. 5. (a) n-type material; (b) p-type material

Semiconductor Diode:

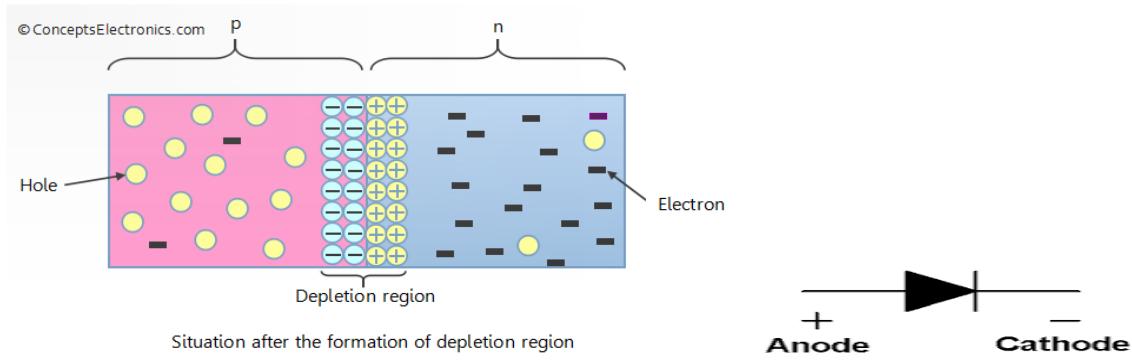


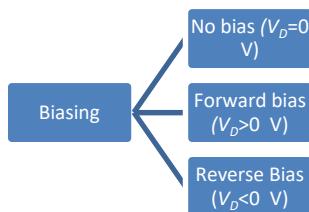
Fig. 6. P-n junction diode and its symbol

Diode is a **unidirectional** device that allows the current to flow in one direction and opposes in other direction.

- Two electrode device
- Mostly used in rectification.
- The arrow denotes the flow of current.

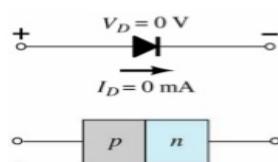
Depletion Region:

This region of uncovered positive and negative ions is called the depletion region due to the depletion of carriers in this region.



No Applied Bias ($V_D=0$ V):

- No external voltage is applied: $V_D=0$ V
- No current is flowing: $I_D=0$ A
- Only a modest depletion region exists



Reverse-Bias Condition ($V_D < 0$ V):

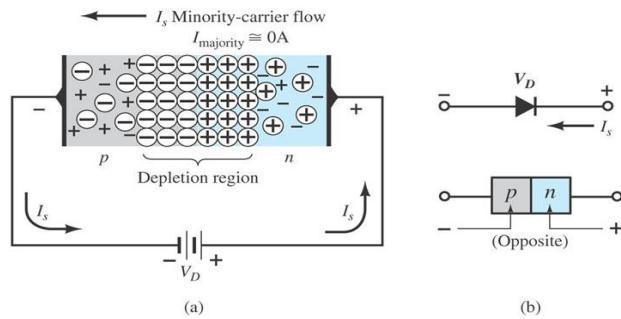


Fig. 7. (a) Internal distribution of charge under reverse-bias conditions; (b) reverse-bias polarity and direction of reverse saturation current

- External voltage is applied across the p-n junction in the opposite polarity of the p and n type materials.
- The reverse bias causes the depletion region to widen.
- The electrons in the n-type material are attracted toward the positive terminal of the voltage source.
- The holes in the p-type material are attracted toward the negative terminal of the voltage source.
- When all minority carriers are flowing across, further increase in bias voltage will not increase the current. This current is referred to as reverse saturation current.
- **Current is due to minority charge carriers.**

Forward characteristics:

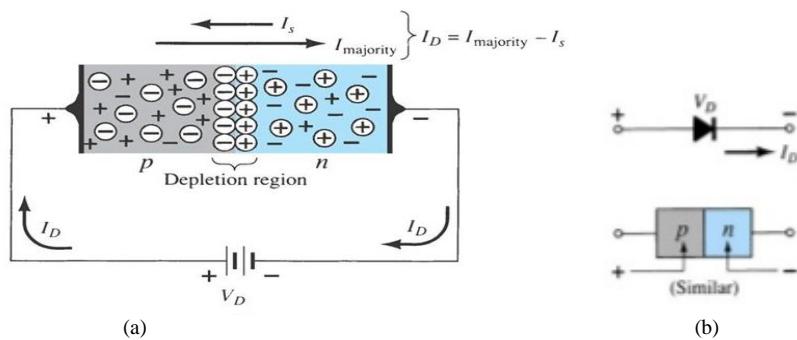


Fig. 8. (a) Internal distribution of charge under forward-bias conditions; (b) forward-bias polarity and direction of resulting current

- External voltage is applied across the p-n junction in the same polarity as the p and n type materials.
- The forward voltage V_D will pressure e⁻ in the n-type and holes in the p-type material to recombine with the ions near the boundary. V_D reduces the width of the depletion region.
- The e⁻ and holes have the sufficient energy to cross the p-n junction.
- A very little amount of current called the **forward current** flows until the forward voltage exceeds the junction barrier potential.
- **Current is due to majority carriers.**

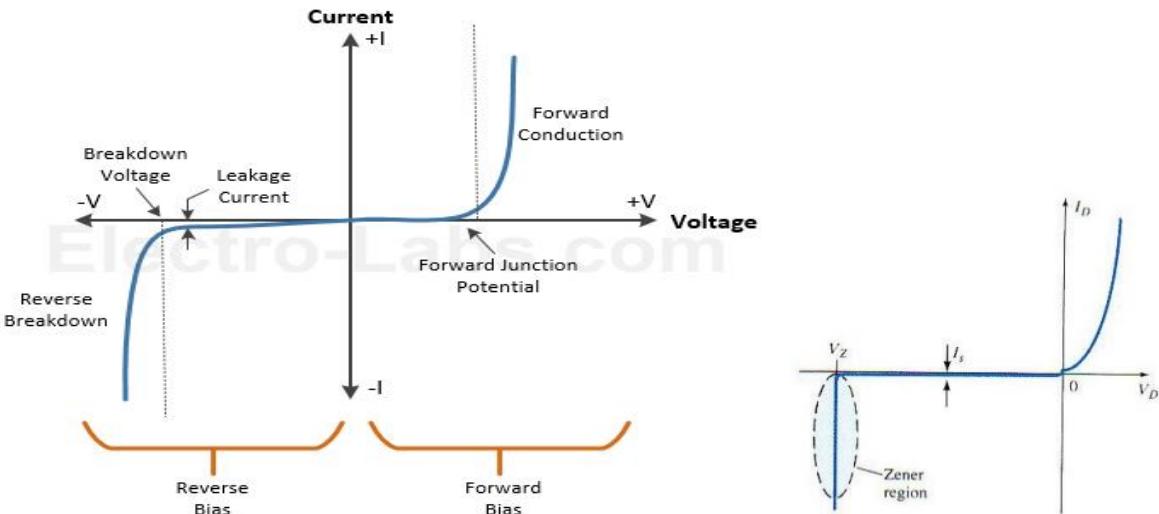


Fig. 9. V-I characteristics of Si diode

Zener Region: At some point the reverse bias voltage is so large that the diode breaks down and the reverse current increases dramatically. The reverse-bias potential that results in this dramatic change in characteristics is called the Zener potential (V_Z).

Recombination lifetime: The recombination lifetime is defined as the average time it takes an excess minority carrier to recombine.

Reverse Saturation Current (I_S): The current that exists under reverse bias conditions is called the reverse saturation current (I_S).

Break down voltage:

During reverse bias, defined as the reverse voltage at which p-n junction breaks down with a sudden rise in reverse current.

Knee voltage:

Knee voltage occurs during forward bias. Defined as forward voltage at which the current through junction increases rapidly.

Peak inverse voltage:

The maximum reverse-bias potential that can be applied before entering the Zener region is called the peak inverse voltage (PIV) or the peak reverse voltage (PRV).

A diode should not exceed peak inverse voltage otherwise the junction may get damaged due to excessive heating.

The forward bias voltage for GaAs diode = 1.2 V, Si diode = 0.7 V and Ge = 0.3 V

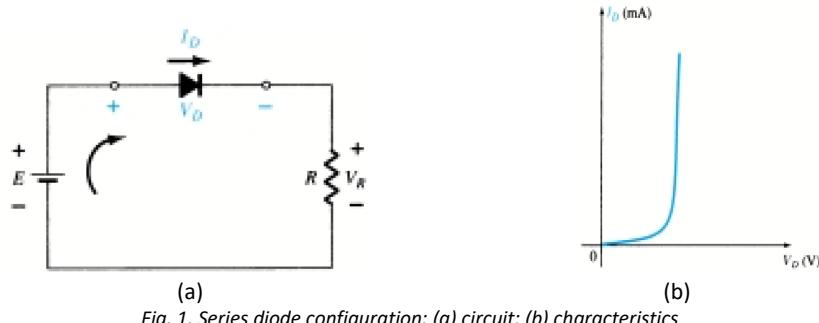
Possible Questions:

Broad Questions:	Short Questions:
1) Explain the Forward bias condition for a p-n junction semiconductor diode with appropriate diagram.	1) Define Donor, Acceptor, Depletion Region, Recombination lifetime, Reverse Saturation Current, Break down voltage, Knee voltage, Peak inverse voltage
2) Explain the Reverse bias condition for a p-n junction semiconductor diode with appropriate diagram.	2) Explain Zener region.
3) State the characteristics of a p-n junction diode.	3) Short notes: n-type material, p-type material
4) Draw the silicon semiconductor diode characteristics.	

Lecture-02

Load Line Analysis:

The load line plots all possible combinations of diode current (I_D) and voltage (V_D) for a given circuit. The intersection of the load line with the characteristics will determine the point of operation of the system.



The diode is in the 'on' state and conduction has been established. Applying Kirchhoff's voltage law to the series circuit

$$\begin{aligned} E - V_D - V_R &= 0 \\ E &= V_D + I_D R \end{aligned} \quad (1)$$

If we set $V_D=0$ V in Eq. (1) and solve for I_D ,

$$\begin{aligned} E &= V_D + I_D R \\ &= 0 \text{ V} + I_D R \\ I_D &= \frac{E}{R} [V_D = 0 \text{ V}] \end{aligned} \quad (2)$$

If we set $I_D=0$ A, Eq. (1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= V_D + (0 \text{ A})R \\ V_D &= E [I_D = 0 \text{ A}] \end{aligned} \quad (3)$$

A straight line drawn between the two points will define the load line as depicted in Fig. 2.

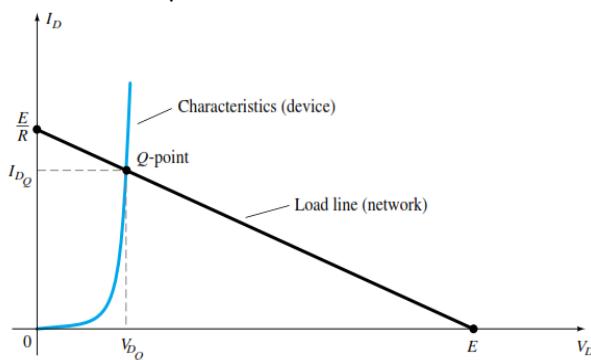


Fig. 2. Drawing the load line and finding the point of operation

Change the level of R (the load) the result will be a change in the slope of the load line. The point of intersection between the two is the point of operation for this circuit.

The point where the load line and the characteristic curve intersect is the Q-point, the point of operation is usually called the **quiescent point** which identifies I_D and V_D for a particular diode in a given circuit.

Series Diode Configurations:

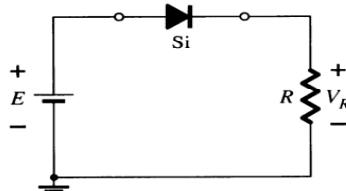


Fig. 3. Series diode configuration

Forward Bias:

Constants

- Silicon Diode: $V_D = 0.7 \text{ V}$
- Germanium Diode: $V_D = 0.3 \text{ V}$

Analysis (for silicon)

- $V_D = 0.7 \text{ V}$ (or $V_D = E$ if $E < 0.7 \text{ V}$)
- $V_R = E - V_D$
- $I_D = I_R = V_R / R$

Reverse Bias:

Diodes ideally behave as open circuits

Analysis

- $V_D = E$
- $V_R = 0 \text{ V}$
- $I_D = 0 \text{ A}$

Example-1:

Determine V_o and I_D for the series circuit of Fig. 4.

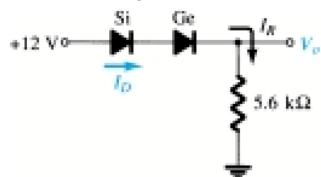
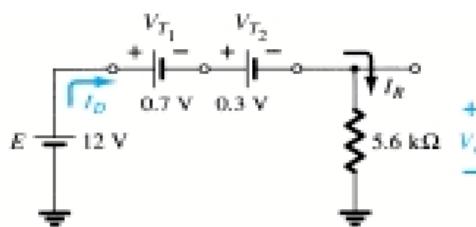


Fig. 4. Circuit for Example 1

Solution:

$$\begin{aligned} V_o &= E - V_{T1} - V_{T2} \\ &= 12 \text{ V} - 0.7 \text{ V} - 0.3 \text{ V} \\ &= 11 \text{ V} \end{aligned}$$

$$I_D = I_R = \frac{V_o}{R} = \frac{11 \text{ V}}{5.6 \text{ k}\Omega} \approx 1.96 \text{ mA}$$



Example-2:

Determine I , V_1 , V_2 and V_o for the series dc configuration of Fig. 5.

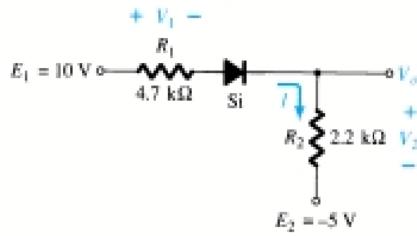


Fig. 5. Circuit for Example 2

Solution:

$$-E_1 + IR_1 + V_D + IR_2 - E_2 = 0$$

$$I = \frac{E_1 - V_D + E_2}{R_1 + R_2} = \frac{10 \text{ V} - 0.7 \text{ V} + 5 \text{ V}}{4.7 \text{ k}\Omega + 2.2 \text{ k}\Omega} = \frac{14.3 \text{ V}}{6.9 \text{ k}\Omega} \approx 2.072 \text{ mA}$$

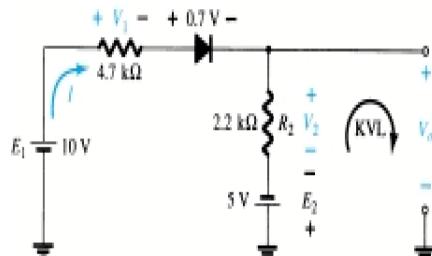
$$V_1 = IR_1 = (2.072 \text{ mA})(4.7 \text{ k}\Omega) = 9.74 \text{ V}$$

$$V_2 = IR_2 = (2.072 \text{ mA})(2.2 \text{ k}\Omega) = 4.56 \text{ V}$$

Applying KVL,

$$E_2 - IR_2 + V_o = 0$$

$$V_o = -E_2 + IR_2 = 4.56 \text{ V} - 5 \text{ V} = -0.44 \text{ V}$$

Example-3:

Determine V_o , I_1 , I_{D1} and I_{D2} for the parallel diode configuration of Fig. 6.

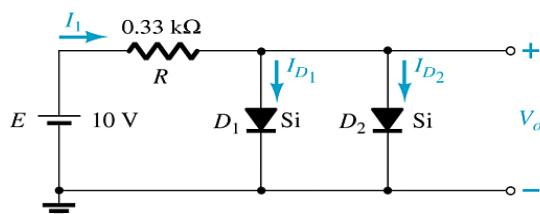


Fig. 6. Circuit for Example 6

Solution:

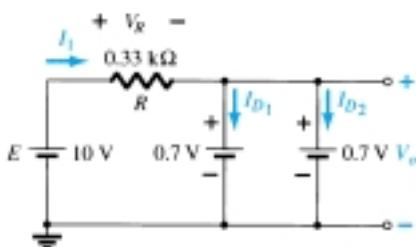
$$V_D = 0.7 \text{ V}$$

$$V_{D1} = V_{D2} = V_o = 0.7 \text{ V}$$

$$V_R = 10 \text{ V} - 0.7 \text{ V} = 9.3 \text{ V}$$

$$I_1 = \frac{E - V_D}{R} = \frac{10 \text{ V} - 0.7 \text{ V}}{0.33 \text{ k}\Omega} = 28 \text{ mA}$$

$$I_{D1} = I_{D2} = \frac{28 \text{ mA}}{2} = 14 \text{ mA}$$



Try Yourself:

1. Determine the current I for the network of Fig. 7.

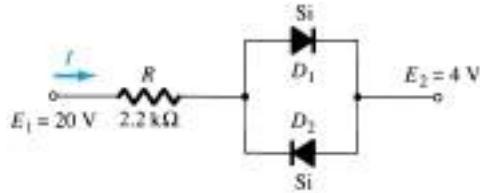


Fig. 7.

2. Determine the voltage V_o for the network of Fig. 8.

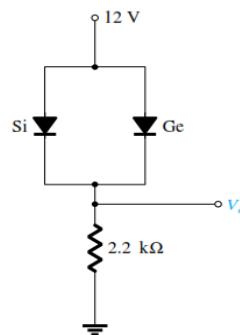


Fig. 8.

3. Determine the currents I_1 , I_2 , and I_{D2} for the network of Fig. 9.

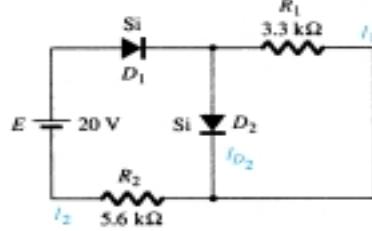


Fig. 9.

Possible Questions:

Broad Questions:	
1) With appropriate circuit diagram explain the DC load line analysis of a semiconductor diode.	Mathematical Problems related to the module and class lecture.

Lecture-3, 4 (Module-03)

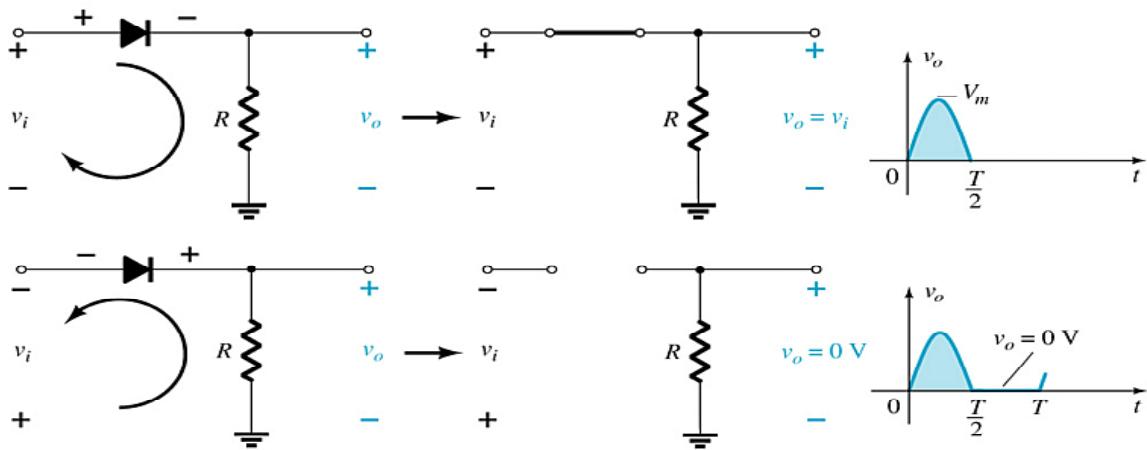
Rectifier:

A rectifier is an electrical device that converts an alternating current into a direct one by allowing a current to flow through it in one direction only.

Half-wave Rectification:

The process of removing one-half the input signal to establish a dc level is aptly called **half-wave rectification**.

The diode only conducts when it is forward biased, therefore only half of the AC cycle passes through the diode to the output.

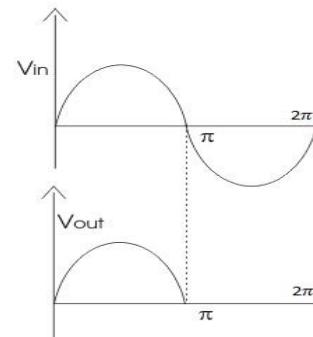


- The DC output voltage/Average value, V_{dc} :

Let, the peak value of output voltage = V_p

Average output voltage,

$$\begin{aligned} V_{dc} &= \frac{1}{2\pi} \int_0^\pi (V_p \sin \omega t) d\omega t \\ &= \frac{V_p}{2\pi} [-\cos \omega t]_0^\pi \\ &= \frac{V_p}{2\pi} (2) \\ &= 0.318 V_p \end{aligned}$$



- The rms value, V_{rms} :

$$\begin{aligned} V_{rms} &= \sqrt{\frac{1}{2\pi} \int_0^\pi (V_p \sin \omega t)^2 d\omega t} \\ &= \sqrt{\frac{V_p^2}{4\pi} \int_0^\pi (1 - \cos 2\omega t) d\omega t} \\ &= \frac{V_p}{2\sqrt{\pi}} (\sqrt{\pi}) \\ &= 0.5V_p \end{aligned}$$

- The period of a half wave signal is the same as the input signal.

$$f_{out} = f_{in}$$

Transformer and peak inverse voltage:

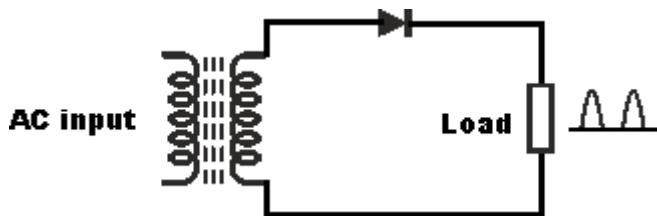


Fig. 1. Half wave rectifier

The peak output voltage, $V_{out(peak)}$ equals the peak secondary voltage, $V_{2(peak)}$

$$V_{out(peak)} = V_{2(peak)}$$

The dc load voltage, $V_{dc} = 0.318V_{out(peak)}$

The dc load current is, $I_{dc} = \frac{V_{dc}}{R_L}$

Peak Inverse Voltage (PIV):

In a rectifier circuit, the maximum reverse voltage that appears across a diode is called the peak inverse voltage (PIV).

$$PIV = V_{2(peak)}$$

The dc diode current is equal to the dc load current,

$$I_{diode} = I_{dc}$$

Example-1:

What is the dc voltage across the load resistor? The peak inverse voltage across the diode? The dc current through the diode? Here, $V_{in} = 40\text{ V}_{rms}$, $R_L = 20\Omega$

Solution:

$$V_{2(peak)} = \frac{V_{2(rms)}}{0.5} = 80\text{ V}$$

Peak secondary voltage, $V_{out} = V_{2(peak)} = 80\text{ V}$

Dc load voltage,

$$V_{dc} = 0.318V_{out(peak)} = 0.318 \times 80 = 25.44\text{ V}$$

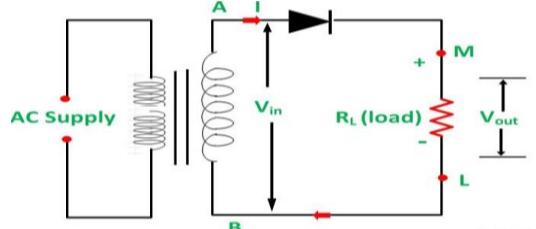
$$PIV = V_{2(peak)} = 80\text{ V}$$

Dc load current,

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{25.44}{20} = 1.272\text{ A}$$

Dc diode current,

$$I_{diode} = I_{dc} = 1.272\text{ A}$$

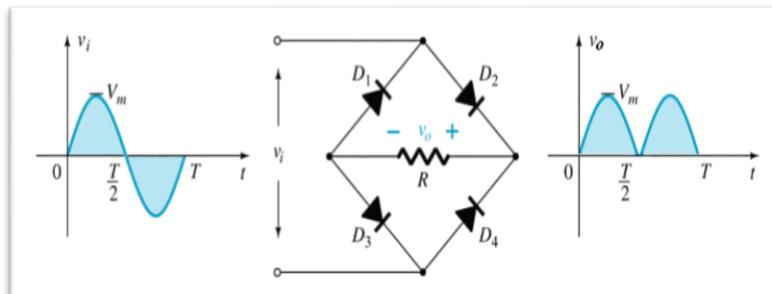


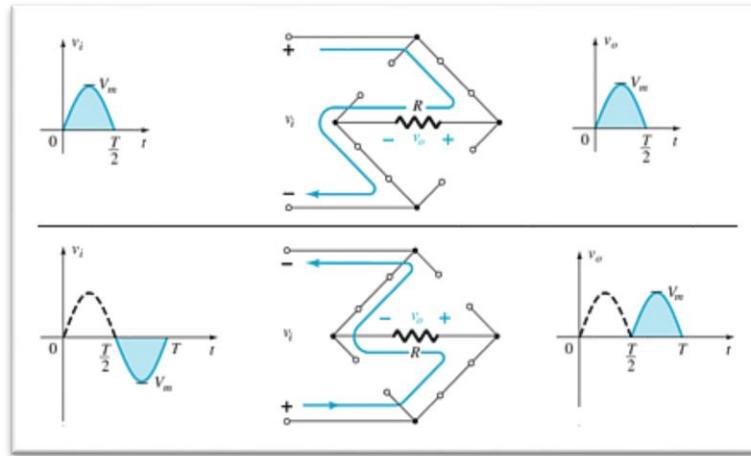
Full-wave Rectification:

The dc level obtained from a sinusoidal input can be improved 100% using a process called full-wave rectification.

The Bridge Rectifier:

The most familiar network for performing such a function is four diodes in a **bridge** configuration.



Working Principle:

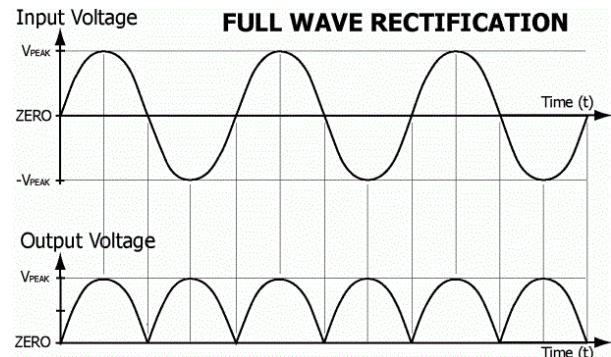
- During the positive half cycle, D_2 and D_3 are forward biased, while D_1 and D_4 are reverse biased.
- Electrons flow up through D_3 , load resistance and D_2
- During the negative half cycle, D_1 and D_4 are conducting, while D_2 and D_3 are off.
- Electrons flow through D_1 , load resistance and D_4
- During either half cycle, the electron flow is to the right through the load resistor. Because of this the load voltage is the full wave signal.

- The DC output voltage/Average value, V_{dc} :**

Let, the peak value of output voltage = V_p

Average output voltage,

$$\begin{aligned} V_{dc} &= \frac{1}{2\pi} \left[\int_0^{\pi} (V_p \sin \omega t) d\omega t + \right. \\ &\quad \left. \int_{\pi}^{2\pi} (V_p \sin \omega t) d\omega t \right] \\ &= \frac{2V_p}{2\pi} [-\cos \omega t]_0^{\pi} \\ &= \frac{V_p}{\pi} (2) \\ &= 0.636 V_p \end{aligned}$$



- The rms value, V_{rms} :**

$$\begin{aligned} V_{rms} &= \sqrt{\frac{1}{2\pi} \left[\int_0^{\pi} (V_p \sin \omega t)^2 d\omega t + \int_{\pi}^{2\pi} (V_p \sin \omega t)^2 d\omega t \right]} \\ &= \sqrt{\frac{2V_p^2}{4\pi} \int_0^{\pi} (1 - \cos 2\omega t) d\omega t} \\ &= \frac{V_p}{\sqrt{2\pi}} (\sqrt{\pi}) \\ &= 0.707 V_p \end{aligned}$$

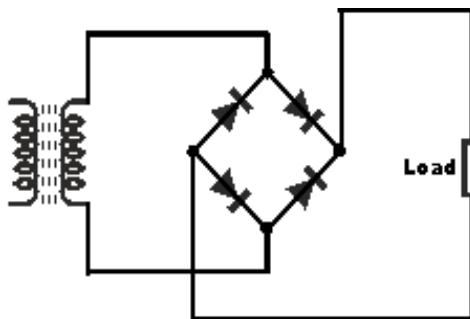
- $PIV = V_{2(peak)}$
- $I_{diode} = I_{dc}/2$

Example-2:

What are the following values, V_{dc} , PIV, and I if $V_{rms}=40V$ and $R_L=20\Omega$

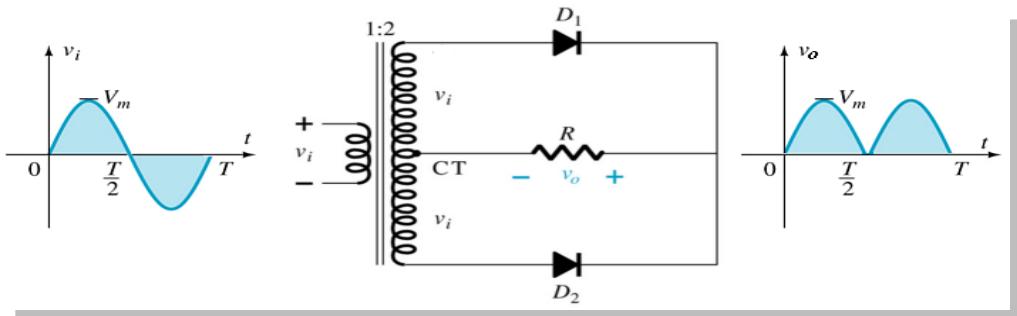
Solution:

$$\begin{aligned}
 V_{2(\text{peak})} &= \frac{40\text{V}}{0.707} = 56.6 \text{ V} \\
 V_{\text{out}(\text{peak})} &= V_{2(\text{peak})} = 56.6 \text{ V} \\
 V_{dc} &= 0.636V_{\text{out}(\text{peak})} = 0.636(56.6) \text{ V} = 36 \text{ V} \\
 PIV &= V_{2(\text{peak})} = 56.6 \text{ V} \\
 I_{dc} &= \frac{V_{dc}}{R_L} = \frac{36 \text{ V}}{20 \Omega} = 1.8 \text{ A} \\
 I_{\text{diode}} &= I_{dc}/2 = \frac{1.8 \text{ A}}{2} = 0.9 \text{ A}
 \end{aligned}$$



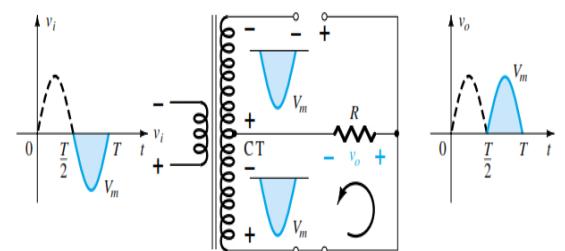
Center-Tapped Transformer:

A second popular full-wave rectifier is only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer.



Working Principle:

- During the positive half cycle of secondary voltage, the upper diode (D_1) is forward biased and lower diode (D_2) is reverse biased.
- Therefore, current flows through the load resistor (R), diode D_1 and upper half winding.
- During negative half cycle, current flows through the load resistor (R), the diode (D_2) and the lower half winding. As D_1 is 'OFF' and D_2 is 'ON'.
- The load current is in the same direction during both half cycles. For this reason, the load voltage is the full-wave signal.



$$V_{dc} = 0.318 \times 2 V_{\text{out}(\text{peak})} \text{ where, } V_{\text{out}(\text{peak})} = \text{peak load voltage}$$

$$V_{\text{out}(\text{peak})} = \frac{V_{2(\text{peak})}}{2} = \text{half the secondary winding}$$

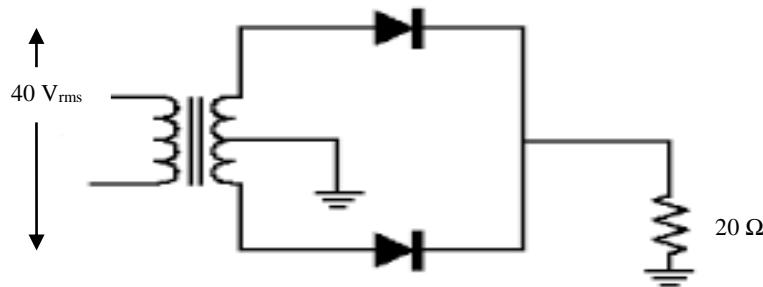
$$f_{\text{out}} = 2f_{\text{in}}$$

$$PIV = V_{2(\text{peak})}$$

$$I_{\text{diode}} = I_{dc}/2 = \text{each diode conducts for only half a cycle}$$

Example-3:

What is the dc voltage across the load resistor? The peak inverse voltage across each diode? The dc current through each diode? Here, $V_{in}=40 \text{ V}_{rms}$, $R_L=20 \Omega$



Solution:

$$V_{2(peak)} = \frac{40\text{V}}{0.707} = 56.6 \text{ V}$$

$$V_{out(peak)} = \frac{V_{2(peak)}}{2} = \frac{56.6 \text{ V}}{2} = 28.3 \text{ V}$$

$$V_{dc} = 0.636V_{out(peak)} = 0.636(28.3) \text{ V} = 18 \text{ V}$$

$$PIV = V_{2(peak)} = 56.6 \text{ V}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{18 \text{ V}}{20 \Omega} = 0.9 \text{ A}$$

$$I_{diode} = I_{dc}/2 = \frac{0.9 \text{ A}}{2} = 0.45 \text{ A}$$

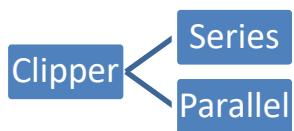
Possible Questions:

Broad Questions:	
1) With appropriate circuit diagram explain the working principle of Half wave rectifier.	Mathematical Problems related to the module and class lecture.
2) With appropriate circuit diagram explain the working principle of a bridge rectifier.	Short Question: What is a rectifier?
3) With appropriate circuit diagram explain the working principle of center tapped full wave rectifier.	

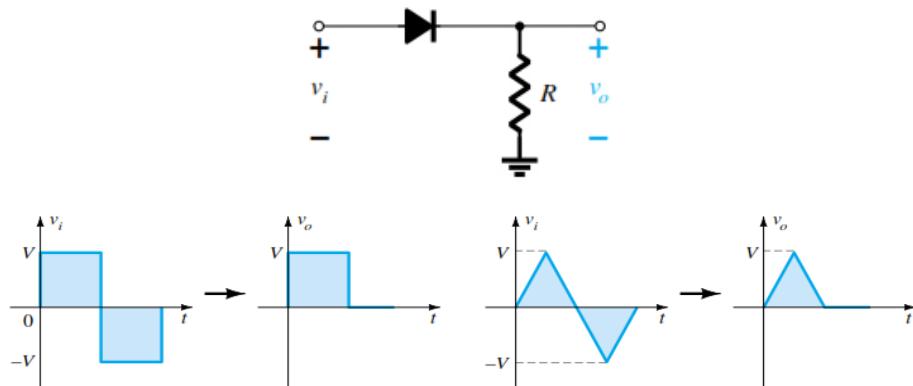
Lecture-4,5

CLIPPERS:

Clippers are networks that employ diodes to clip away a portion of an input signal without distorting the remaining part of the applied waveform.

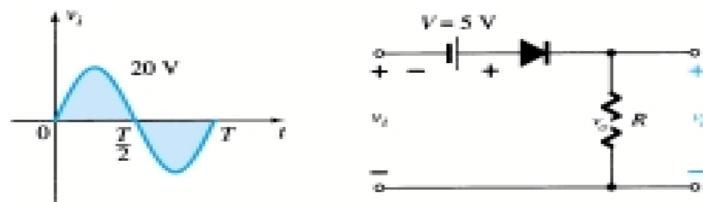


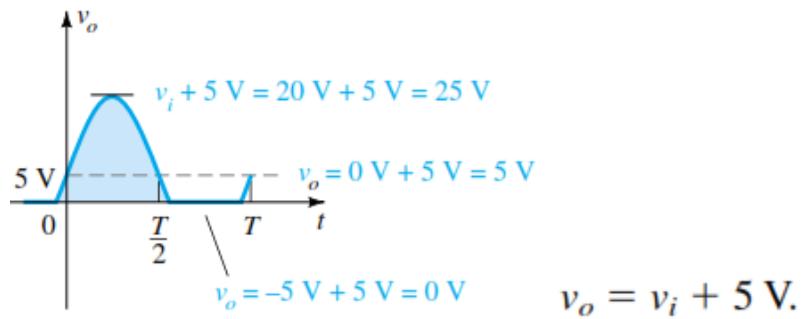
Series:



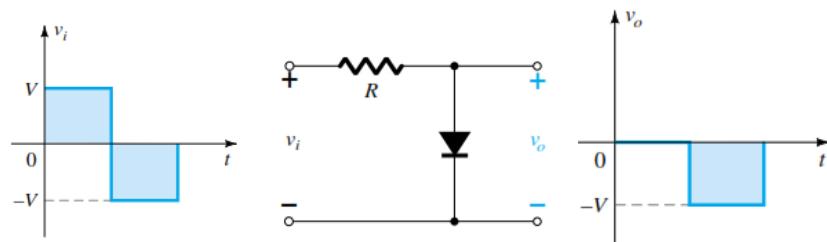
Example-1:

Determine the output waveform for the network



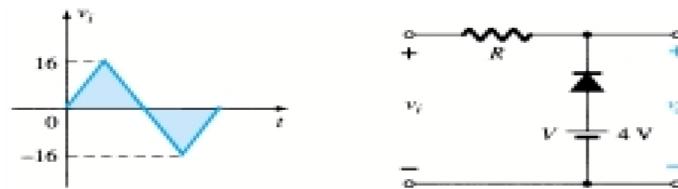


Parallel:

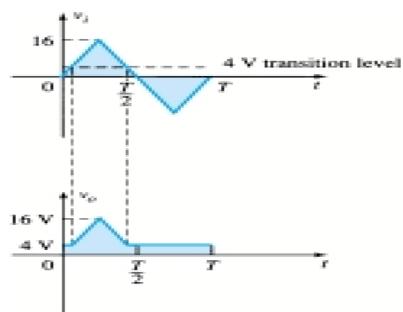


Example-1:

Determine the output waveform for the network

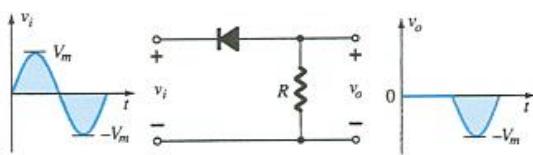


Solution:

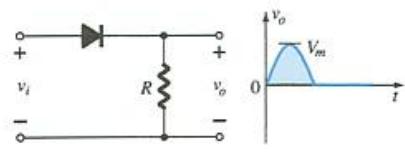


Simple Series Clippers (Ideal Diodes)

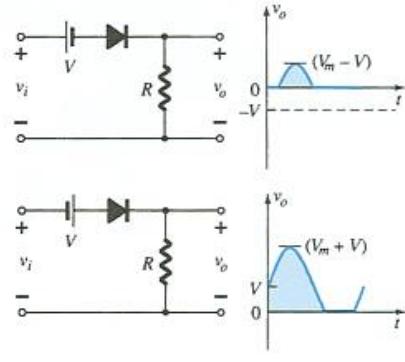
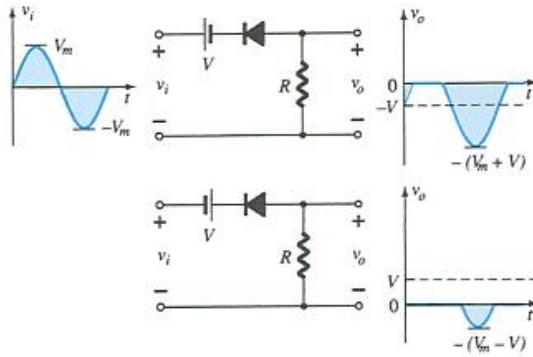
POSITIVE



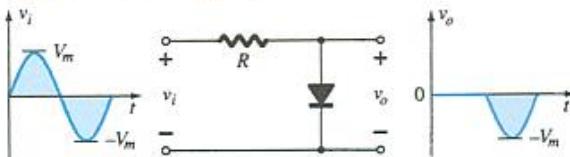
NEGATIVE



Biased Series Clippers (Ideal Diodes)

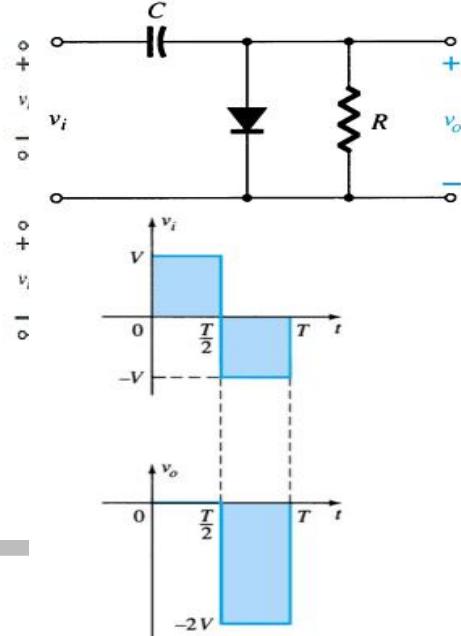
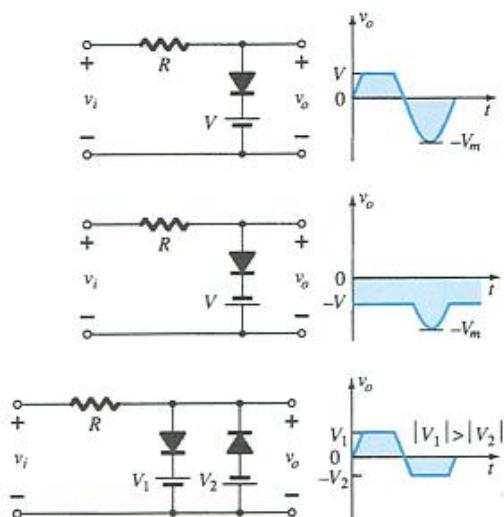


Simple Parallel Clippers (Ideal Diodes)



NEGATIVE

Biased Parallel Clppers (Ideal Diodes)

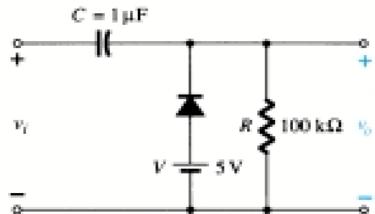
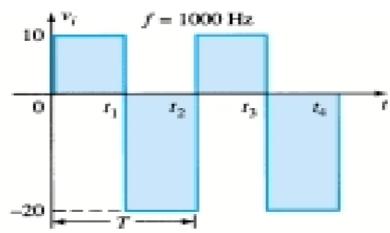


Clampers:

A diode and capacitor can be combined to “clamp” an AC signal to a specific DC level.

Example-3:

Determine v_o for the network



Solution:

Applying KVL,

$$-20 \text{ V} + V_C - 5 \text{ V} = 0$$

$$V_C = 25 \text{ V}$$

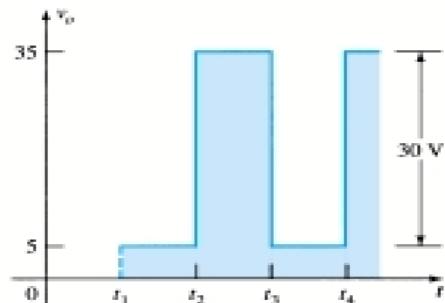
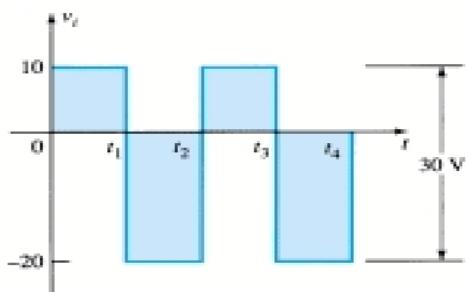
Applying KVL,

$$+10 \text{ V} + 25 \text{ V} - v_o = 0$$

$$v_o = 35 \text{ V}$$

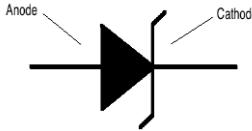
$$\tau = RC = (100 \text{ k}\Omega)(0.1 \text{ }\mu\text{F}) = 0.01 \text{ s} = 10 \text{ ms}$$

The total discharge time is therefore $5\tau = 5(10 \text{ ms}) = 50 \text{ ms}$.



Zener Diodes:

A zener diode is a diode designed to operate in the breakdown region because its voltage is almost



constant. It is ideal for voltage regulator.

When $V_i \geq V_z$

- The Zener is on
- Voltage across the Zener is V_z
- Zener current: $I_z = I_R - I_{RL}$
- The Zener Power: $P_z = V_z I_z$

When $V_i < V_z$

- The Zener is off
- The Zener acts as an open circuit

Example-4:

- (a) For the Zener diode network, determine V_L , V_R , I_z and P_z
 (b) Repeat part (a) with $R_L = 3 \Omega$

Solution:

(a)

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2 \text{ k}\Omega (16 \text{ V})}{1 \text{ k}\Omega + 1.2 \text{ k}\Omega} = 8.73 \text{ V}$$

Since $V = 8.73 \text{ V}$ is less than $V_z = 10 \text{ V}$, the diode is in the “off” state,

$$V_L = V = 8.73 \text{ V}$$

$$V_R = V_i - V_L = 16 \text{ V} - 8.73 \text{ V} = 7.27 \text{ V}$$

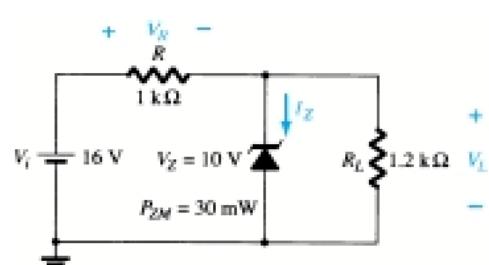
$$I_z = 0 \text{ A}$$

$$P_z = V_z I_z = V_z (0 \text{ A}) = 0 \text{ W}$$

(b)

$$V = \frac{R_L V_i}{R + R_L} = \frac{3 \text{ k}\Omega (16 \text{ V})}{1 \text{ k}\Omega + 3 \text{ k}\Omega} = 12 \text{ V}$$

Since $V = 12 \text{ V}$ is greater than $V_z = 10 \text{ V}$, the diode is in the “on” state



$$V_L = V_Z = \mathbf{10 \text{ V}}$$

$$V_R = V_i - V_L = 16 \text{ V} - 10 \text{ V} = \mathbf{6 \text{ V}}$$

$$I_L = \frac{V_L}{R_L} = \frac{10 \text{ V}}{3 \text{ k}\Omega} = 3.33 \text{ mA}$$

$$I_R = \frac{V_R}{R} = \frac{6 \text{ V}}{1 \text{ k}\Omega} = 6 \text{ mA}$$

$$I_Z = I_R - I_L \text{ [Eq. (2.18)]}$$

$$= 6 \text{ mA} - 3.33 \text{ mA}$$

$$= \mathbf{2.67 \text{ mA}}$$

$$P_Z = V_Z I_Z = (10 \text{ V})(2.67 \text{ mA}) = \mathbf{26.7 \text{ mW}}$$

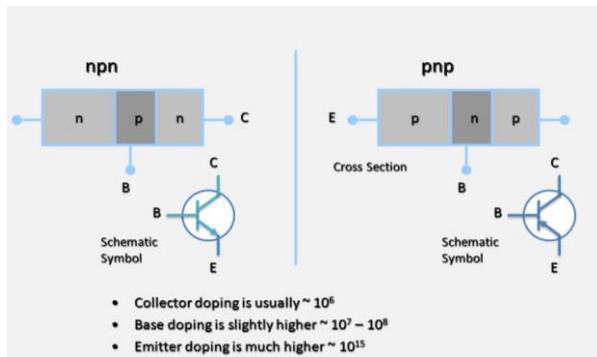
Voltage Regulator:

A circuit that converts a varying dc input voltage into a constant output dc voltage.

Possible Questions:

	Short Question:	
1) Output waveform sketching for given clipper or clamper circuit.	1) Definition: Clipper, Clamper, Zener diode, Voltage regulator.	Mathematical Problems related to the module and class lecture.

BJT: Bipolar Junction Transistor. The term bipolar reflects that holes and electrons participate in the injection process into the opposite polarized material. If only one carrier is employed (electron or hole), it is considered a unipolar device. The terminals have been indicated by E for emitter, C for collector and B for base.



- Transistor is a three-layer semiconductor device, either p-n-p or n-p-n transistor.
- Transistor is an electronic component used in a circuit to control a large amount of current and voltage with a small amount of voltage or current.
- It can be used to amplify or switch electrical signals or power.

The name transistor is a combination of the words transfer and resistor.

Transfer+ resistor= transistor

Because it is a resistor or semiconductor device which can amplify electrical signals as they are transferred through it from input to output terminals.

Doping Level:

In a BJT the emitter layer is heavily doped, the base is lightly doped and the collector is moderately doped.

Emitter>Collector>Base

The emitter emits more electrons, so it is highly doped. The purpose of collector is to collect the electrons coming from emitter, thus it is moderately doped. Base should have always less doping to reduce the transit time.

Width: Collector>Emitter>Base

Operation of p-n-p Transistor:

- With the external source, V_{EE} and V_{CC} , one p-n junction of a transistor is reverse biased, while the other is forward biased.
- In base-to-emitter, the depletion region has been reduced in width due to the applied forward bias, resulting in a heavy flow of majority carriers from the p- to the n-type material.
- Due to the reverse bias in base-to-collector, the larger number of majority carriers of p-type material will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal.
- The sandwiched n-type material is very thin and has a low conductivity; a very small number of these carriers will take this path of high resistance to the base terminal, which is negligible.
- Applying KVL,

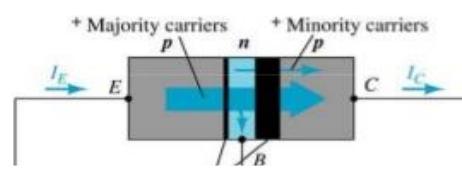


Fig. 1. Majority and minority carrier flow of a pnp transistor.



$$I_E = I_C + I_B$$

$$I_C \cong I_E$$

$$V_{BE} = 0.7 \text{ V}$$

Operating point:

For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Because the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated Q -point). Figure-2 shows a general output device characteristic with four operating points indicated.

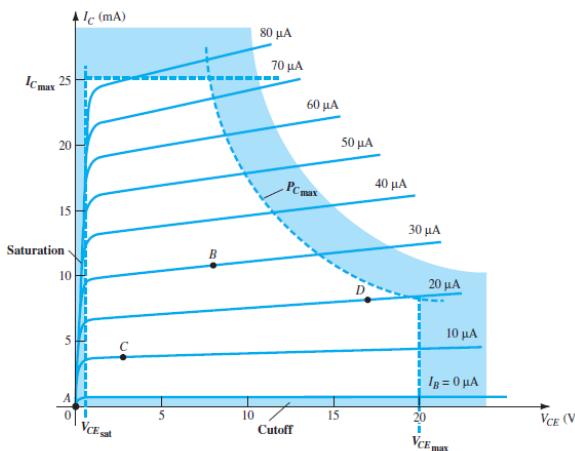


Figure-2: Various operating points within the limits of operation of a transistor.

The biasing circuit can be designed to set the device operation at any of these points or others within the *active region*. The maximum ratings are indicated on the characteristics of Fig-2 by a horizontal line for the maximum collector current $I_{C\max}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE\max}$. The maximum power constraint is defined by the curve $P_{C\max}$ in the same figure. At the lower end of the scales are the *cutoff region*, defined by $I_B \leq 0 \mu\text{A}$, and the *saturation region*, defined by $V_{CE} \leq V_{CESat}$.

Alpha (α)

In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called alpha and defined by the following equation:

$$\alpha_{dc} = \frac{I_C}{I_E}$$

Beta (β):

In the dc mode the levels of I_C and I_B are related by a quantity called beta and defined by the following equation:

$$\beta_{dc} = \frac{I_C}{I_B}$$

Relationship Between α and β :

$$\begin{aligned}
 I_E &= I_C + I_B \\
 \Rightarrow \frac{I_C}{\alpha} &= I_C + \frac{I_C}{\beta} [\because I_B = I_C/\beta, I_E = I_C/\alpha] \\
 \Rightarrow \frac{1}{\alpha} &= 1 + \frac{1}{\beta} \\
 \Rightarrow \beta &= \alpha\beta + \alpha = (\beta + 1)\alpha \\
 \therefore \alpha &= \frac{\beta}{\beta + 1} \text{ or, } \beta = \frac{\alpha}{1 - \alpha}
 \end{aligned}$$

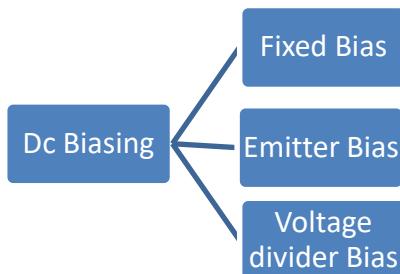
$$I_C = \beta I_B$$

$$I_E = I_C + I_B$$

$$= \beta I_B + I_B$$

$$I_E = (\beta + 1)I_B$$

DC Biasing:



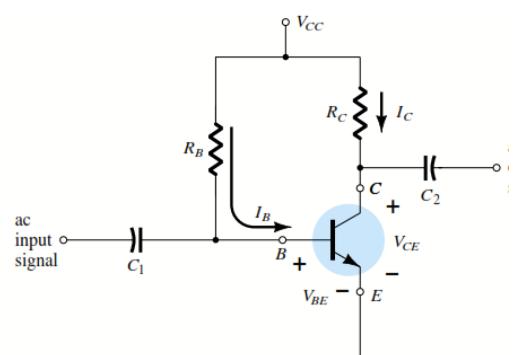
Fixed-Bias:

Forward Bias of Base–Emitter:

Applying KVL,

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



Collector–Emitter Loop:

$$I_C = \beta I_B$$

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$$V_{CE} = V_C$$

$$V_{BE} = V_B - V_E$$

$$V_{BE} = V_B$$

Example-1:

Determine the following for the fixed-bias configuration

- (a) I_{BQ} and I_{CQ} .
- (b) V_{CEQ} .
- (c) V_B and V_C .
- (d) V_{BC} .

Solution:

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega} = 47.08 \mu\text{A}$$

$$I_{CQ} = \beta I_{BQ} = (50)(47.08 \mu\text{A}) = 2.35 \text{ mA}$$

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C R_C \\ &= 12 \text{ V} - (2.35 \text{ mA})(2.2 \text{ k}\Omega) \\ &= 6.83 \text{ V} \end{aligned}$$

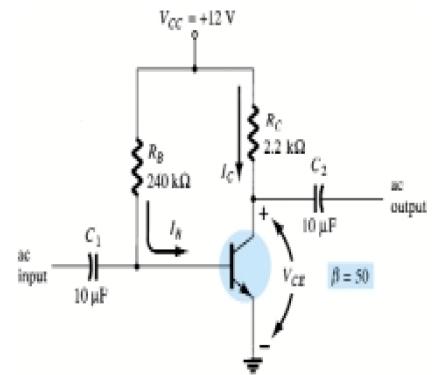
$$V_B = V_{BE} = 0.7 \text{ V}$$

$$V_C = V_{CE} = 6.83 \text{ V}$$

Using double-subscript notation yields

$$\begin{aligned} V_{BC} &= V_B - V_C = 0.7 \text{ V} - 6.83 \text{ V} \\ &= -6.13 \text{ V} \end{aligned}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.



Emitter Bias:

Base-Emitter Loop

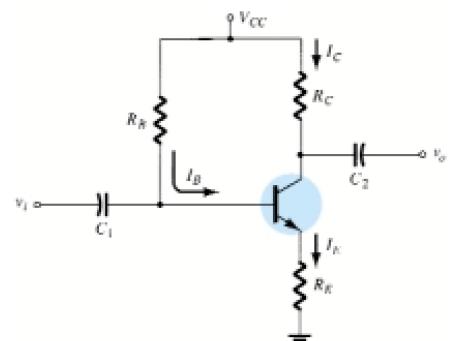
Applying KVL,

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0 \quad [I_E = (\beta + 1) I_B]$$

$$-I_B (R_B + (\beta + 1) R_E) + V_{CC} - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$



Collector-Emitter Loop

Applying KVL,

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} - V_{CC} + I_C (R_C + R_E) = 0$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$V_E = I_E R_E$$

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CE} + V_E$$

$$V_C = V_{CC} - I_C R_C$$

Or,

$$V_B = V_{CC} - I_B R_B$$

$$V_B = V_{BE} + V_E$$

Example-2:

For the emitter bias network of

- (a) I_B .
- (b) I_C .
- (c) V_{CE} .
- (d) V_C .
- (e) V_E .
- (f) V_B .
- (g) V_{BC} .

Solution

$$(a) \text{ Eq. (4.17): } I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{430 \text{ k}\Omega + (51)(1 \text{ k}\Omega)} \\ = \frac{19.3 \text{ V}}{481 \text{ k}\Omega} = 40.1 \mu\text{A}$$

$$(b) \quad I_C = \beta I_B \\ = (50)(40.1 \mu\text{A}) \\ \cong 2.01 \text{ mA}$$

$$(c) \text{ Eq. (4.19): } V_{CE} = V_{CC} - I_C(R_C + R_E) \\ = 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega + 1 \text{ k}\Omega) = 20 \text{ V} - 6.03 \\ = 13.97 \text{ V}$$

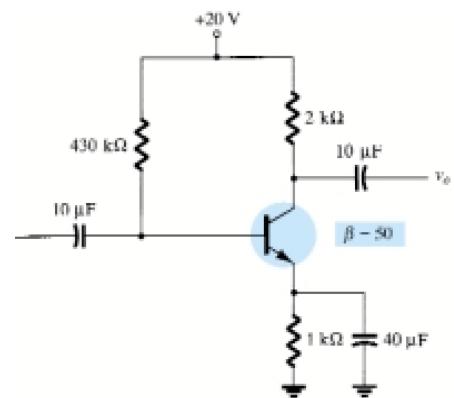
$$(d) \quad V_C = V_{CC} - I_C R_C \\ = 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega) = 20 \text{ V} - 4.02 \text{ V} \\ = 15.98 \text{ V}$$

$$(e) \quad V_E = V_C - V_{CE} \\ = 15.98 \text{ V} - 13.97 \text{ V} \\ = 2.01 \text{ V}$$

$$\text{or } V_E = I_E R_E \cong I_C R_E \\ = (2.01 \text{ mA})(1 \text{ k}\Omega) \\ = 2.01 \text{ V}$$

$$(f) \quad V_B = V_{BE} + V_E \\ = 0.7 \text{ V} + 2.01 \text{ V} \\ = 2.71 \text{ V}$$

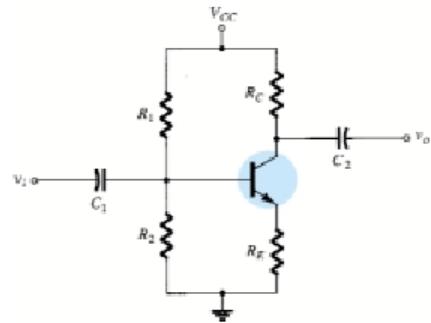
$$(g) \quad V_{BC} = V_B - V_C \\ = 2.71 \text{ V} - 15.98 \text{ V} \\ = -13.27 \text{ V} \quad (\text{reverse-biased as required})$$



Voltage-Divider Bias:

There are two types of analyses for voltage divider bias. If $\beta R_E \leq 10R_2$, then it is exact analysis. If $\beta R_E \geq 10R_2$, approximate analysis is applied.

Exact analysis:



$$R_{Th} = R_1 \| R_2$$

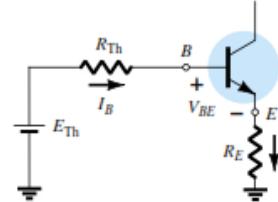
$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Applying KVL,

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



Approximate analysis:

The voltage across R_2 , which is actually the base voltage, can be determined from the equation,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Once V_B is determined, the level of V_E can be calculated from,

$$V_E = V_B - V_{BE}$$

and the emitter current can be determined from.

$$I_E = \frac{V_E}{R_E}$$

And $I_{CQ} \approx I_E$

The collector-to-emitter voltage is determined by, $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

But, because $I_E \approx I_C$,

$$V_{CEQ} = V_{CC} - I_C(R_C + R_E)$$

Example-3.1:

Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration.

Solution:

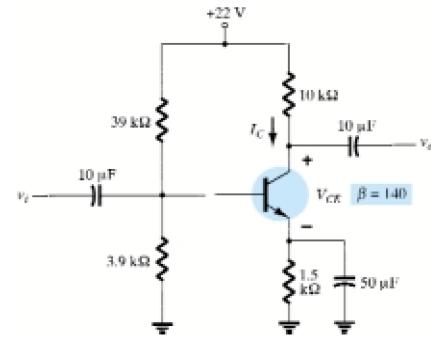
Here, $(140 \times 1.5) \geq (10 \times 3.9)$. So, it is approximate analysis.

$$\begin{aligned} V_B &= \frac{R_2 V_{CC}}{R_1 + R_2} \\ &= \frac{(3.9 \text{ k}\Omega)(22 \text{ V})}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} \\ &= 2 \text{ V} \end{aligned}$$

$$\begin{aligned} V_E &= V_B - V_{BE} \\ &= 2 \text{ V} - 0.7 \text{ V} \\ &= 1.3 \text{ V} \end{aligned}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3 \text{ V}}{1.5 \text{ k}\Omega} = 0.867 \text{ mA}$$

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\ &= 22 \text{ V} - (0.867 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\ &= 22 \text{ V} - 9.97 \text{ V} \\ &= 12.03 \text{ V} \end{aligned}$$

**Example 3.2:**

Determine the levels of I_{CQ} and V_{CEQ} for the voltage-divider configuration of following figure.

Solution: Here, $\beta R_E \leq 10 R_2$

$$(50)(1.2 \text{ k}\Omega) \leq 10(22 \text{ k}\Omega)$$

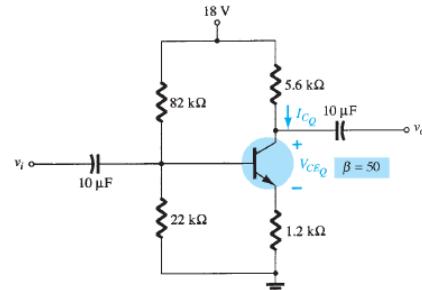
$60 \text{ k}\Omega \leq 220 \text{ k}\Omega$. So, it is exact analysis.

$$R_{Th} = R_1 || R_2 = 82 \text{ k}\Omega || 22 \text{ k}\Omega = 17.35 \text{ k}\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= 22 \text{ k}\Omega (18 \text{ V}) / (82 \text{ k}\Omega + 22 \text{ k}\Omega)$$

$$= 3.81 \text{ V}$$



$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{3.81 - 0.7}{17.35 + (50)(1.2)} \text{ A}$$

$$= 39.6 \text{ mA}$$

$$I_{CQ} = \beta I_B = (50)(39.6 \text{ mA}) = 1.98 \text{ mA}$$

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$

$$= 18 \text{ V} - (1.98)(5.6 + 1.2)$$

$$= 4.54 \text{ V}$$

Dc Bias with Voltage Feedback:

Applying KVL,

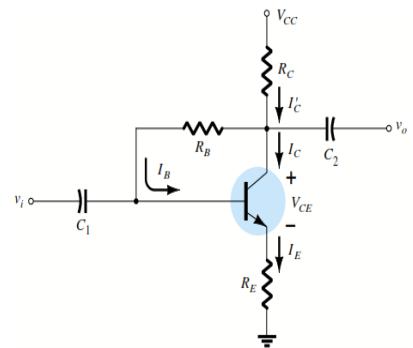
$$V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

**Example-4:**

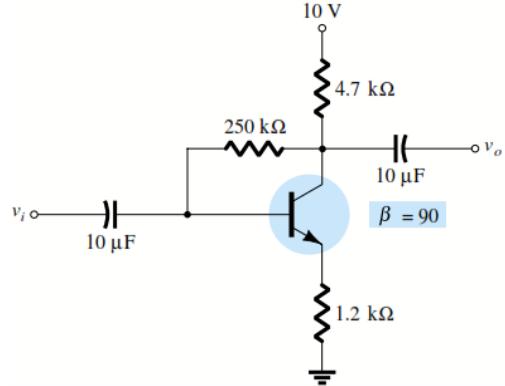
Determine I_{CQ} and V_{CEQ}

Solution:

$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \\ &= \frac{10 \text{ V} - 0.7 \text{ V}}{250 \text{ k}\Omega + (90)(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega)} \\ &= \frac{9.3 \text{ V}}{250 \text{ k}\Omega + 531 \text{ k}\Omega} = \frac{9.3 \text{ V}}{781 \text{ k}\Omega} \\ &= 11.91 \mu\text{A} \end{aligned}$$

$$\begin{aligned} I_{CQ} &= \beta I_B = (90)(11.91 \mu\text{A}) \\ &= 1.07 \text{ mA} \end{aligned}$$

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C (R_C + R_E) \\ &= 10 \text{ V} - (1.07 \text{ mA})(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega) \\ &= 10 \text{ V} - 6.31 \text{ V} \\ &= 3.69 \text{ V} \end{aligned}$$

**Possible Questions:**

Broad Questions:	Short Questions:	
1) Derivation of I_B and V_{CE} for fixed bias.	1) What is Transistor? Why dc biasing is necessary for transistor?	Mathematical Problems related to the module and class lecture.
2) Derivation of I_B and V_{CE} for emitter bias	2) Describe the doping level of emitter, base and collector.	
3) Derivation of I_B and V_{CE} for voltage divider bias.	3) What does the term bipolar reflect?	
4) Relation between α and β .	4) Why is it called transistor?	

Electronics I (EEE-201)
Course Teacher: Farhana Rahman
Lecture-06 (Module-06)

MOSFET/IGFET:

The full form of MOSFET is **Metal Oxide Semiconductor Field-Effect Transistors**. The full form of **IGFET** is **Insulated Gate FET**.

Why are MOSFET's more widely used?

- Size smaller
- Ease of manufacture
- Lesser power utilization
- It allows placement of approximately 2 billion transistors on a single IC.
- Backbone of very large scale integration (VLSI)

Device Structure:

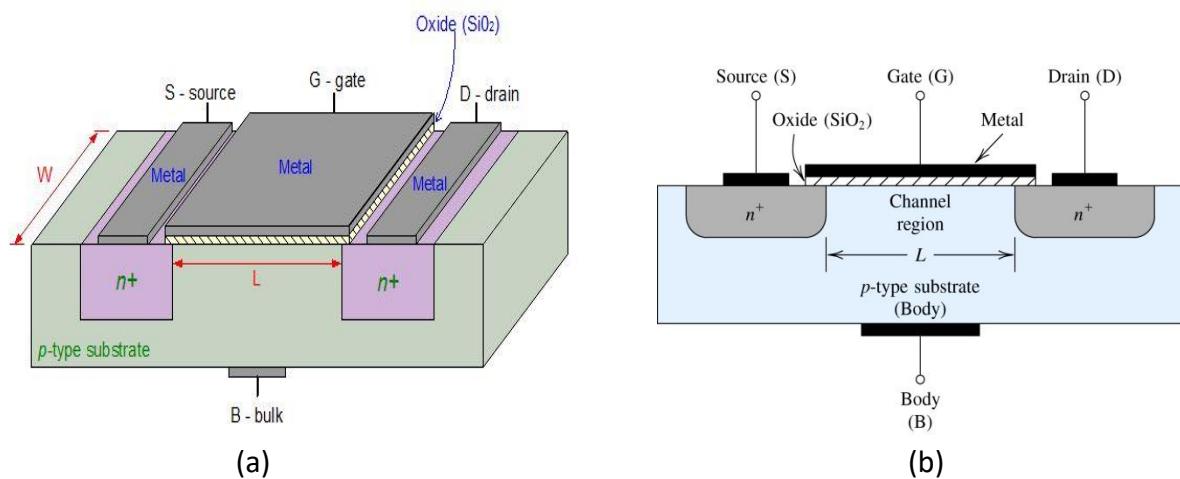


Fig. 1. Physical structure of the enhancement type N-MOS transistor; (a) perspective view; (b) cross-section

- Transistor fabricated on a p-type substrate
- Two heavily doped n-type regions n⁺ source and n⁺ drain are created in the substrate.
- Thin layer of silicon dioxide (SiO₂) (thickness, t_{ox} = 2-50 nm) is grown on the surface of the p-substrate as a insulator.
- Metal on the top of the oxide forms the **gate electrode** of the device.
- The four terminals are: gate (G), source (S), drain (D) and body (B)

Operation with No Gate Voltage:

- With zero voltage applied to gate, two back-to-back diodes exist in series between drain and source.
- They prevent current from drain to source when a voltage v_{DS} is applied.

Creating a Channel for Current Flow:

What happens if (1) source and drain are grounded and (2) positive voltage is applied to gate?

- v_{GS} is applied to the gate terminal, causing a positive build up of positive charge along metal electrode.
- This “build up” causes free holes to be repelled from region of p-type substrate under gate.
- This “migration” results in the uncovering of negative **bound charges**, originally neutralized by the free holes
- The positive gate voltage also attracts electrons from the n^+ source and drain regions into the channel.
- Once a sufficient number of these electrons accumulate, an n-region is created and connects the source and drain region.
- Thus a path is provided to for current from D to S.

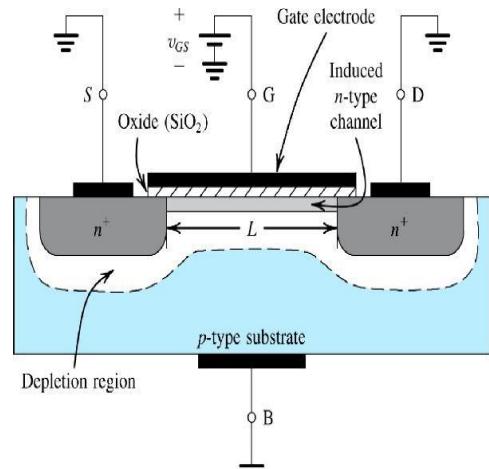


Fig. 2 . Physical structure of the enhancement type N-MOS transistor with positive gate voltage

Threshold Voltage (V_t) – is the minimum value of v_{GS} required to form a conducting channel between drain and source (typically between 0.3 and 0.6V)

Field-effect – when positive v_{GS} is applied, an electric field develops between the gate electrode and induced n-channel, the conductivity of this channel is affected by the strength of field. SiO₂ layer acts as dielectric

Effective / Overdrive voltage – is the difference between v_{GS} applied and V_t .

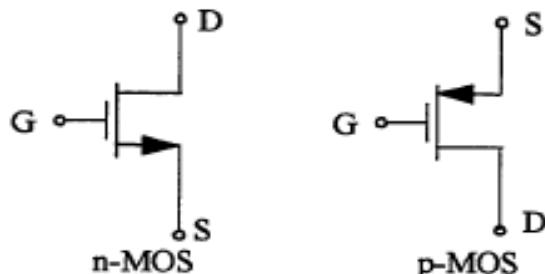
$$v_{OV} = v_{GS} - V_t$$

Oxide Capacitance (C_{ox}) – is the capacitance of the parallel plate capacitor per unit gate area (F/m^2)

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \text{ in } F/m^2$$

Where ϵ_{ox} = *permittivity of the Silicon oxide* = 3.9 ϵ_0 = $3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} F/m$
 t_{ox} = *oxide thickness*

Circuit Symbol:



Applying Small v_{DS} : For small values of v_{DS} n-channel acts like a variable resistance whose value is controlled by v_{ov}

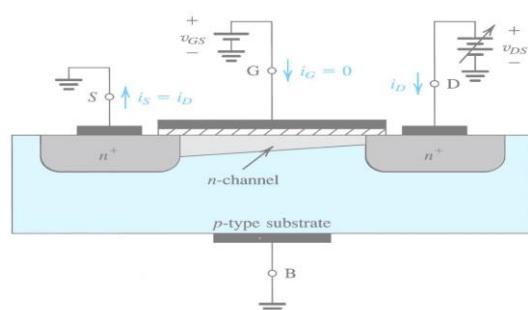
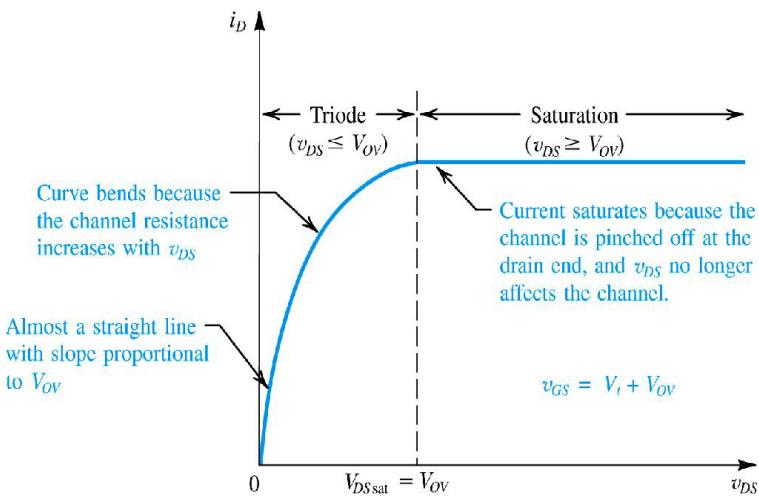


Fig. 2 . Operation of e-NMOS as v_{DS} Is increased



In triode region,

$$\begin{aligned} i_D &= (\mu_n C_{ox}) \left(\frac{W}{L} \right) [(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2] \\ &= k_n \left(\frac{W}{L} \right) [(v_{GS} - v_t)v_{DS} - \frac{1}{2}v_{DS}^2] \dots \text{(1)} \end{aligned} \quad \text{Where, } k_n = \mu_n C_{ox}$$

In saturation region,

$$i_D = \frac{1}{2} k_n \left(\frac{W}{L} \right) (v_{GS} - v_t)^2 \dots \text{(2)} \quad \text{Where, } k_n = \mu_n C_{ox}$$

I_D = drain current

C_{ox} = capacitance per unit area

μ_n = mobility of electrons

W = aspect ratio of the MOSFET

L = channel length

Example-1:

For a MOSFET, gate voltage is 3 V, threshold voltage is 0.7 V, drain voltage is 5 V, and source is connected to ground. Determine the state of MOSFET.

Solution:

$$v_{GS} - v_t = (3 - 0.7)V = 2.3 \text{ V}$$

$$v_{DS} = 5 \text{ V}$$

$\therefore v_{DS} > v_{GS} - v_t$, so the MOSFET is in the saturation state.

MOSFET circuits at DC:

Example-2:

Consider a process technology for which $L=0.4 \mu\text{m}$, $t_{ox}=8 \text{ nm}$, $\mu_n=450 \text{ cm}^2/\text{V.s}$ and $V_t=0.7 \text{ V}$.

- (a) Find C_{ox} and k_n^2 ; (b) With $W/L=8 \mu\text{m}/0.8 \mu\text{m}$, calculate the values of v_{GS} and $v_{DS \min}$ needed to operate the transistor in the saturation region with a dc current $I_D=100 \mu\text{A}$.

Solution:

$$(a) C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}}{8 \times 10^{-9}} = 4.32 \times 10^{-3} \text{ F/m}^2$$

$$k_n = \mu_n C_{ox} = 450 \times 4.32 \times 10^{-3} = 194 \times 10^{-6} = 194 \mu\text{A/V}^2$$

(b) For operation in the saturation region,

$$\begin{aligned} i_D &= \frac{1}{2} k_n \frac{W}{L} (v_{GS} - v_t)^2 \\ \Rightarrow 100 &= \frac{1}{2} \times 194 \times \frac{8}{0.8} (v_{GS} - v_t)^2 \\ \Rightarrow v_{GS} - 0.7 &= 0.32 \text{ V} \\ \Rightarrow v_{GS} &= 1.02 \text{ V} \\ \text{and, } v_{DS\min} &= v_{GS} - v_t = 0.32 \text{ V} \end{aligned}$$

Example-3:

Design the circuit that the transistor operates at $I_D = 0.4 \text{ mA}$ and $V_D = +0.5 \text{ V}$. The NMOS transistor has $V_t = 0.7 \text{ V}$, $\mu_n C_{ox} = 100 \mu\text{A/V}^2$, $L = 1 \mu\text{m}$ and $W = 32 \mu\text{m}$.

Solution:

$$V_D = 0.5 \text{ V} \Rightarrow V_G = 0 \text{ V},$$

NMOS transistor operating in the saturation region.

$$\begin{aligned} I_D &= \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_t)^2 \\ \Rightarrow 0.4 \text{ mA} &= \frac{1}{2} \times 100 \mu\text{A} / V^2 \times \frac{32}{1} (V_{GS} - V_t)^2 \end{aligned}$$

$$\Rightarrow 400 = \frac{1}{2} \times 100 \times (V_{GS} - V_t)^2$$

$$\Rightarrow (V_{GS} - V_t)^2 = 0.25 \text{ V}$$

$$\Rightarrow V_{GS} - V_t = 0.5 \text{ V}$$

Thus,

$$V_{GS} = 0.5 \text{ V} + V_t = 0.5 \text{ V} + 0.7 \text{ V} = 1.2 \text{ V}$$

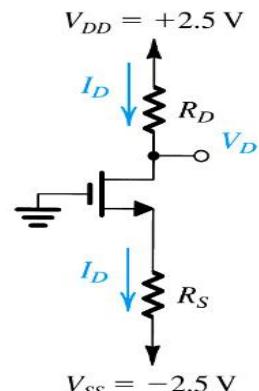
$$\text{Now, } V_{GS} = V_G - V_S = 0 - V_S = -V_S$$

$$\Rightarrow 1.2 \text{ V} = -V_S$$

$$\therefore V_S = -1.2 \text{ V}$$

$$\therefore R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ K}\Omega$$

$$\therefore R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5 \text{ K}\Omega$$



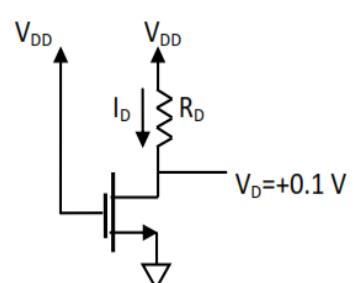
Try yourself:

Redesign the circuit of example-3 that the transistor operates at $V_{DD} = -V_{SS} = 2.5 \text{ V}$, $I_D = 0.3 \text{ mA}$ and $V_D = +0.4 \text{ V}$. The NMOS transistor has $V_t = 1 \text{ V}$, $\mu_n C_{ox} = 60 \mu\text{A/V}^2$, $L = 3 \mu\text{m}$ and $W = 120 \mu\text{m}$.

Example-4:

Design the circuit to establish a drain voltage of 0.1 V . What is the resistance between drain and source at this operating point? Let $V_t = 1 \text{ V}$, $K_n'(W/L) = 1 \text{ mA/V}^2$, $V_{DD} = +5 \text{ V}$.

Solution:



$$V_D = 0.1 \text{ V} < V_G = 5 \text{ V},$$

NMOS transistor operating in the triode region.

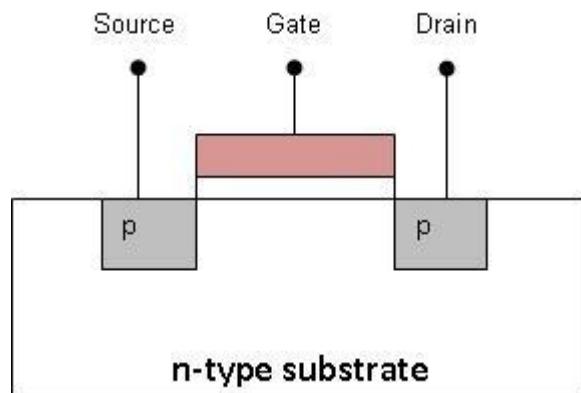
$$I_D = k_n \left(\frac{W}{L} \right) [(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$\Rightarrow I_D = 1 \times [(5 - 1) \times 0.1 - \frac{1}{2} \times 0.01]$$

$$\therefore I_D = 0.395 \text{ mA}$$

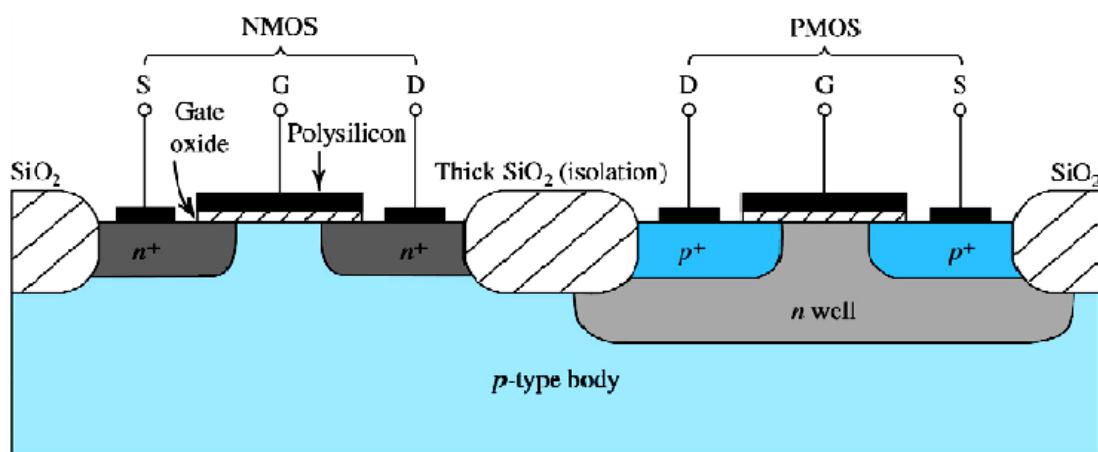
$$\therefore R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5 - 0.1}{0.395} = 12.4 \text{ K}\Omega$$

The p-Channel MOSFET:



Complementary MOS or CMOS:

- CMOS employs MOS transistors of both polarities.
- More difficult to fabricate
- More powerful and flexible
- More prevalent than NMOS or PMOS



Possible Questions:

Broad Questions:	Short Questions:	
1) Describe the structure of a NMOS device.	1) Define: Threshold voltage (V_t) for a MOSFET.	Mathematical Problems related to the module and class lecture.
2) How does a channel create for current flow in a NMOS transistor?	2) Draw the physical structure for a NMOS/PMOS and their circuit symbol.	
	3) Why are MOSFET's more widely used?	
	4) What is Complementary MOS or CMOS? Draw the physical structure of a CMOS.	