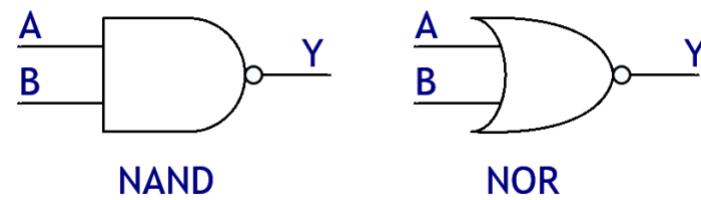


ELEC 527 Homework 1

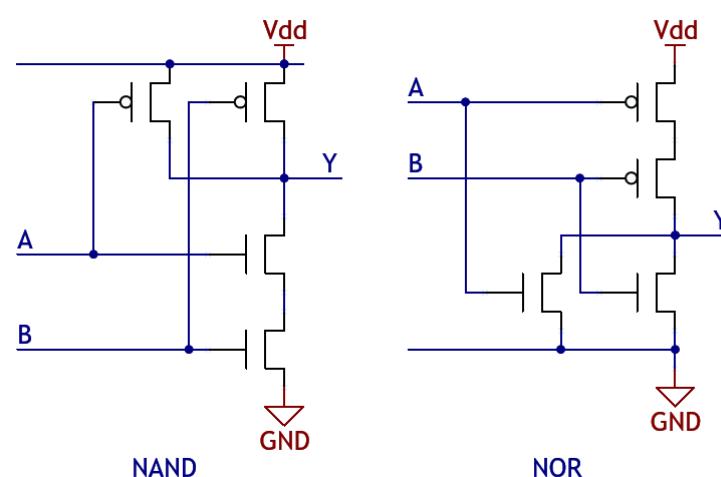
Name: Yufei Gu NetID: yg77

1. Basic Logic - NAND gate, NOR gate

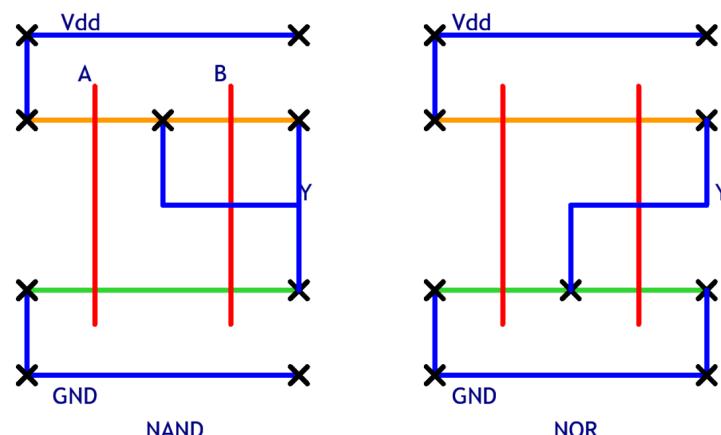
1. Logic diagram



2. Transistor diagram

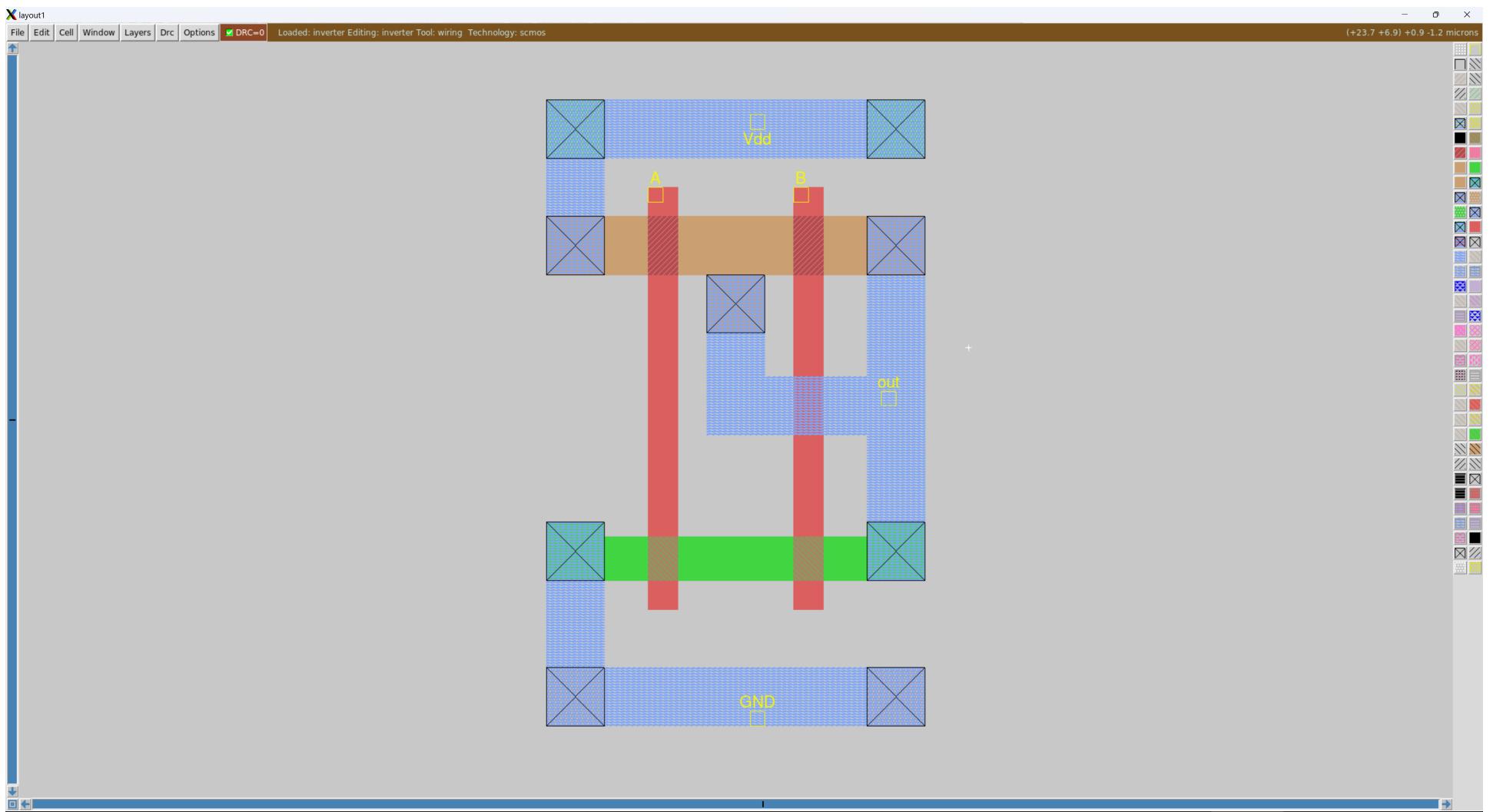


3. Stick Diagram

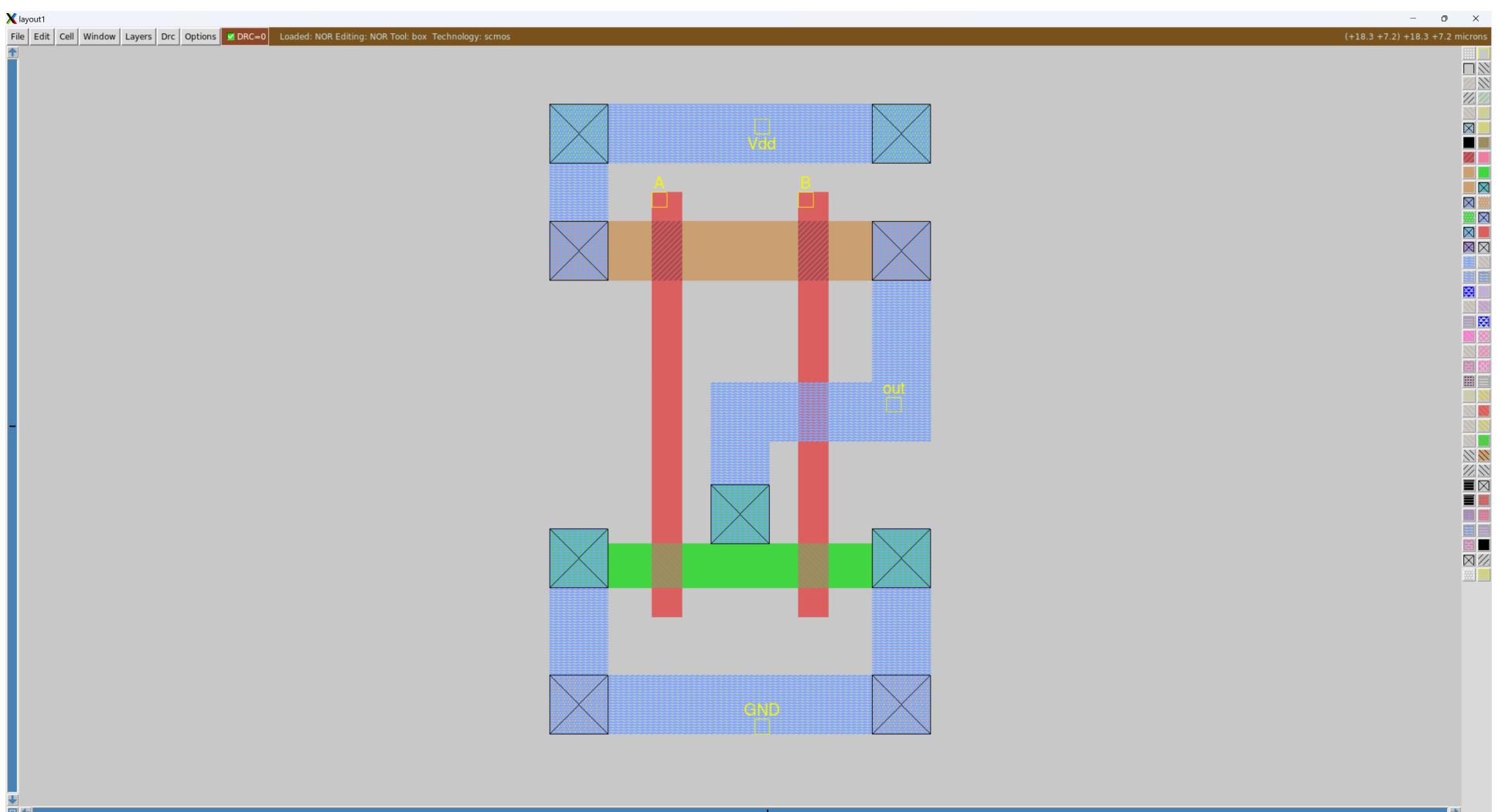


4. Magic

- NAND Gate



- NOR Gate



5. Irsim

- NAND Gate

```

|
| NAND.cmd.txt
|
| Comments
| Elec422/527
| CMOS NAND for AMI05
|
| Spring 2023
|
| logfile padtest_sim.log
ana A B out

```

```

V      A 0 0 1 1 0 1 0 0 1 0 1
V      B 0 1 0 1 1 0 1 1 1 0 0
clock vdd 1
R

```

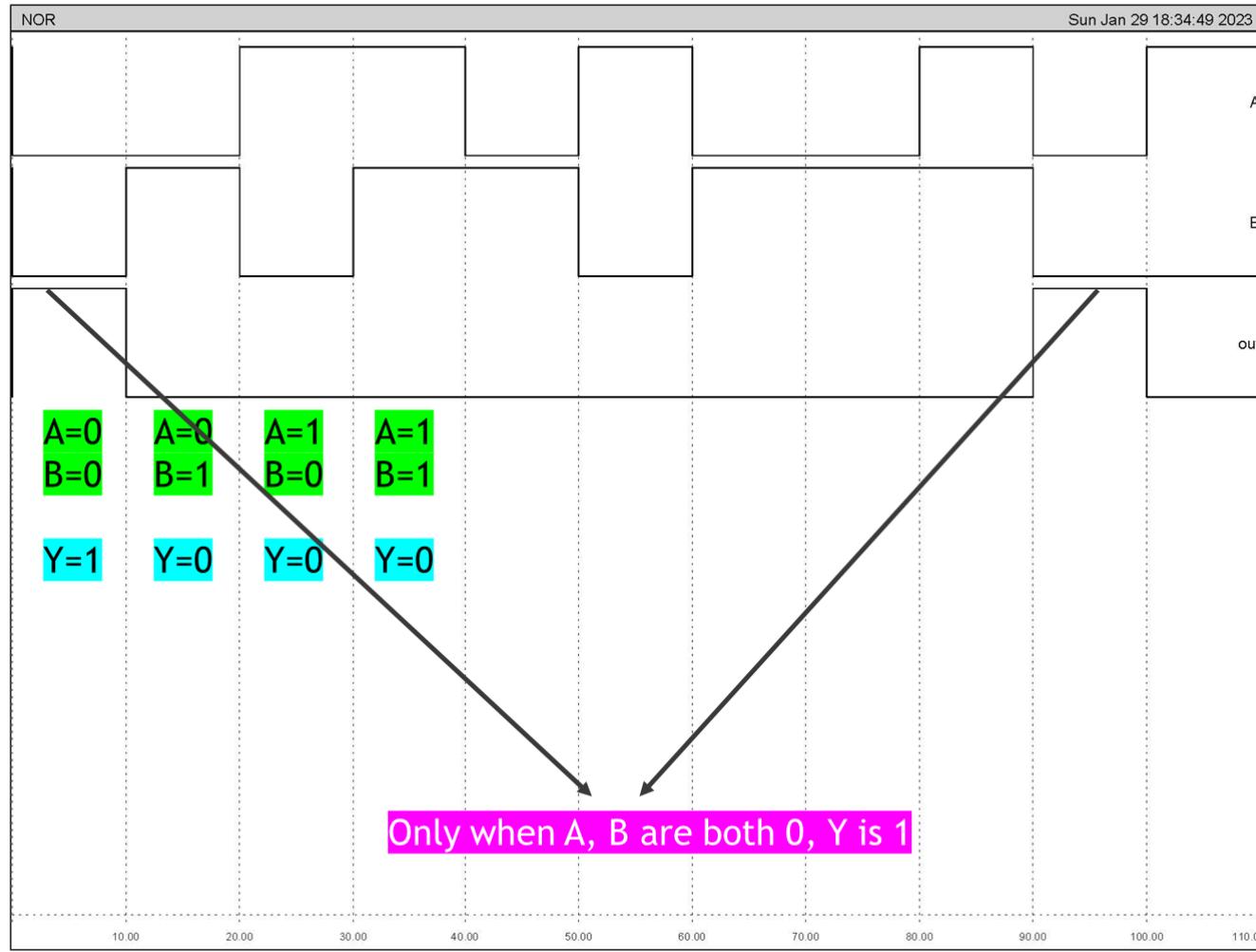


- NOR Gate

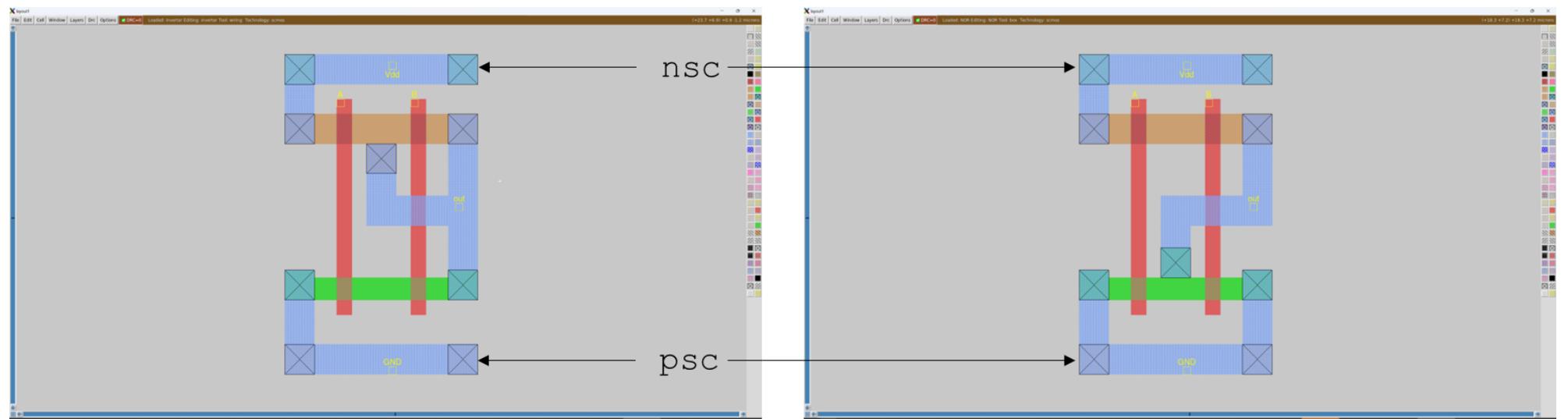
```

|
| NOR.cmd.txt
|
| Comments
| Elec422/527
| CMOS NOR for AMI05
|
| Spring 2023
|
| logfile padtest_sim.log
ana A B out
V      A 0 0 1 1 0 1 0 0 1 0 1
V      B 0 1 0 1 1 0 1 1 1 0 0
clock vdd 1
R

```

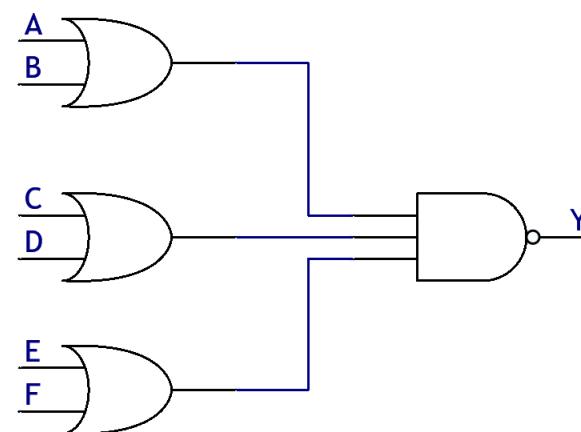


6. Sufficient Substrate contacts

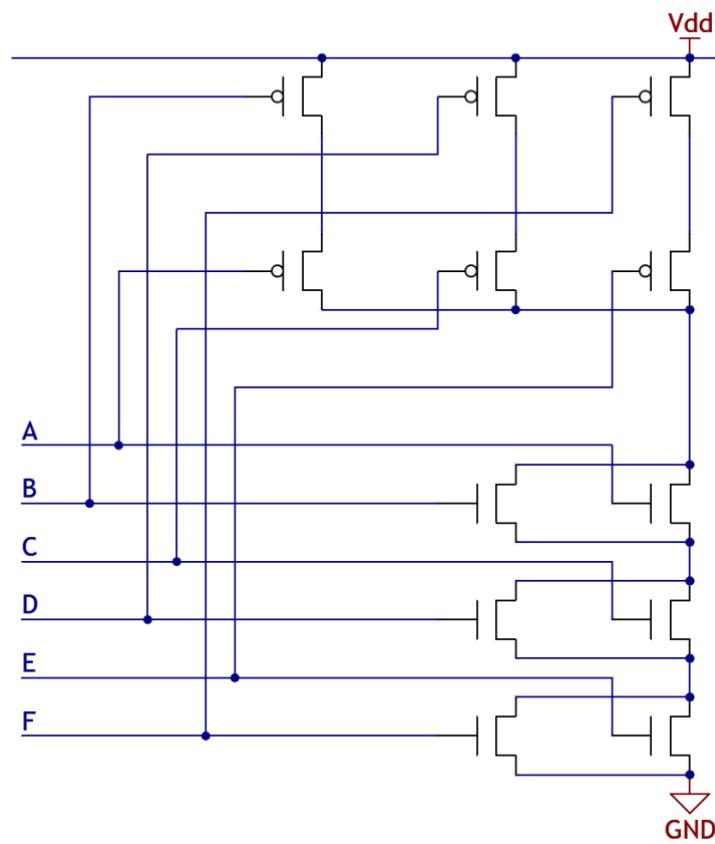


2. Logic Expression Compound Gate

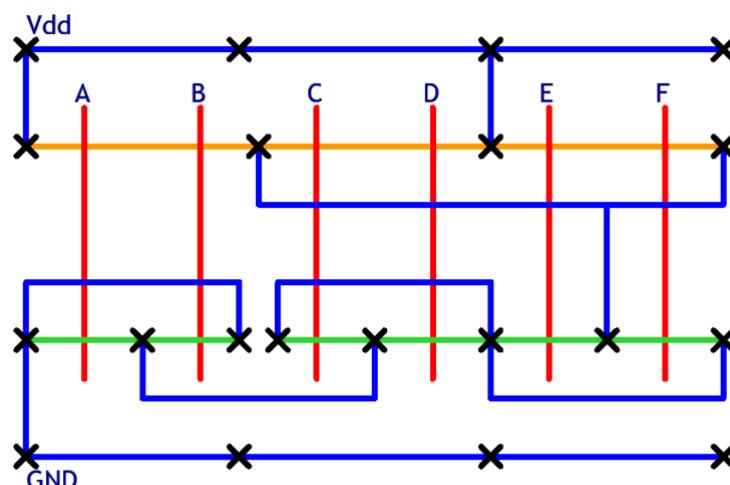
1. Logic diagram



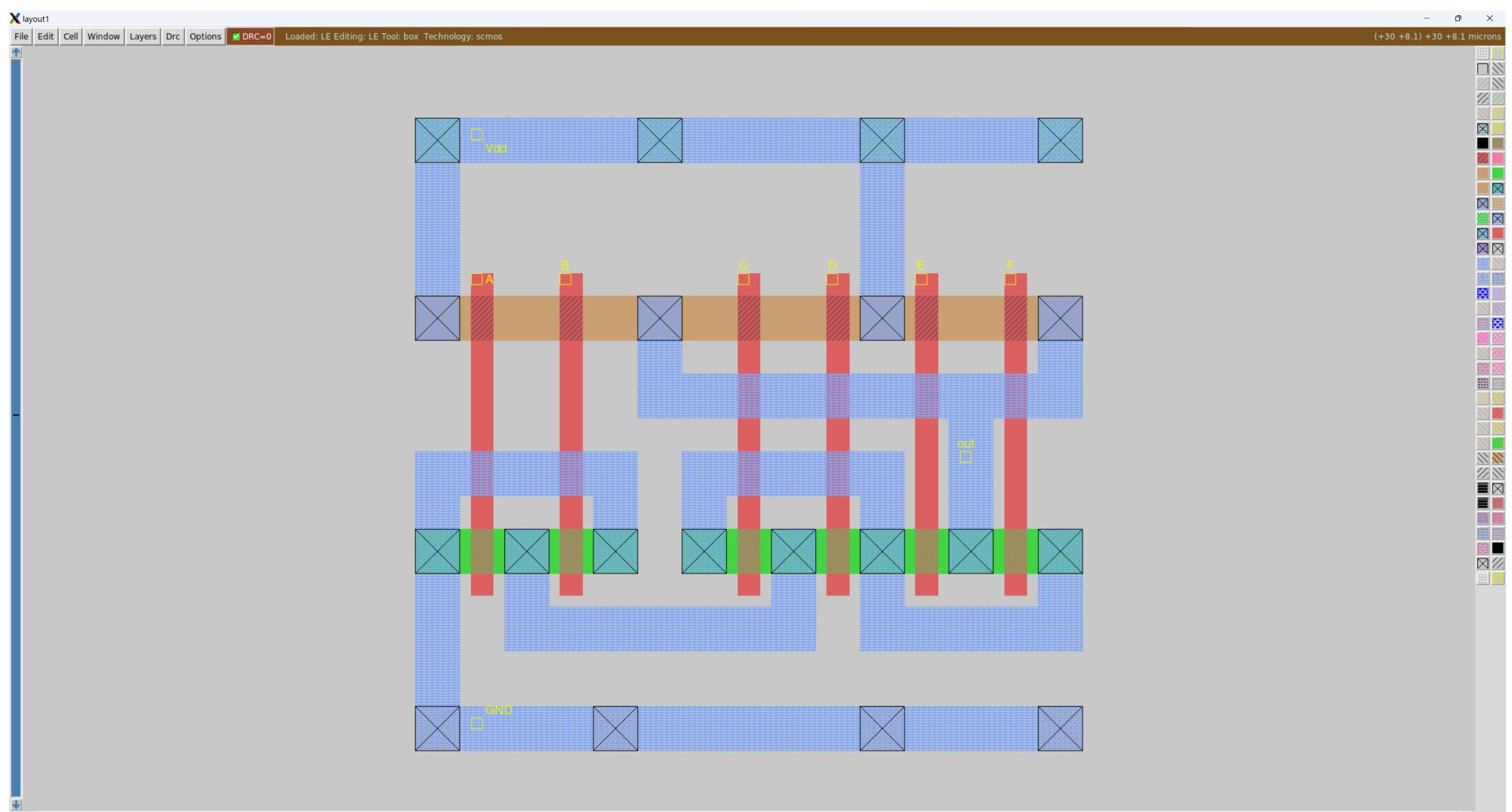
2. Transistor diagram



3. Stick Diagram



4. Magic

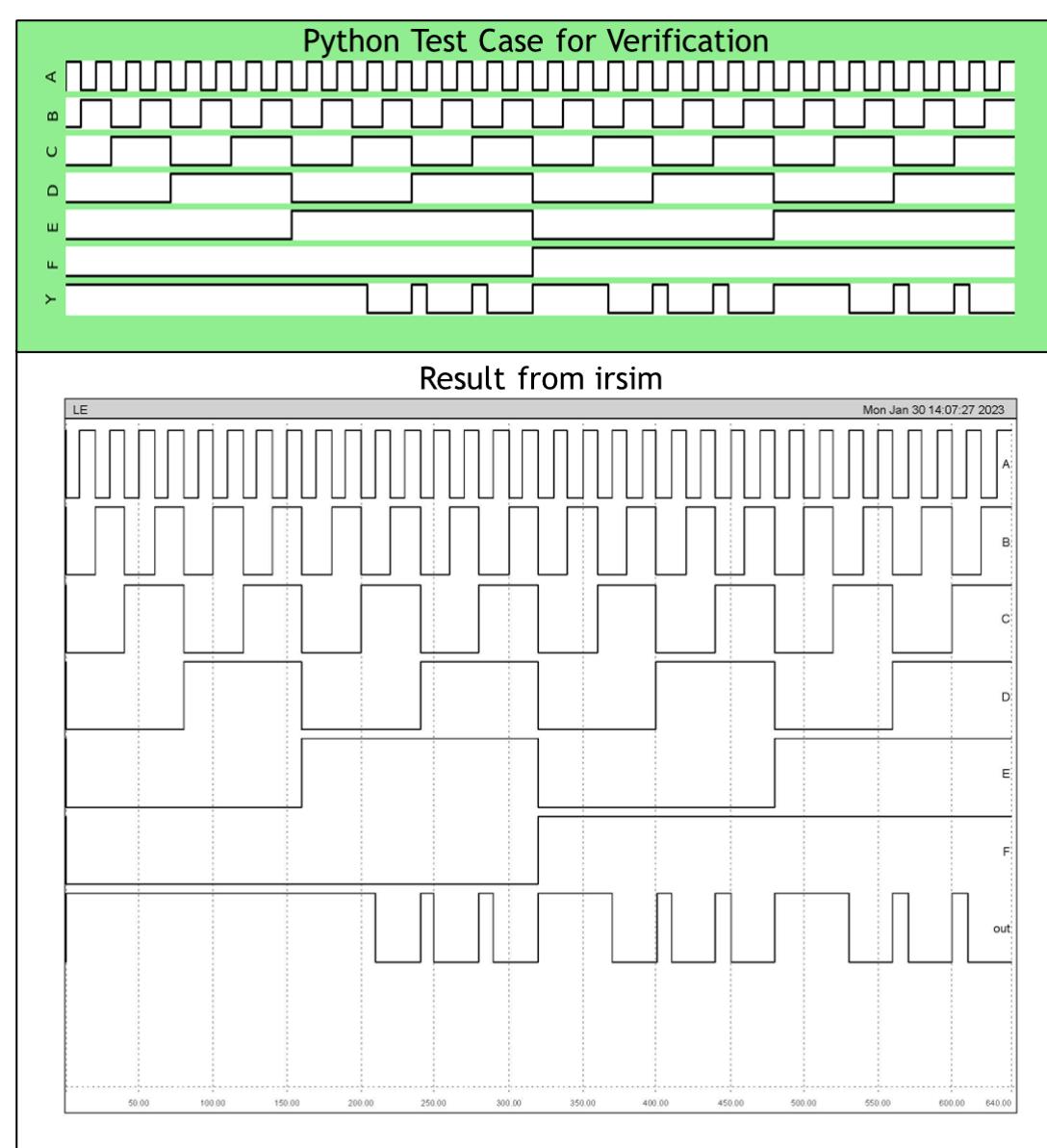


5. Irsim

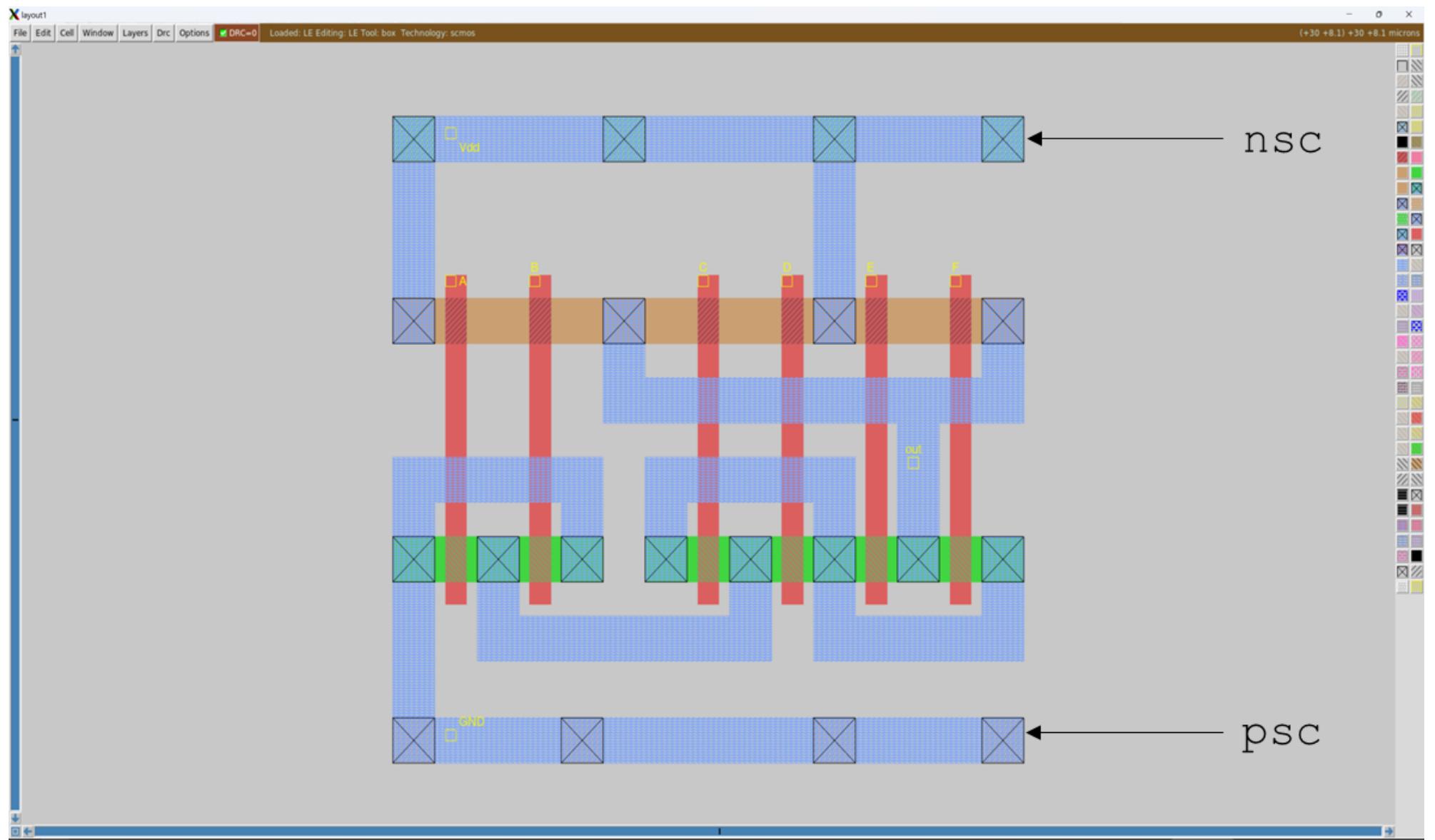
```

|_
| LE.cmd.txt
|_

```

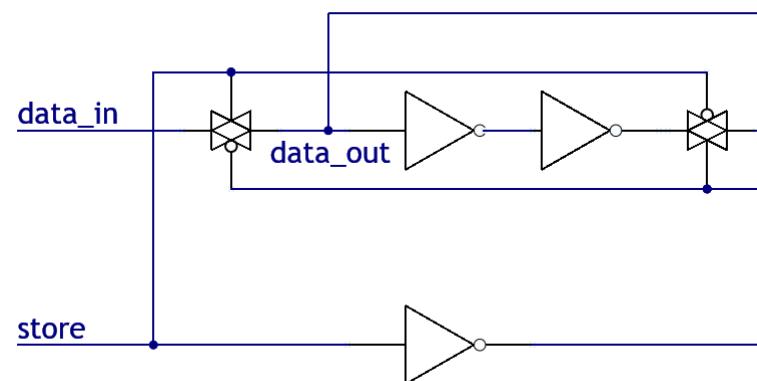


6. Sufficient Substrate contact

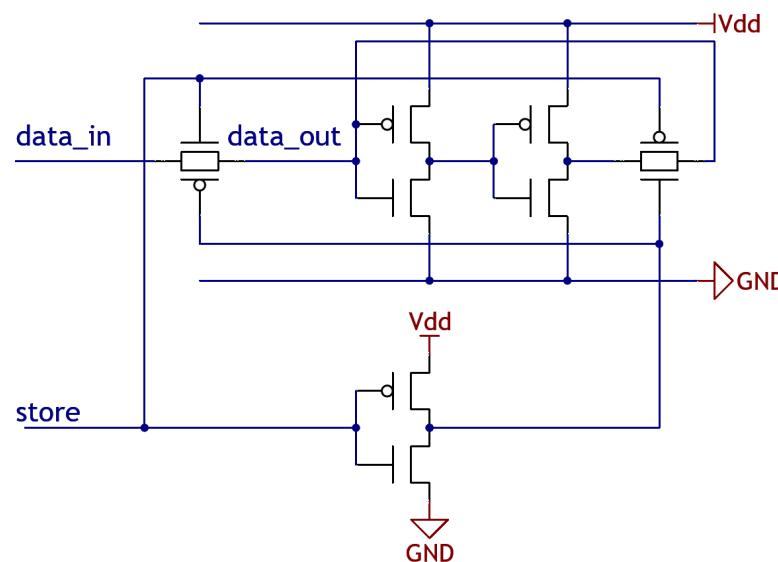


3. Static Latch

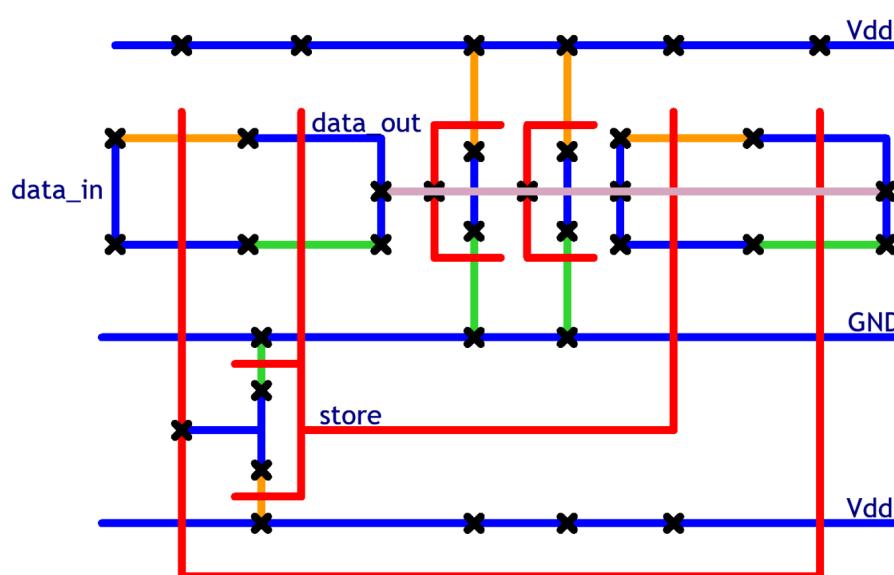
1. Logic diagram



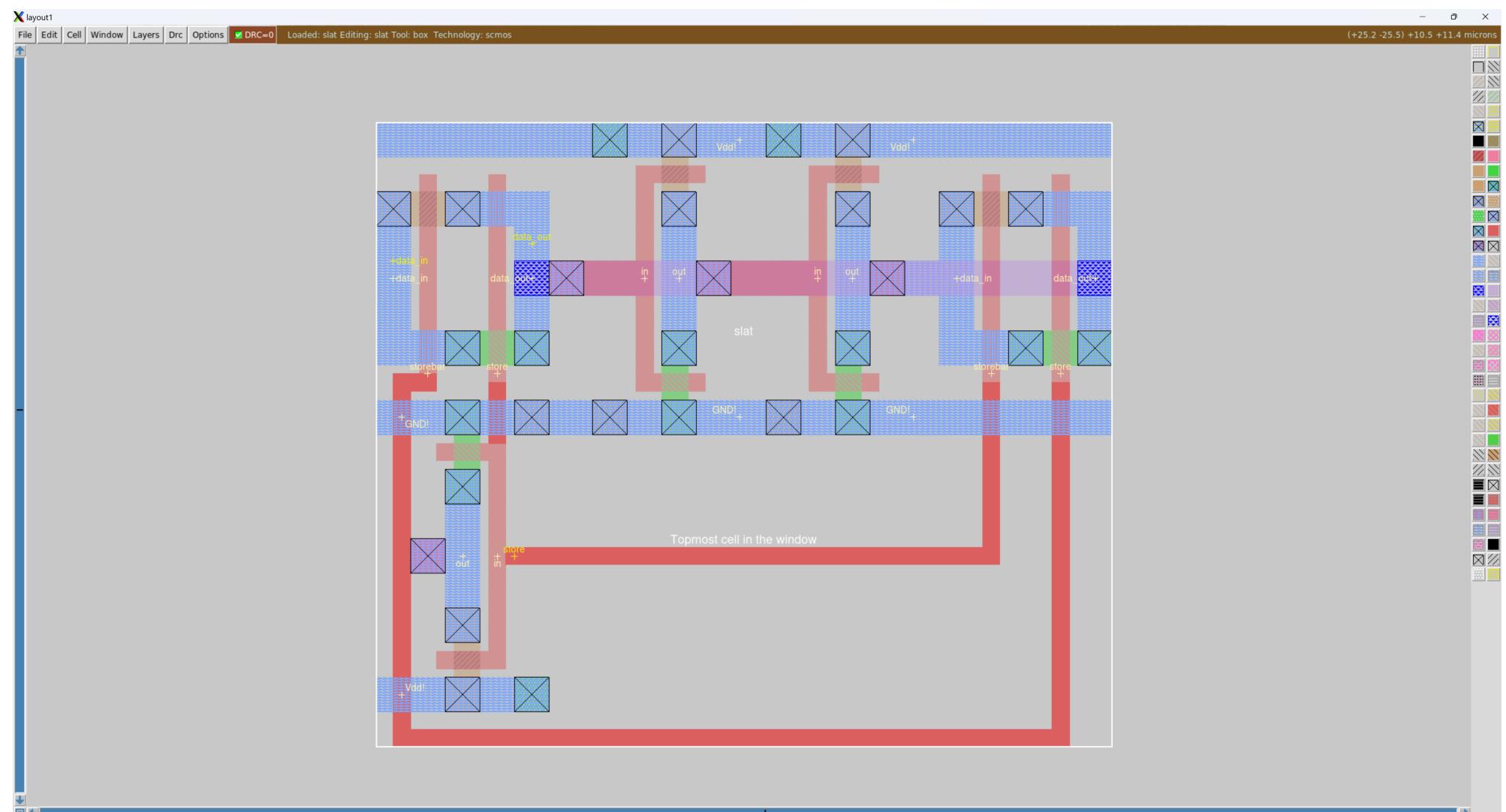
2. Transistor diagram



3. Stick Diagram



4. Magic



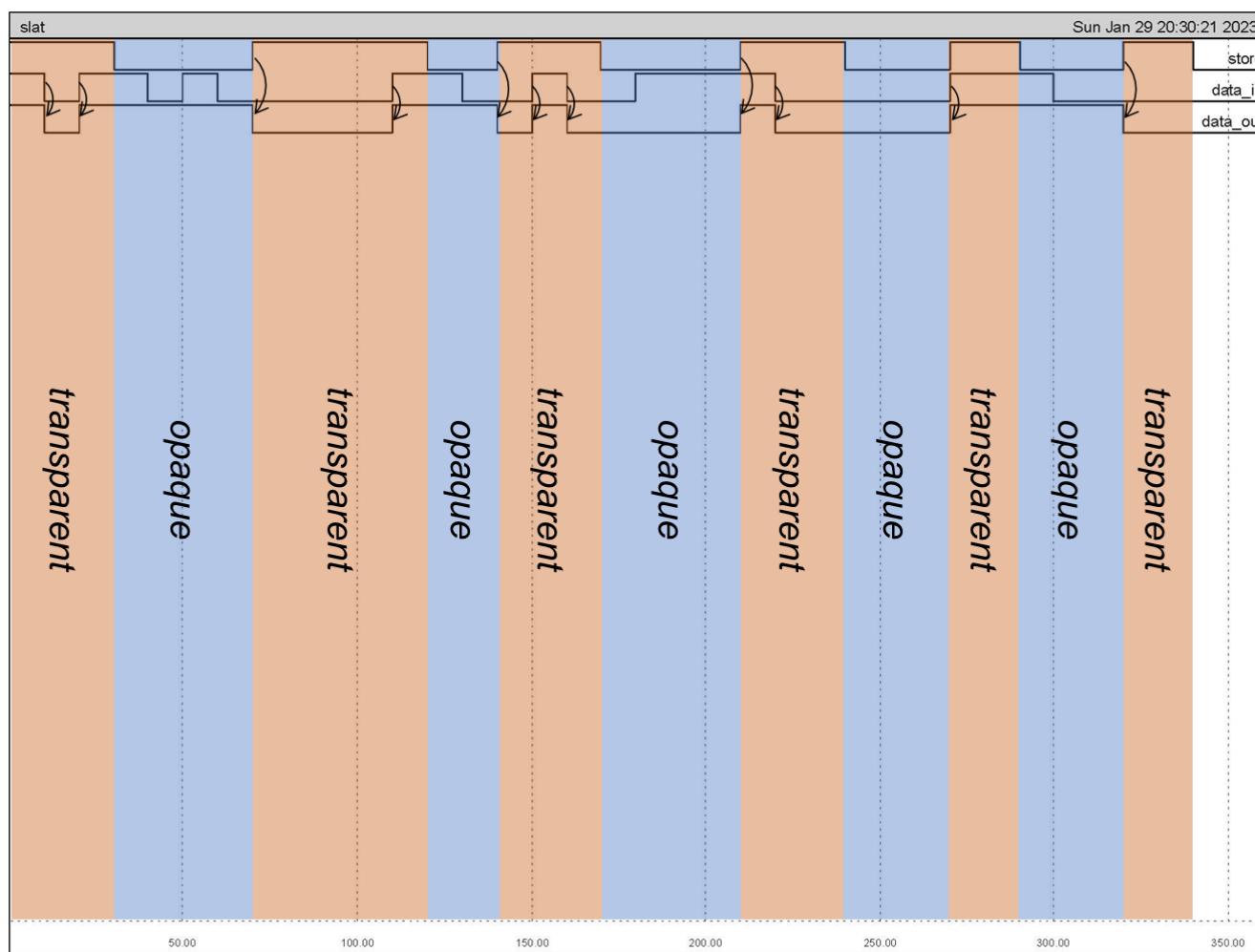
5. Irsim

- slat.cmd

```
|  
| slat.cmd.txt  
|  
| Comments  
| E1ec422/527 HW1 Problem 3  
| CMOS Static Latch  
| Spring 2023  
|  
| Please submit the output generated by irsim for this command file  
| clock definition of vdd as constant 1 allows irsim to read  
| the v input commands without a real clock signal in this problem  
| Please MARK UP the irsim output with color highlights to  
| to explain in words what is happening with each store sequence  
| in terms of data_in values captured.  
|  
logfile slat.log  
ana store data_in data_out  
v store 1 1 1 0 0 0 0 1 1 1 1 1 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0  
v data in 1 0 1 1 0 1 0 0 0 0 0 1 1 0 0 1 0 0 1 1 1 1 0 0 0 0 0 1 1 1 1 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0
```

```
clock vdd 1
```

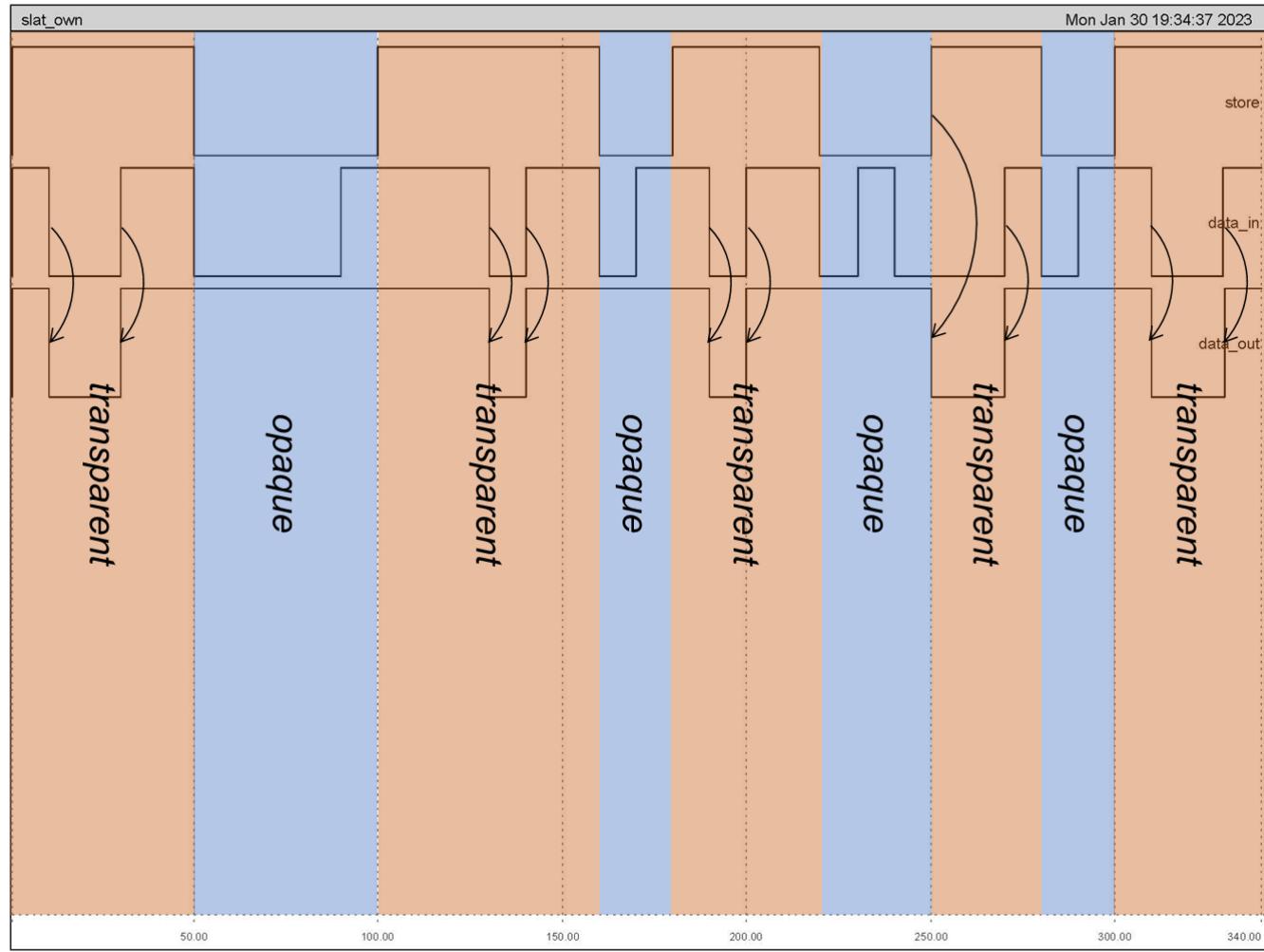
```
R
```



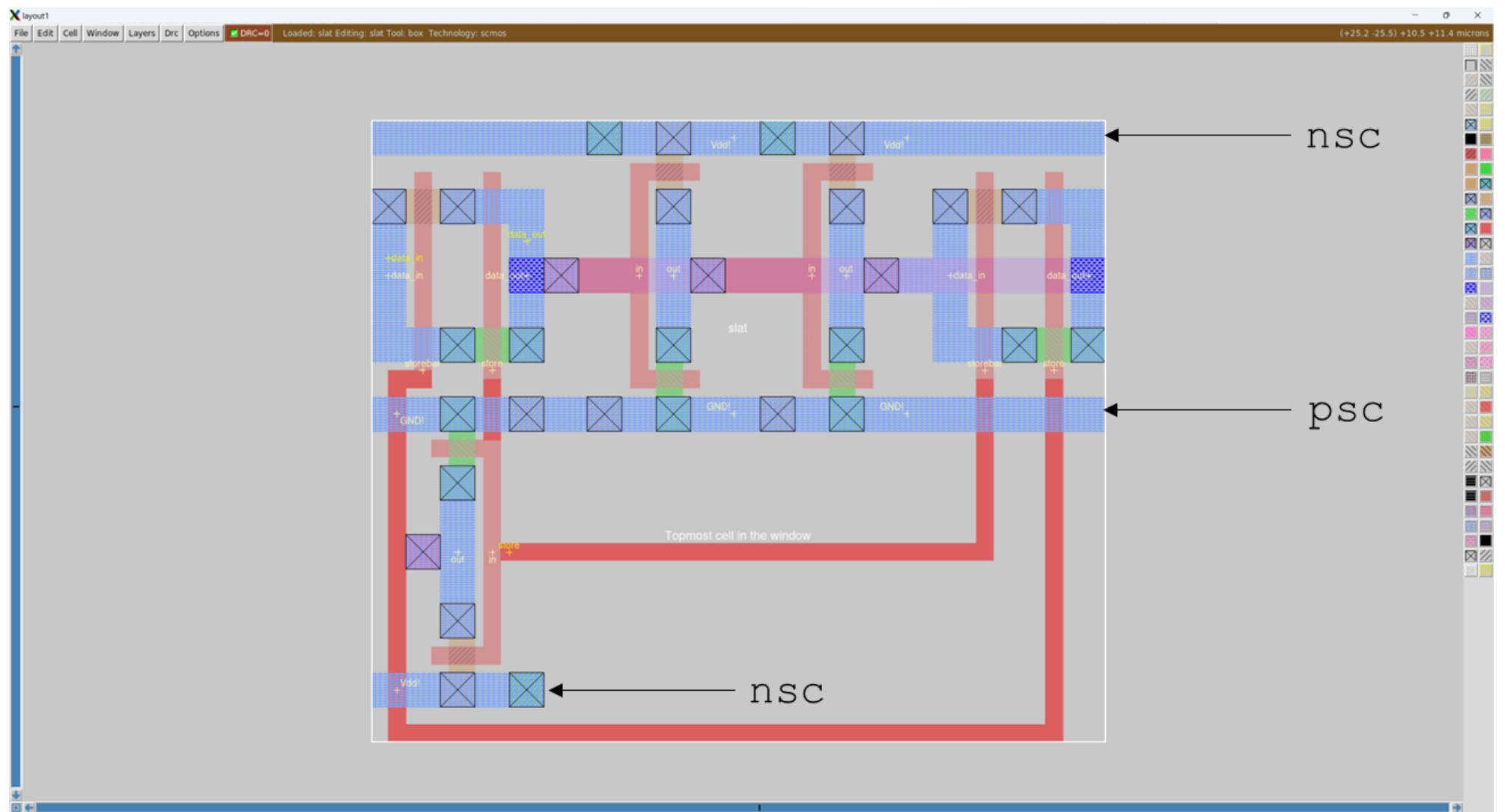
When the store is high, the latch input and output are transparent, and when the store is low, the latch holds the last value.

- `slat_own.cmd`

```
|  
| slat_own.cmd.txt  
|  
| Comments  
| Elec422/527 HW1 Problem 3  
| CMOS Static Latch  
| Spring 2023  
|  
| Please submit the output generated by irsim for this command file  
| clock definition of vdd as constant 1 allows irsim to read  
| the v input commands without a real clock signal in this problem  
| Please MARK UP the irsim output with color highlights to  
| to explain in words what is happening with each store sequence  
| in terms of data_in values captured.  
|  
logfile slat.log  
ana store data_in data_out  
v store    1 1 1 1 1 0 0 0 0 0 1 1 1 1 1 0 0 1 1 1 1 0 0 0 1 1 1 1 0 0 1 1 1 1  
v data_in  1 0 0 1 1 0 0 0 0 1 1 1 1 0 1 1 0 1 1 0 1 1 0 1 0 0 0 1 0 1 1 0 0 1  
clock vdd 1  
R
```

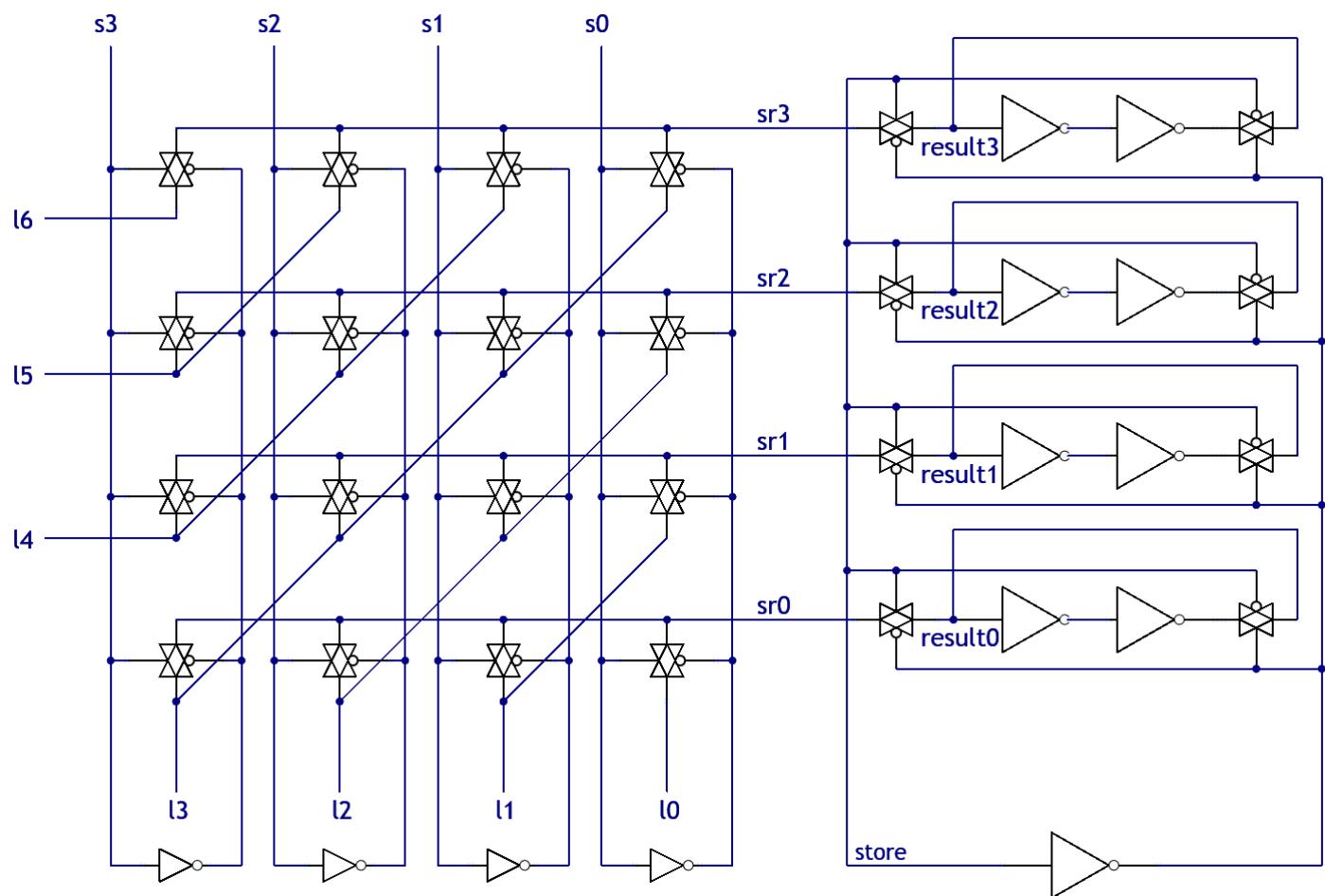


6. Sufficient Substrate contacts

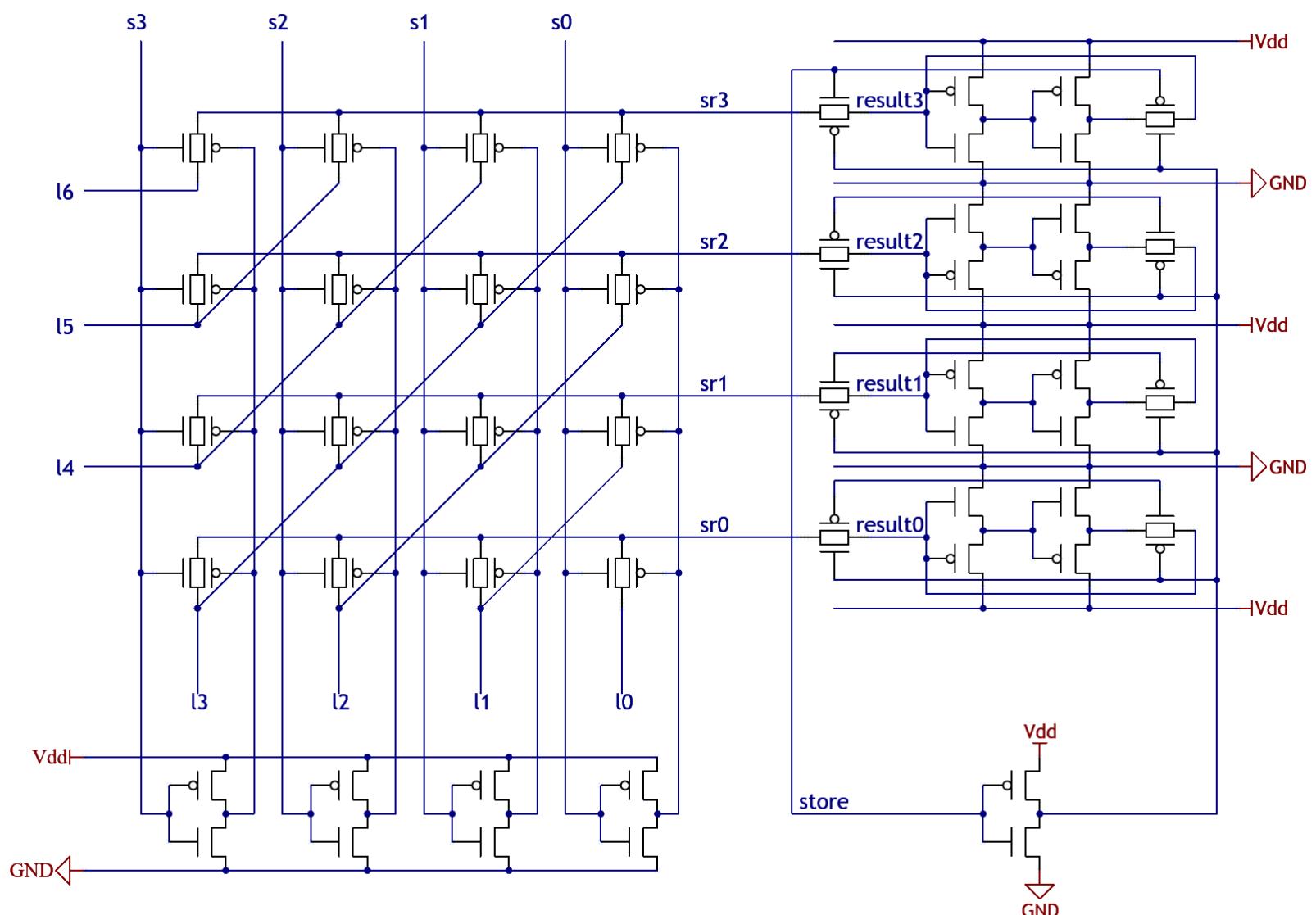


4. Barrel Shifter

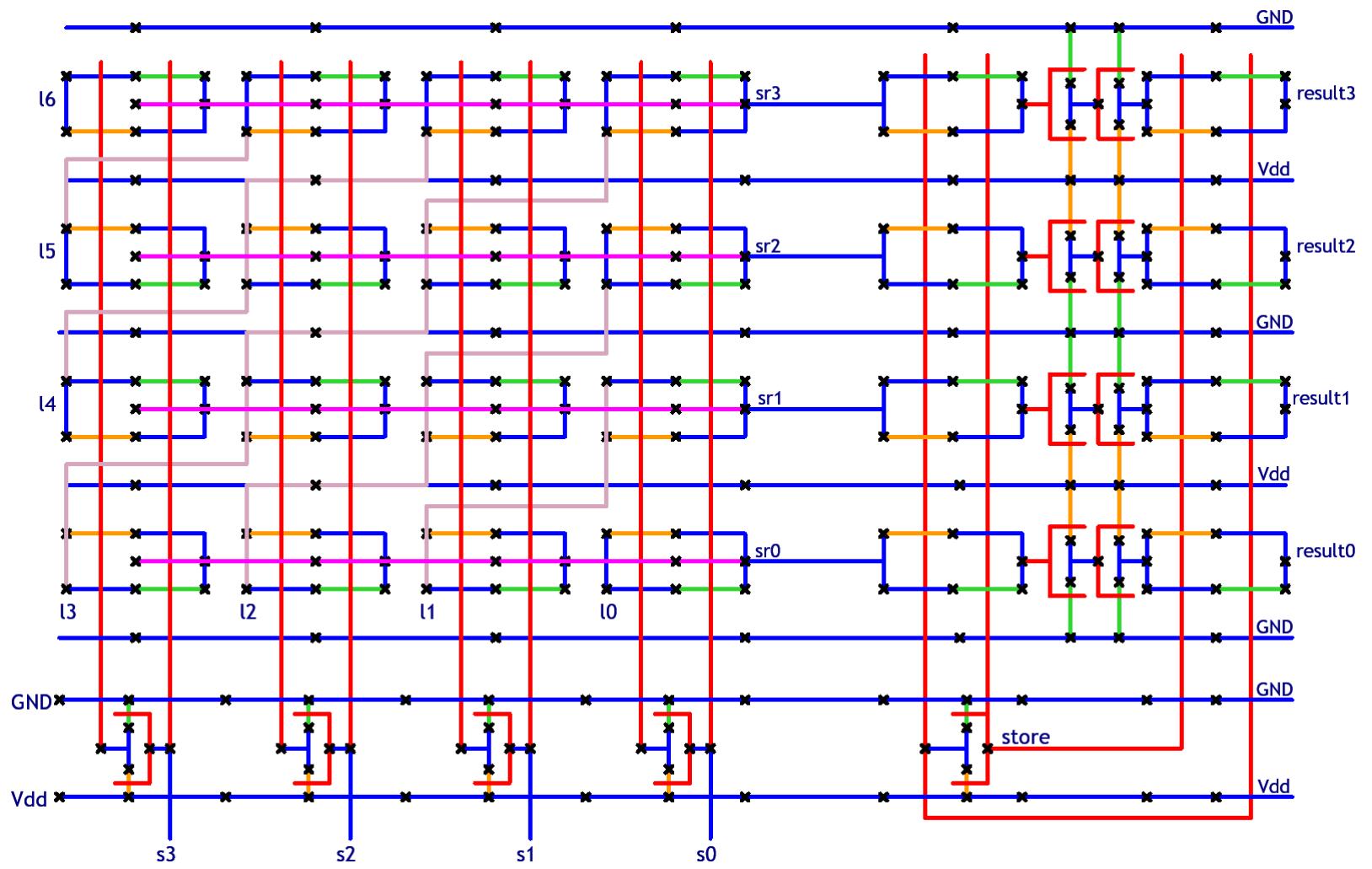
1. Logic diagram - complete



2. Transistor diagram - complete



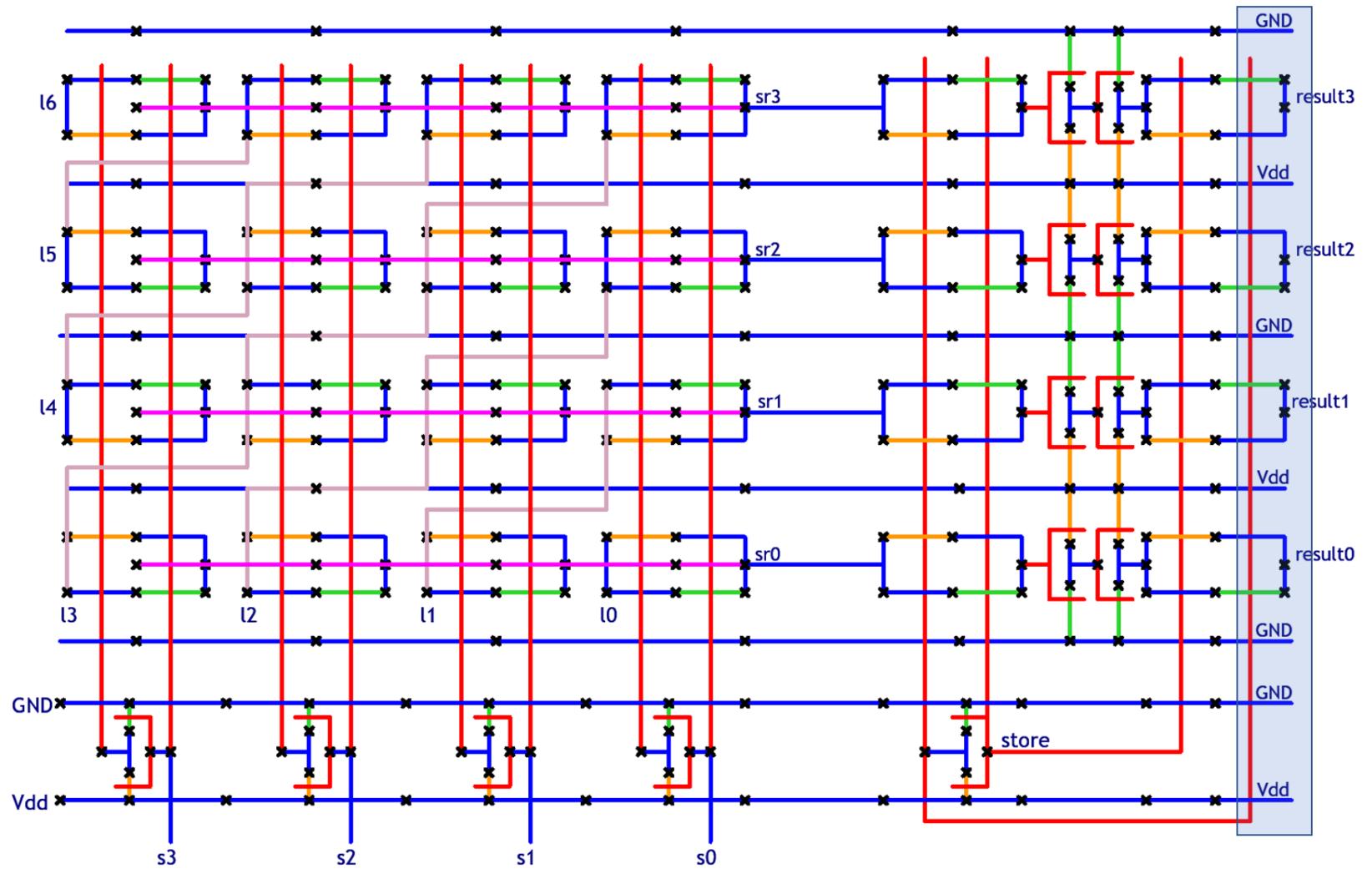
3. Stick Diagram - complete



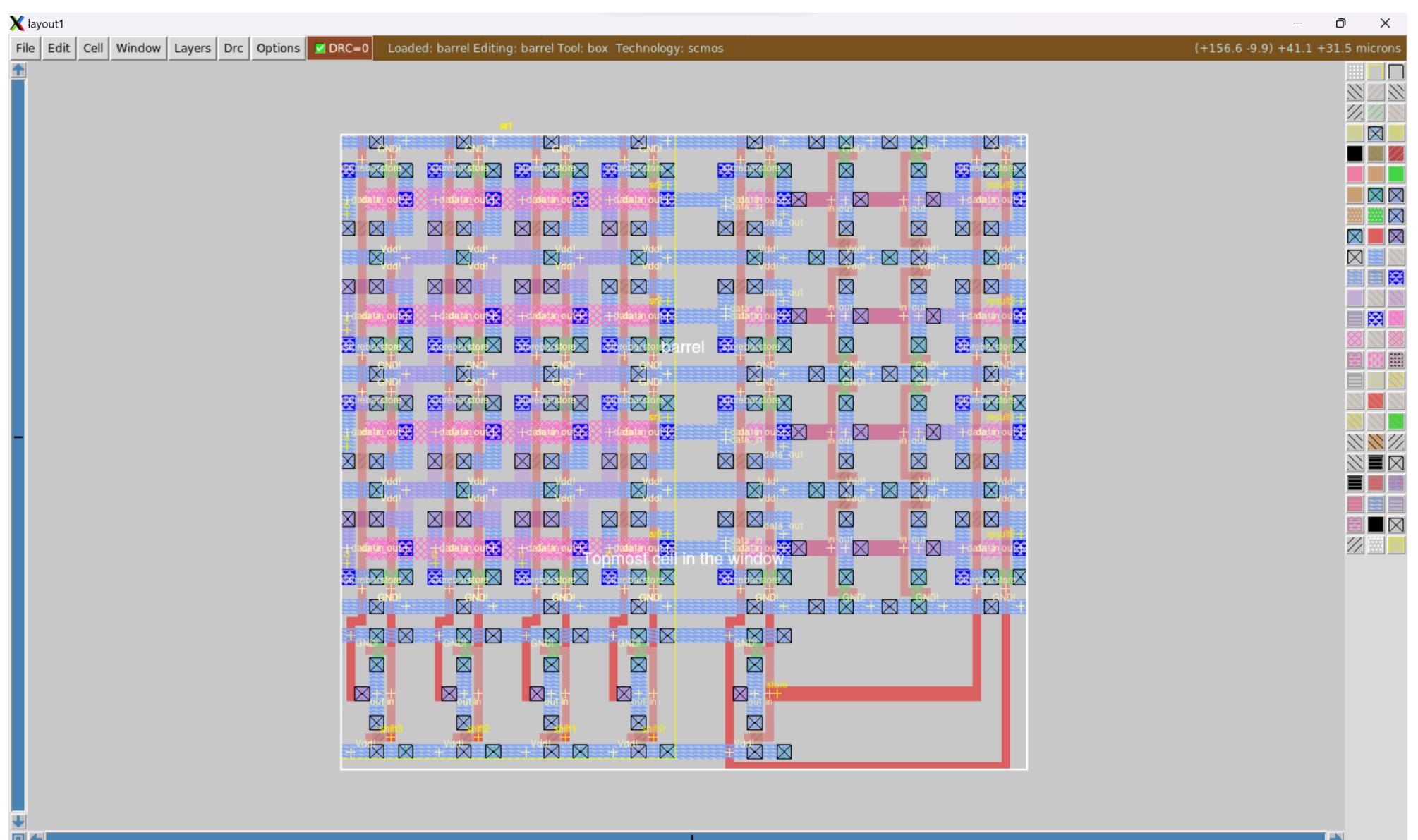
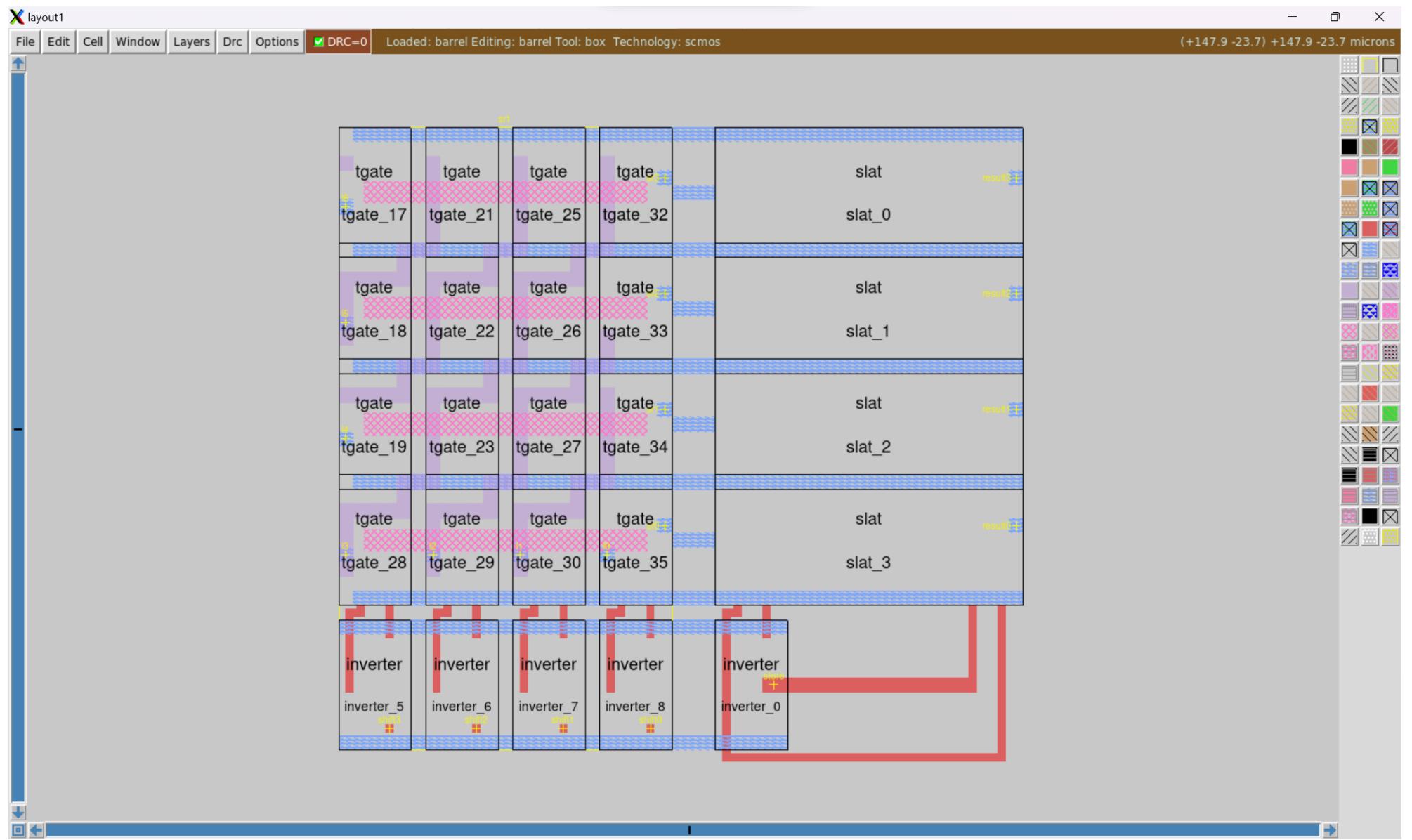
4. Alternate mirroring of barrel columns and latch bit rows

Mirroring is used, so Vdd and GND are staggered, and the upper and lower cells can share Vdd and GND.

Alternate mirroring is both applied to tgates and inverters.



5. Magic using cell hierarchy



6. Irsim (test vectors: own and barrel.cmd)

- barrel.cmd

```

|
| barrel.cmd.txt
|
| Comment Lines start with |
|
| Elec 422/527 HW1 Problem 4
| CMOS 4x4 Transmission Gate Barrel Shifter with Static Latch Array
| Spring 2023

```

|
| Please submit the output generated by irsim for this command file
| input data literals are 16, 15, 14, 13, 12, 11, 10
| 16 is MSB, 10 is LSB in terms of input data bits
| barrel shifter control is shift3, shift2, shift1, shift0
| outputs of barrel shifter before latches are sr3, sr2, sr1, sr0
| latch control (or enable) signal for all 4 latches is store
| final outputs of latch are result3, result2, result1, result0
| clock definition of vdd as constant 1 allows irsim to read
| the v input commands without a real clock signal in this problem
| Please MARK UP the irsim output with color highlights to
| to explain in words what is happening with each shift and store
| sequence in terms of data values (literals 0 through 6) captured.
| Note that not all shifted sequences are actually stored.
| Also explain what happens when all shift lines are low 0 and
| we try to latch a value, or when multiple shift lines are high 1.
|

logfile barrel.log

ana 16 15 14 13 12 11 10 shift3 shift2 shift1 shift0 sr3 sr2 sr1 sr0
ana store result3 result2 result1 result0

| First data set

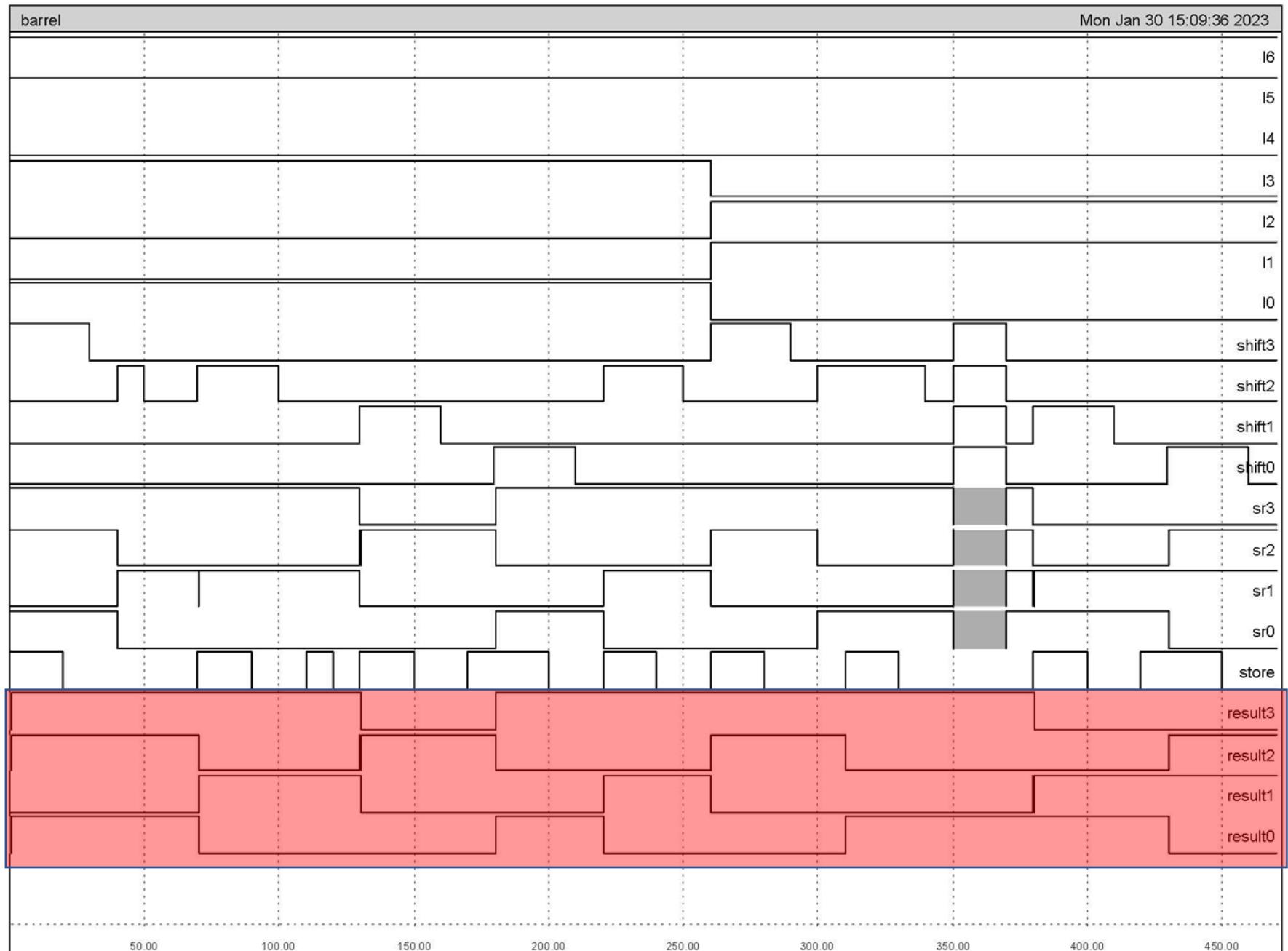
v 16 1
v 15 1
v 14 0
v 13 1
v 12 0
v 11 0
v 10 1
v shift3 1 1 1 0
v shift2 0 0 0 0 1 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0
v shift1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0
v shift0 1 1 1 0 0 0 0
v store 1 1 0 0 0 0 0 1 1 0 0 1 0 1 1 0 0 1 1 1 0 0 1 1 0 0
clock vdd 1

R

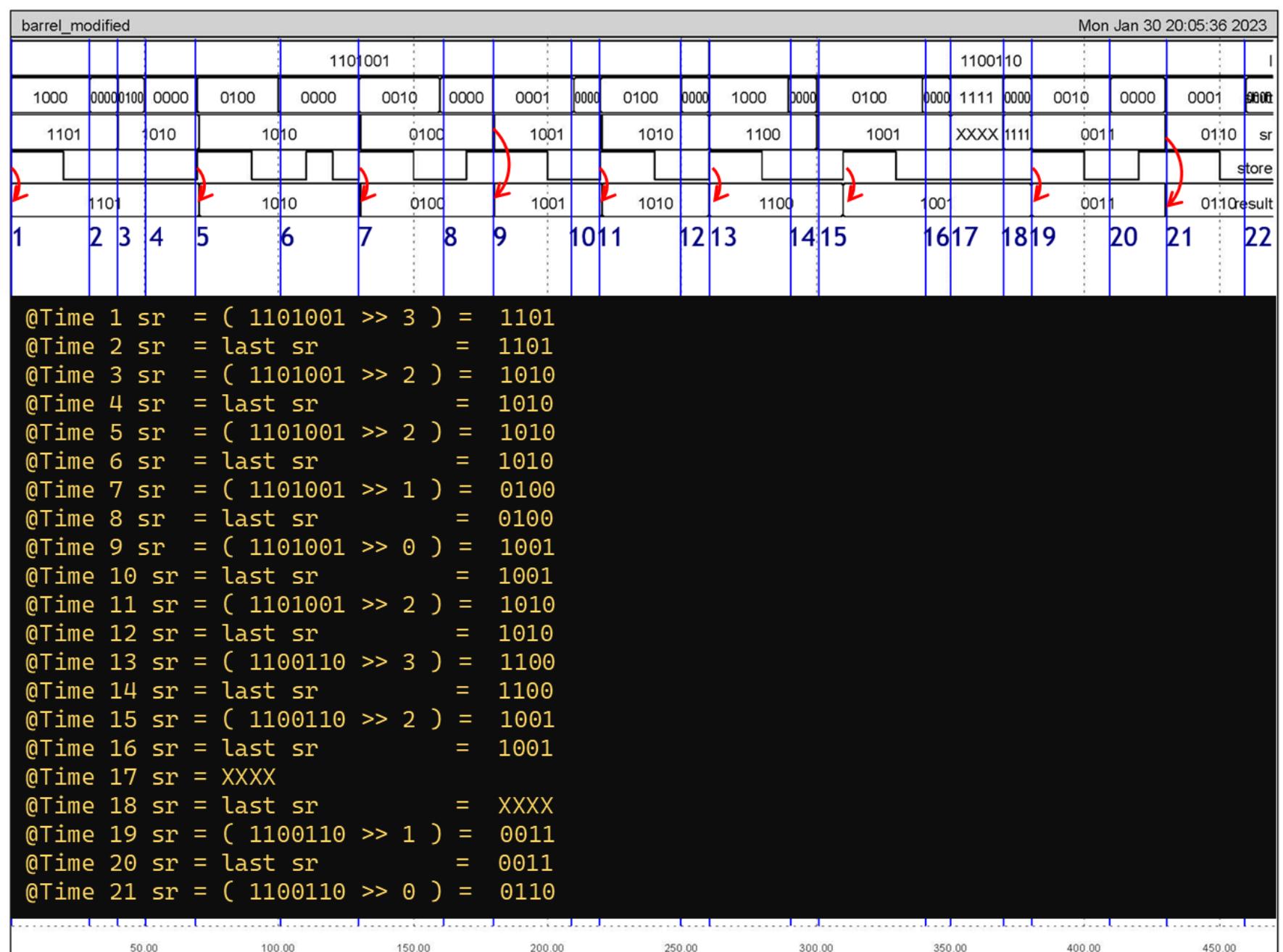
| Second data set with intentional error case to observe

v 16 1
v 15 1
v 14 0
v 13 0
v 12 1
v 11 1
v 10 0
v shift3 1 1 1 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
v shift2 0 0 0 0 1 1 1 1 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
v shift1 0 0 0 0 0 0 0 0 0 1 1 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
v shift0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 1 1 1 0
v store 1 1 0 0 0 1 1 0 0 0 0 0 1 1 0 0 1 1 1 0 0
clock vdd 1

R



It can latch 0 or 1 as shown in red block above.



When the store is high, the value of result is the value of sr (transparent mode)

When store is low, the value of result remains unchanged (opaque mode)

When all shift lines are low 0, sr remains unchanged. At this time, all tgates outputs are in a high-impedance state, and due to the existence of distributed capacitance, tgates maintains the original value.(Like Time 2-3, 4-5 ...)

When multiple shift lines are high 1, sr is X, this may be caused by conflicting logical values.(Like Time 17-18)

- barrel_own.cmd

```
|  
| barrel_own.cmd.txt  
|  
| Comment lines start with |  
|  
| Elec 422/527 HW1 Problem 4  
| CMOS 4x4 Transmission Gate Barrel Shifter with Static Latch Array  
| Spring 2023  
|  
| Please submit the output generated by irsim for this command file  
| input data literals are 16, 15, 14, 13, 12, 11, 10  
| 16 is MSB, 10 is LSB in terms of input data bits  
| barrel shifter control is shift3, shift2, shift1, shift0  
| outputs of barrel shifter before latches are sr3, sr2, sr1, sr0  
| latch control (or enable) signal for all 4 latches is store  
| final outputs of latch are result3, result2, result1, result0  
| clock definition of vdd as constant 1 allows irsim to read  
| the v input commands without a real clock signal in this problem  
| Please MARK UP the irsim output with color highlights to  
| to explain in words what is happening with each shift and store  
| sequence in terms of data values (literals 0 through 6) captured.  
| Note that not all shifted sequences are actually stored.  
| Also explain what happens when all shift lines are low 0 and  
| we try to latch a value, or when multiple shift lines are high 1.  
|  
logfile barrel.log  
vector l      16 15 14 13 12 11 10  
vector shift   shift3 shift2 shift1 shift0  
vector sr      sr3 sr2 sr1 sr0  
vector result  result3 result2 result1 result0  
ana l shift sr store result  
| First data set  
v 16      0  
v 15      0  
v 14      1  
v 13      0  
v 12      0  
v 11      1  
v 10      0  
v shift3  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0  
v shift2  1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0  
v shift1  0 0 0 0 1 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0
```

```

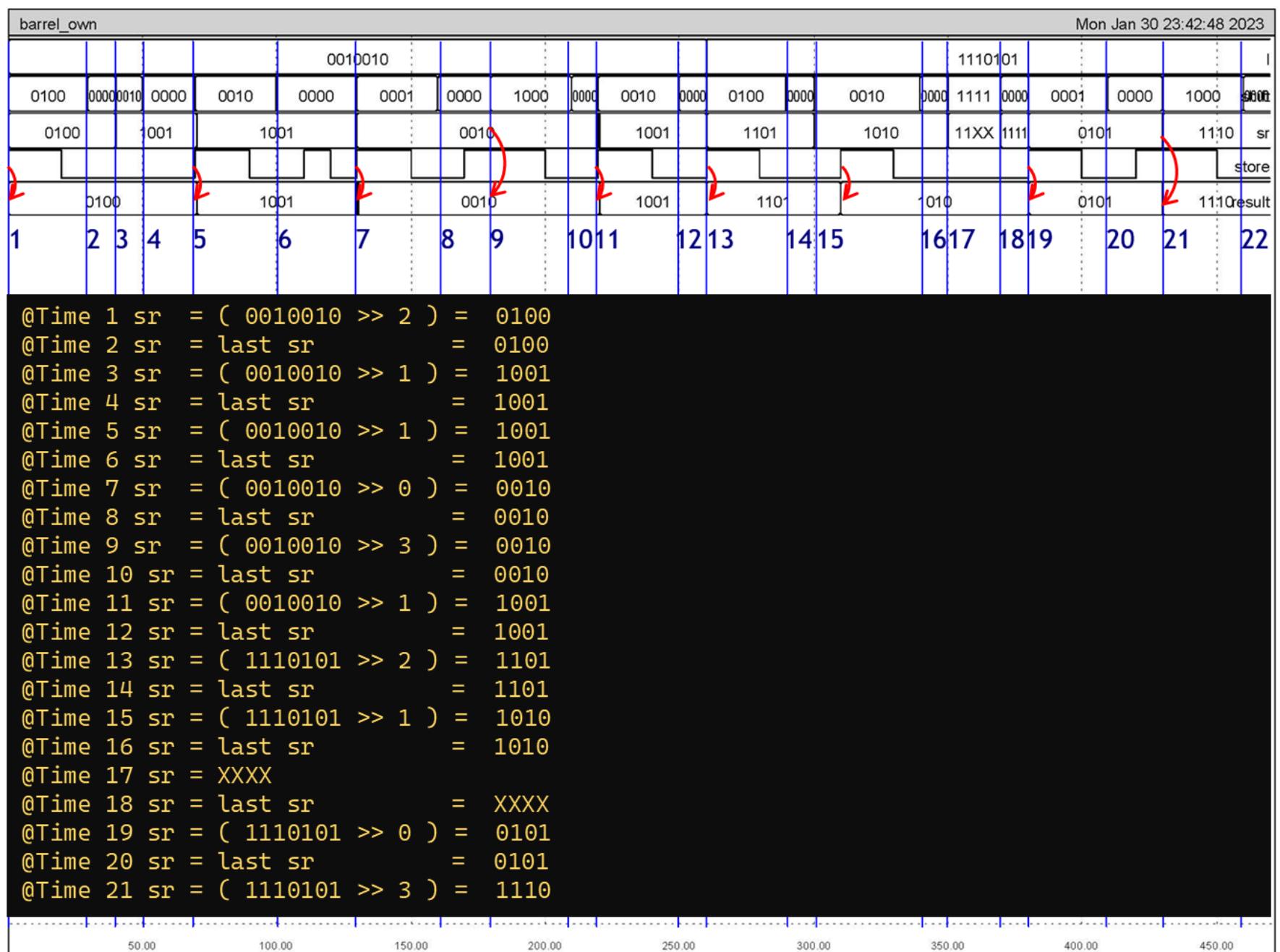
v shift0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0
v store 1 1 0 0 0 0 0 1 1 0 0 1 0 1 1 0 0 1 1 1 0 0 1 1 0 0
clock vdd 1
R

| Second data set with intentional error case to observe

v 16      1
v 15      1
v 14      0
v 13      0
v 12      1
v 11      1
v 10      0
v shift3 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 1 1 1 0
v shift2 1 1 1 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0
v shift1 0 0 0 0 1 1 1 1 0 1 1 0 0 0 0 0 0 0 0 0 0
v shift0 0 0 0 0 0 0 0 0 0 1 1 0 1 1 1 0 0 0 0 0 0
v store 1 1 0 0 0 1 1 0 0 0 0 0 1 1 0 0 1 1 1 0 0
clock vdd 1

```

R



7. Substrate contacts also near barrel tgates

