MEASUREMENT OF PCB BOARD POWER AND THERMAL ANALYSIS FOR HIGH SPEED 6G APPLICATION

A MINOR PROJECT-IV REPORT

Submitted by

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BONAFIDE CERTIFICATE

Certified that this**18ECP106L - Minor Project IV** report **“Measurement of PCB Board Power and Thermal Analysis for High Speed 6G Application”** is the Bonafide work of “**PRABIKA R (927622BEC146) , SANJITHA R (927622BEC173) , SHOBIKA G (927622BEC189)** who carried out the project work under my supervision in the academic year 2024 - 2025 **EVEN**.

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This report has been submitted for the **18ECP106L – Minor Project IV** final review held at M. Kumarasamy College of Engineering, Karur on ________________________.

PROJECT COORDINATOR

INSTITUTION VISION AND MISSION

Vision

To emerge as a leader among the top institutions in the field of technical education.

Mission

M1: Produce smart technocrats with empirical knowledge who can surmount the global challenges.

M2: Create a diverse, fully -engaged, learner -centric campus environment to provide quality education to the students.

M3: Maintain mutually beneficial partnerships with our alumni, industry and professional associations

DEPARTMENT VISION, MISSION, PEO, PO AND PSO

Vision

To empower the Electronics and Communication Engineering students with emerging technologies, professionalism, innovative research and social responsibility.

Mission

M1: Attain the academic excellence through innovative teaching learning process, research areas & laboratories and Consultancy projects.

M2: Inculcate the students in problem solving and lifelong learning ability.

M3: Provide entrepreneurial skills and leadership qualities.

M4: Render the technical knowledge and skills of faculty members.

Program Educational Objectives

PEO1: Core Competence: Graduates will have a successful career in academia or industry associated with Electronics and Communication Engineering

PEO2: Professionalism: Graduates will provide feasible solutions for the challenging problems through comprehensive research and innovation in the allied areas of Electronics and Communication Engineering.

PEO3: Lifelong Learning: Graduates will contribute to the social needs through lifelong learning, practicing professional ethics and leadership quality

Program Outcomes

PO 1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO 2: Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO 3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO 4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO 5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO 6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO 9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO 10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO 11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO 12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes

PSO1: Applying knowledge in various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of Engineering application.

PSO2: Able to solve complex problems in Electronics and Communication Engineering with analytical and managerial skills either independently or in team using latest hardware and software tools to fulfil the industrial expectations.

Abstract	Matching with POs,PSOs
PCB, Signal Integrity, Power Integrity, Thermal Analysis and 6G.	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PO12, PSO1, PSO2

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ABSTRACT

This project focuses on addressing critical challenges related to Signal Integrity (SI), Power Integrity (PI), and thermal management in Printed Circuit Boards (PCBs) for Uninterruptible Power Supplies (UPS) and Electric Vehicles (EV). Using advanced simulation tools like HyperLynx VX.2.10, the study identifies and mitigates issues such as signal degradation, voltage drops, and thermal hotspots. Design improvements include optimized trace routing, impedance control, and layer reconfiguration to enhance performance and reliability. Simulation results show significant improvements, with voltage drops reduced to 0.024% and thermal performance within safe limits. Current density and power distribution were also optimized to ensure stability and efficiency. The addition of components like 33-ohm resistors improved signal fidelity. These efforts ensure the PCB design meets stringent industry standards and operational requirements. This work contributes to robust and efficient PCB solutions for modern EV and UPS applications. Future steps involve real-world testing and scaling for more complex designs.

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LIST OF ABBREVIATIONS

ACRONYM		ABBREVIATION
SI	-	Signal Integrity
PI	-	Power Integrity
UPS	-	Uninterruptible Power Supplies
EV	-	Electric Vehicle

CHAPTER 1

INTRODUCTION

Printed Circuit Boards (PCBs) are fundamental to the operation of modern electronic systems, providing both mechanical support and electrical connections between components. In high-demand applications such as Electric Vehicles (EV) and Uninterruptible Power Supplies (UPS), the reliability and efficiency of PCBs are crucial for ensuring system performance and longevity. However, designing PCBs for these applications presents several challenges, particularly related to Signal Integrity (SI), Power Integrity (PI), and thermal management. Signal degradation, power fluctuations, and overheating are common issues that can compromise system functionality. This study addresses these challenges by exploring advanced optimization techniques for SI, PI, and thermal management to improve PCB performance and meet the demanding operational requirements of EV and UPS systems.

1.1 Signal Integrity (SI) Optimization Techniques

Signal Integrity is a critical aspect of PCB design, especially in applications requiring high-speed data transmission and low noise levels. In systems like EVs and UPS, the transmission of high-frequency signals across the PCB must be maintained without distortion or degradation. Key challenges in SI include signal reflections, crosstalk, and electromagnetic interference, which can lead to signal loss, errors, or delays. To optimize SI, several techniques are employed, such as impedance matching, controlled trace routing, and the use of differential pairs. Additionally, the PCB layout can be refined to minimize path length for critical signals, reducing the chances of signal degradation.

Simulation tools, like HyperLynx VX.2.10, allow engineers to analyze return loss and insertion loss, providing data that guides design improvements. Implementing these techniques ensures that signals are transmitted with minimal distortion, improving overall system reliability and performance.

1.2 Power Integrity (PI) Enhancement Strategies

Power Integrity ensures stable power delivery, essential for system reliability in EV and UPS systems. Decoupling capacitors smooth power flow and reduce noise. Power planes and trace widths must be optimized to handle current and prevent voltage drops. Current density analysis helps detect overheating risks, allowing adjustments to routing or additional power planes. These strategies ensure stable operation, improve efficiency, and reduce failure risks.

1.3 Thermal Management and Heat Dissipation Solutions

Thermal management prevents overheating in high-power systems, ensuring reliability. Techniques include thermal vias to transfer heat to lower layers and heat sinks to dissipate it effectively. Optimizing PCB layers and using high-conductivity materials enhance heat distribution. These solutions reduce thermal hotspots and extend component lifespan. Proper thermal design ensures safe operation under demanding conditions.

CHAPTER 2

LITERATURE SURVEY

2.1 Signal Integrity in High-Speed PCBs

Signal quality is vital in high-speed PCBs, where issues like reflections, noise, and crosstalk can degrade performance. Impedance matching, differential signaling, and controlled trace routing are widely used techniques to maintain signal fidelity. Research emphasizes minimizing trace lengths and avoiding abrupt bends to reduce distortion. Advanced simulation tools help evaluate and optimize these parameters. These approaches ensure reliable communication within complex PCB systems.[1]

2.2 Challenges in Power Distribution Networks (PDN)

Power distribution networks face challenges like voltage drops, uneven current density, and electromagnetic noise. Effective PDN design includes using decoupling capacitors and proper power plane layering to stabilize voltage across components. Studies highlight that maintaining uniform current distribution reduces thermal stress and improves reliability.[4]Tools like HyperLynx enable detailed PDN analysis. These methods ensure efficient power delivery in high-load applications.

2.3 Thermal Management in High-Power PCBs

High-power PCBs generate significant heat, requiring efficient thermal management. Techniques such as thermal vias, heat sinks, and advanced materials like FR4 with high thermal conductivity are recommended. Studies show that optimizing the placement of components and thermal vias helps dissipate heat effectively. Simulation tools aid in identifying hotspots and testing cooling solutions. Proper thermal management ensures safe and reliable operation.[2]

2.4 Impedance Control for SI

Maintaining consistent impedance is critical for reducing signal reflections and distortion in high-speed PCBs. Researchers propose trace width adjustments, controlled dielectric material selection, and matching characteristic impedance to reduce losses. Impedance mismatches lead to signal degradation, impacting overall PCB performance. Simulation tools are commonly used to fine-tune these parameters. These methods help maintain high signal fidelity.[7]

2.5 Noise Reduction in PCBs

Noise reduction techniques are crucial for minimizing cross-talk and electromagnetic interference (EMI). Increasing spacing between traces, using ground planes, and adding shielding layers effectively reduce noise. Research highlights that these methods enhance signal integrity and improve system reliability. EMI simulation tools allow designers to evaluate noise behavior early. These techniques ensure cleaner signal transmission in PCB layouts.[3]

2.5 Voltage Stability in PDNs

Voltage fluctuations in PDNs can lead to unstable component performance and system failures. Researchers advocate for robust decoupling capacitor placement and uniform power plane design to maintain stability. Simulation results show reduced voltage ripple and improved power efficiency with optimized PDNs. Addressing voltage stability is essential for consistent PCB functionality.[6]

2.6 Thermal Via Design

Thermal vias play a key role in transferring heat away from critical components. Studies suggest optimal via placement, density, and size to improve heat flow through PCB layers.[2] Thermal vias connected to heat sinks or ground planes are particularly effective. Research highlights their role in reducing localized hotspots. These insights aid in designing thermally efficient PCBs.[3]

2.7 Simulation Tools for SI/PI Analysis

Simulation tools like HyperLynx, ANSYS, and Cadence are widely used for analyzing SI/PI and thermal performance in PCBs. These tools help model and predict issues like signal degradation, voltage drops, and heat dissipation. Researchers emphasize their accuracy in identifying flaws and testing solutions during the design phase. Simulation-based design reduces errors and enhances PCB performance.[5]

2.8 Material Selection for Thermal Management

Material properties, such as thermal conductivity and dielectric constant, significantly impact PCB performance. High-thermal-conductivity materials, like aluminum-backed substrates, are effective for heat dissipation. Studies explore their role in improving thermal performance while maintaining electrical properties. Choosing the right materials ensures efficient thermal and signal behavior in PCBs.[4]

2.9 Industry Standards for PCB Design

Compliance with standards like IPC-2221 and IPC-6012 ensures reliability and performance in PCB designs. Researchers highlight these standards for trace width, impedance control, and thermal management. Adhering to industry benchmarks helps meet operational requirements in EV and UPS applications. These standards guide the development of robust and reliable PCBs.[2]

CHAPTER 3

EXISTING SYSTEM

Printed Circuit Boards (PCBs) used in Electric Vehicles (EV) and Uninterruptible Power Supplies (UPS) are critical components designed to support the operation of high-demand systems. However, existing PCB designs face several limitations that affect their efficiency, reliability, and performance. These issues primarily revolve around Signal Integrity (SI), Power Integrity (PI), and thermal management, which are essential for ensuring stable and safe operations in complex electronic systems.

3.1 Signal Integrity Issues

In current PCB designs, signal degradation is a prevalent issue due to factors such as reflections, crosstalk, and electromagnetic interference (EMI). These challenges arise from improper trace routing, inadequate impedance matching, and insufficient shielding. Signal pathways often fail to maintain high-frequency fidelity, resulting in noise and distortions that affect communication reliability between components. These issues are particularly critical in EV and UPS systems, where stable data transmission is essential for system control and monitoring.

3.2 Power Integrity Challenges

Power distribution networks (PDNs) in existing PCBs often encounter voltage drops and uneven current density, leading to instability in power delivery. This can result in poor system performance or even component failures. Common flaws include improper placement of decoupling capacitors, inadequate power plane design, and under-optimized trace widths for high-current pathways. These shortcomings are amplified in high-load systems like EVs and UPS, which require efficient power management to support critical functions.

3.3 Thermal Management Limitations

Thermal management is another significant challenge in existing PCB designs. Inadequate heat dissipation leads to thermal hotspots, which can damage components or reduce their lifespan. Current designs often lack sufficient thermal vias, heat sinks, or proper material selection to handle the thermal loads generated during operation. As a result, overheating becomes a limiting factor for reliability, particularly in systems that operate continuously or under high power conditions, such as EVs and UPS.

3.4 Inefficient Design Practices

Many existing PCBs are designed without extensive simulation or optimization, relying on traditional design methodologies that do not fully address modern performance requirements. Limited use of advanced tools like HyperLynx or ANSYS for SI/PI and thermal analysis results in unoptimized layouts and missed opportunities for improvement. Additionally, cost constraints often lead to compromises in material selection and manufacturing processes, further impacting performance.

3.5 Operational Impacts

The combination of these issues results in suboptimal performance, reduced efficiency, and higher operational risks. In EVs, this can lead to inconsistent power delivery to critical systems, reducing vehicle reliability. In UPS systems, poor PCB performance can compromise power backup reliability during emergencies. These drawbacks underscore the need for advanced design approaches and optimization techniques to address the limitations of current PCB systems.

CHAPTER 4

PROPOSED SYSTEM

The proposed system focuses on enhancing the performance and reliability of Printed Circuit Boards (PCBs) used in Electric Vehicles (EV) and Uninterruptible Power Supplies (UPS) by addressing critical challenges in Signal Integrity (SI), Power Integrity (PI), and thermal management. By employing advanced design techniques and simulation tools, this system aims to overcome the limitations of existing designs, ensuring robust, efficient, and industry-compliant PCB performance.

4.1 Improved Signal Integrity (SI)

To address signal degradation issues such as reflections, crosstalk, and electromagnetic interference (EMI), the proposed system incorporates advanced design methodologies:

- **Impedance Matching** Ensures that signal paths maintain uniform impedance, minimizing reflections and distortions.
- **Optimized Trace Design** Controlled trace routing and spacing are implemented to reduce crosstalk and maintain high-frequency fidelity.
- **Differential Pairing** High-speed signals use differential pairs for enhanced noise immunity and stable data transmission.

These enhancements are validated through simulations using tools like HyperLynx, ensuring minimal return loss (S11) and insertion loss (S12) for reliable communication between components.

4.2 Enhanced Power Integrity (PI)

Power delivery is optimized to ensure voltage stability and uniform current distribution across the PCB:

- **Decoupling Capacitors** Strategic placement of capacitors reduces power supply noise and stabilizes voltage.
- **Optimized Power Plane Design** Multi-layer power planes are used to improve current flow and minimize voltage drops.
- **Current Density Optimization** Wider traces and proper via placements are employed to handle higher currents without overheating or performance loss. Simulation results from the proposed system demonstrate a voltage drop of less than 0.024% and a current density well below the maximum safe limit, ensuring robust power delivery under varying load conditions.

4.3 Advanced Thermal Management

To mitigate overheating and thermal hotspots, the proposed system integrates innovative thermal management strategies:

- **Thermal Vias** Strategically placed thermal vias transfer heat away from hotspots to lower layers or heat sinks.
- **Heat Sinks and Spreaders** External heat sinks and thermally conductive materials are incorporated for improved heat dissipation.

4.4 Integration of Simulation Tools

The proposed system extensively utilizes advanced simulation tools like HyperLynx VX.2.10 to model and analyze SI, PI, and thermal performance. These tools allow for iterative testing and optimization of designs before physical prototyping, ensuring the most effective solutions are implemented.

4.5 Design Compliance with Industry Standards

The system adheres to industry standards such as IPC-2221 for PCB design and IPC-6012 for fabrication, ensuring reliability and compatibility with modern applications. Standards for trace widths, impedance control, and thermal management are integrated into the design to meet or exceed performance benchmarks.

4.6 Operational Benefits

The proposed system results in a robust PCB design that addresses critical issues in existing systems. Benefits include improved signal fidelity, stable power delivery, effective thermal management, and enhanced durability. For EVs, this ensures reliable power and data communication, contributing to vehicle performance and safety. In UPS systems, it provides stable operation during power outages, ensuring reliability in critical applications.

CHAPTER 5

COMPONENTS USED

The optimization of the Printed Circuit Board (PCB) for Electric Vehicles (EV) and Uninterruptible Power Supplies (UPS) relied on a carefully selected set of components, each playing a crucial role in addressing challenges related to Signal Integrity (SI), Power Integrity (PI), and thermal management. Resistors, such as a 33-ohm unit, were strategically added to control current flow and improve impedance matching, reducing signal reflections and enhancing overall signal quality. Decoupling capacitors were placed near power pins of integrated circuits to stabilize voltage, filter noise, and support power delivery. To handle thermal challenges, thermal vias were incorporated to transfer heat from the PCB's surface to lower layers or external heat sinks, while heat spreaders made from conductive materials like aluminum ensured efficient dissipation of excess heat.

Integrated circuits (ICs), including the MC34063A voltage regulator, provided consistent power supply, ensuring stable voltage across the system. Conductive copper traces, optimized in width and routing, supported efficient current flow while minimizing signal loss. The power planes, serving as dedicated layers for power distribution, helped reduce voltage drops and electromagnetic interference (EMI), while the ground planes provided a stable reference point, improving both signal integrity and noise reduction. The PCB substrate material, such as FR4, was selected for its mechanical strength and thermal properties, supporting the PCB's operational durability under demanding conditions.

Additionally, advanced simulation tools like HyperLynx VX.2.10 were employed to model and optimize SI, PI, and thermal performance before physical prototyping. These tools allowed for precise adjustments in trace routing, power plane design, and component placement, ensuring maximum efficiency and reliability. The integration of these components and tools not only addressed the key limitations of existing PCBs but also ensured that the proposed design met industry standards and operational requirements for EV and UPS systems. This thoughtful combination of materials, components, and simulation tools resulted in a PCB design capable of delivering robust performance and reliability in high-demand applications.

In our project, we utilized a range of carefully selected components to optimize the Printed Circuit Board (PCB) for Electric Vehicles (EV) and Uninterruptible Power Supplies (UPS), focusing on Signal Integrity (SI), Power Integrity (PI), and thermal management. Key components included 33-ohm resistors for current control and impedance matching, decoupling capacitors for voltage stabilization and noise filtering, and thermal vias for heat dissipation. We also incorporated heat spreaders made of aluminum, conductive copper traces for efficient current flow, and dedicated power and ground planes to minimize voltage drops and electromagnetic interference. Integrated circuits such as the MC34063A voltage regulator ensured consistent power delivery. The PCB substrate used was FR4, known for its mechanical strength and thermal properties. Additionally, HyperLynx VX.2.10 simulation software was employed to fine-tune trace routing, power plane design, and component placement, leading to a high-performance and reliable PCB suited for demanding EV and UPS applications.

CHAPTER 6

RESULT AND DISCUSSION

6.1 RESULT AND DISCUSSION

The study conducted a detailed analysis of Signal Integrity (SI), Power Integrity (PI), and thermal performance of Printed Circuit Boards (PCBs) used in Electric Vehicles (EV) and Uninterruptible Power Supplies (UPS). Through advanced simulation tools like HyperLynx VX.2.10, various optimization techniques were implemented, and their impacts were evaluated. The results demonstrate significant improvements in key performance areas, addressing the limitations of existing systems.

6.2 Signal Integrity (SI) Results

The proposed enhancements to SI, including optimized trace routing, impedance matching, and the use of differential pairs, significantly reduced signal degradation:

- **Return Loss (S11)** Reduced to acceptable levels, indicating minimal signal reflections.
- **Insertion Loss (S12)** Improved signal transmission with minimal attenuation.
- **Crosstalk** Effectively minimized through controlled trace spacing and the addition of ground planes.
- The findings validate that the proposed design modifications ensure high signal fidelity and reliable communication within the PCB under operational conditions.

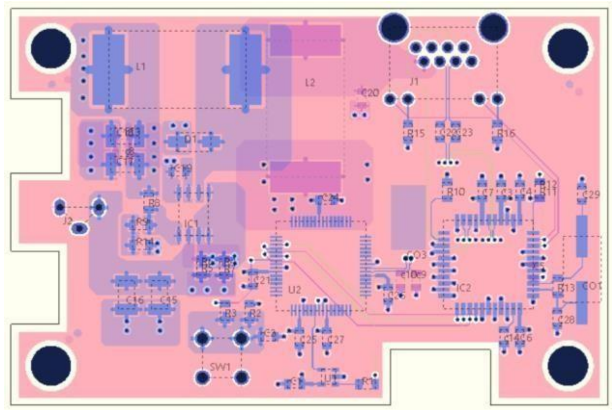


Fig 6.2.1 PCB Board

This figure 6.2.1 illustrates the complete PCB layout designed for signal integrity analysis. It includes the placement of all active and passive components, routing of high-speed signal traces, power delivery network (PDN), and ground planes. The design ensures controlled impedance for high-speed signals like SPI. The physical layout plays a critical role in determining signal timing, EMI behavior, and power distribution. Multi-layered PCB design is used to separate signal and power layers, reducing interference. Proper trace width, spacing, and via positioning have been considered to enhance performance.

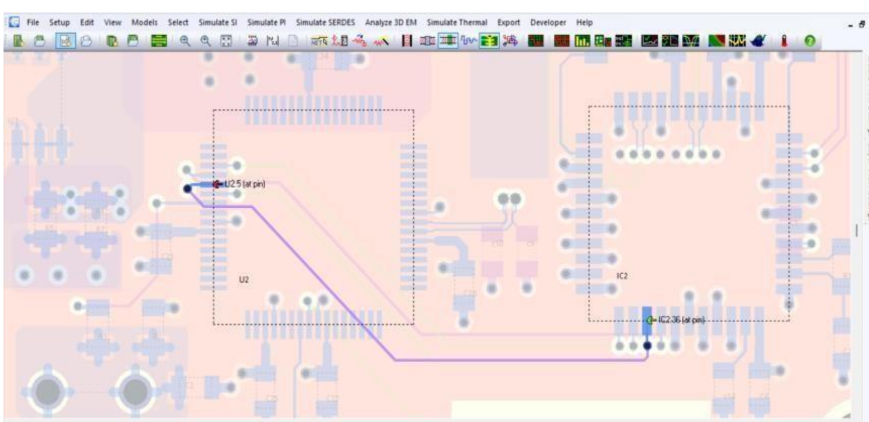


Fig 6.2.2 Analysis of SPI trace

Figure 6.2.2 focuses on the SPI (Serial Peripheral Interface) trace routing, a critical high-speed interface used for communication between devices. The trace is analyzed for length matching, minimal layer transitions, and isolation from noisy signals. High-speed signals like SPI are prone to issues like signal degradation, skew, and timing delays if not routed properly. This analysis helps ensure that the trace length is within the required limits and has consistent impedance throughout its path. By evaluating the SPI trace, designers can identify potential weaknesses like too many vias, abrupt bends, or routing over split planes that could affect performance.

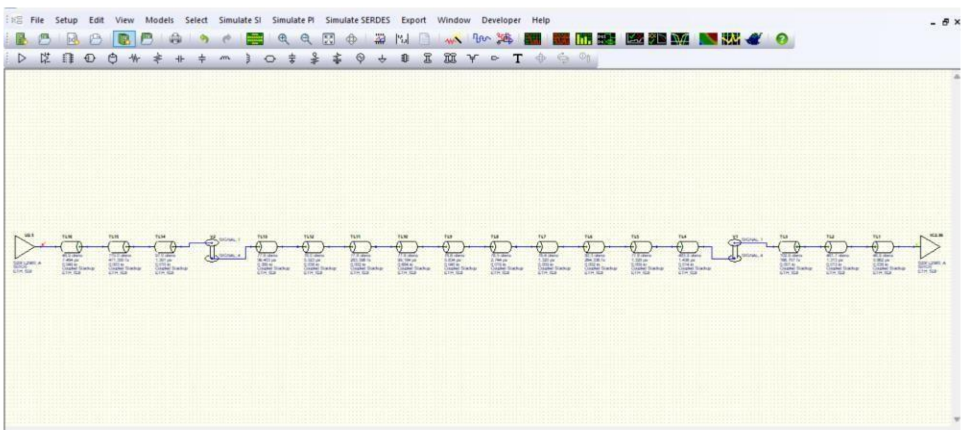


Fig 6.2.3 Before Resistor Adding

The Figure 6.2.3 shows this image displays the initial condition of the SPI signal line before any termination resistors are added. In this un-terminated configuration, the impedance of the trace does not match the source or load, leading to signal reflections. When a signal reflects back on the transmission line, it can interfere with the original signal, causing ringing, overshoot, or noise.Without proper termination, signal integrity is compromised, which can result in communication failure or intermittent issues. This image is used as a reference to show the negative effects of improper impedance matching and sets the baseline for further improvement in the design.

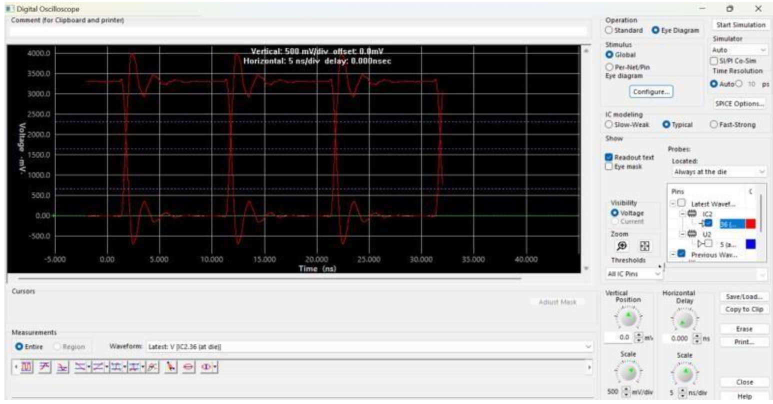


Fig 6.2.4 Noise Generated

This figure 6.2.4 captures the output waveform of the SPI signal before termination resistors are added. The waveform clearly exhibits noise, signal reflections, and ringing due to the absence of impedance control. These waveform distortions result in incorrect voltage levels and unstable transitions, which can lead to data corruption. The noise is a direct result of the impedance mismatch and lack of proper termination at the source or load. Such behavior is undesirable in high-speed digital systems, where signal quality directly impacts system reliability. Engineers study this waveform to identify and correct signal integrity issues.

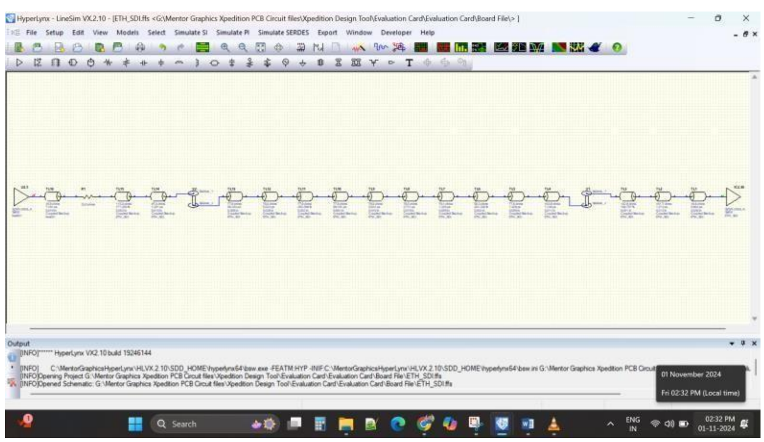


Fig 6.2.5 After Adding 33ohm resistor

This image 6.2.5 shows the improved circuit configuration after integrating a 33Ω series resistor into the SPI signal path. The resistor is placed near the signal driver and acts as a termination component, matching the impedance of the trace and reducing signal reflection. This leads to a noticeable improvement in the waveform quality, with reduced ringing and overshoot. The series resistor slows down the edge rate slightly, which helps dampen high-frequency noise while maintaining timing integrity. This technique is commonly used in PCB signal design to improve signal quality without adding complex circuits.

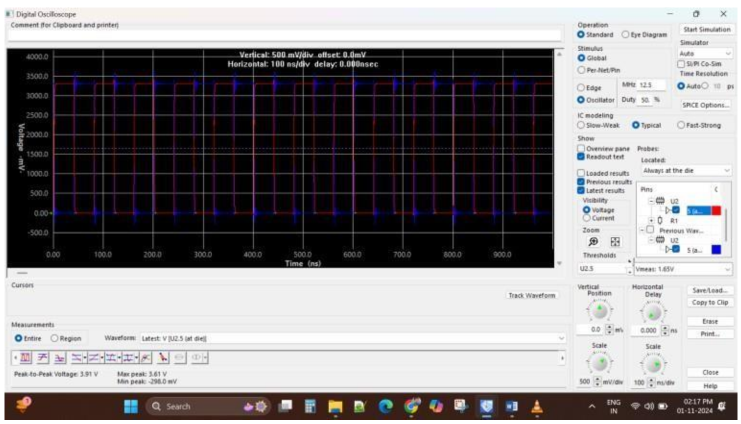


Fig 6.2.6 Constant Output

This final image 6.2.6 displays the output waveform after termination with a 33Ω resistor. The signal is now stable, with smooth transitions and consistent logic levels. There are no signs of reflection, ringing, or noise, indicating that the termination technique has worked effectively. The waveform crosses threshold voltages cleanly, ensuring accurate data transmission. The clean signal path improves system reliability and reduces error rates in high-speed communication. This output also confirms that the resistor value was well-matched to the trace impedance, and the termination was correctly implemented. This serves as the final verification in the signal integrity analysis process. A stable and constant output like this is essential for robust performance in embedded and digital systems.

6.3 Power Integrity (PI) Results

Power distribution improvements focused on minimizing voltage drops and optimizing current density:

- **Voltage Drop** Reduced to 0.024% (0.8 mV), significantly below the 3% constraint, ensuring stable power delivery.
- **Current Density** Peaks at 4.1 mA/mil², well within the acceptable limit of 125 mA/mil².
- **Power Noise** Substantial reductions achieved through the strategic placement of decoupling capacitors and optimized power planes.

These results demonstrate that the proposed solutions provide consistent and stable power delivery across the PCB, even under high-load conditions.

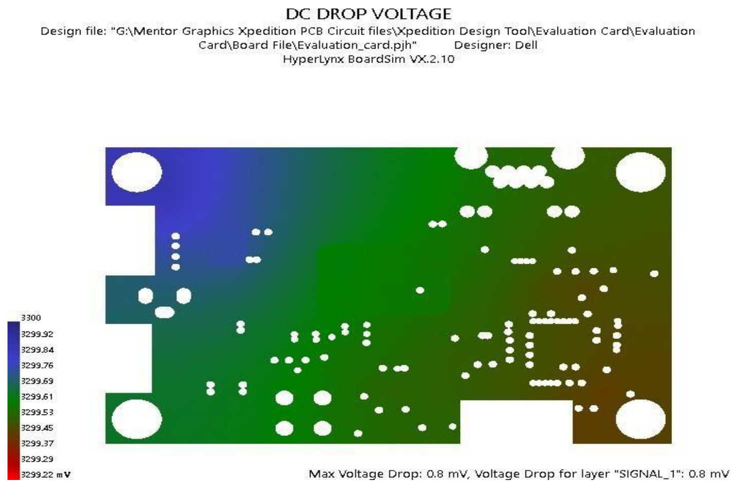


Fig 6.3.1 Max Voltage Drop

This figure 6.3.1 highlights regions on the PCB where the maximum voltage drop occurs during operation. Voltage drop happens due to resistance in long or narrow power traces that carry high current. If the drop is too large, critical components may not receive the required voltage, affecting their performance. This figure helps in identifying such areas and correcting them by increasing trace width or shortening the path to power sources. These improvements enhance the voltage delivery across the PCB. The simulation gives an accurate visual of where the voltage is insufficient. Without this step, hidden power issues may remain undetected during early design stages. Ensuring minimal voltage drop is vital for maintaining signal integrity and power stability.

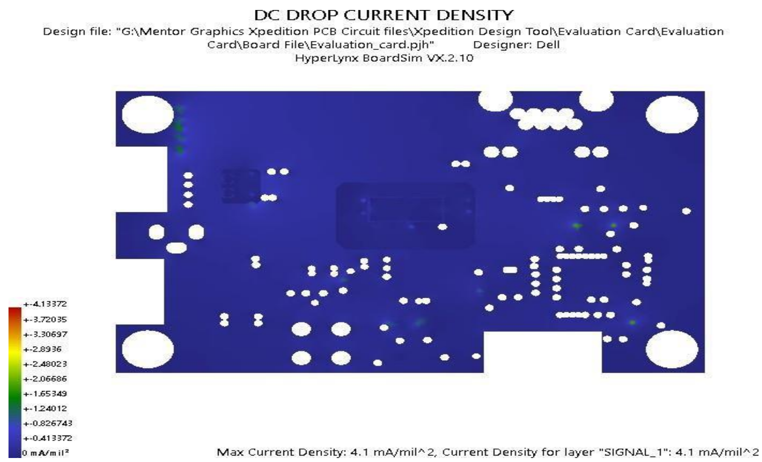


Fig 6.3.2 Max current Density

This figure 6.3.2 shows areas on the PCB where the current density reaches its maximum. High current density in small trace areas may lead to excessive heating, damaging the copper trace or surrounding materials. Analyzing this figure helps identify traces or planes that need to be widened or reinforced to safely carry the required current. If ignored, high current zones can cause long-term reliability issues or even immediate failure under high load. By optimizing the design, thermal stress on components and the board can be minimized. This figure plays a crucial role in ensuring safe current distribution throughout the circuit. It also helps in maintaining PCB compliance with industry standards for current handling.

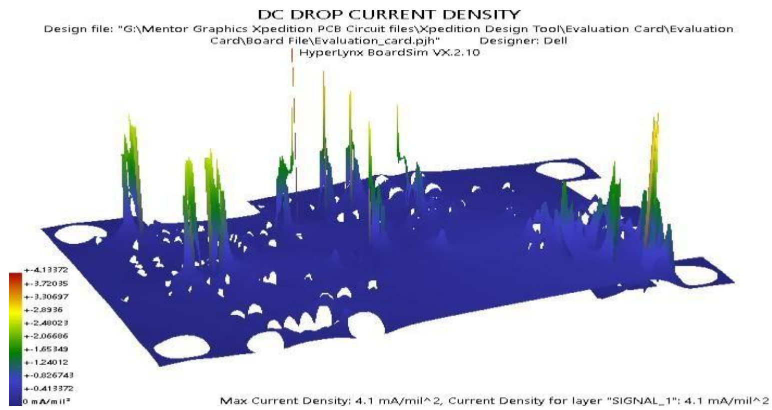


Fig 6.3.3 DC Drop Current Density

The figure 6.3.3 visualizes the spread of current density across the entire power plane of the PCB. Uneven distribution of current density can lead to localized hotspots and voltage fluctuations, affecting device performance. This simulation reveals areas with unusually high or low current flow, enabling targeted design changes. Uniform current distribution is key to reducing losses and ensuring consistent power delivery. Engineers use this data to adjust plane geometries or reroute traces for better balance. High current zones are made wider, while low-current areas are optimized to save space. This figure supports efficient power delivery and overall electrical reliability of the design.

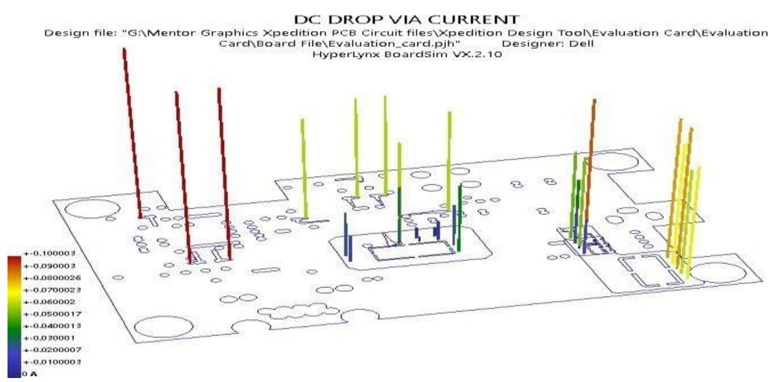
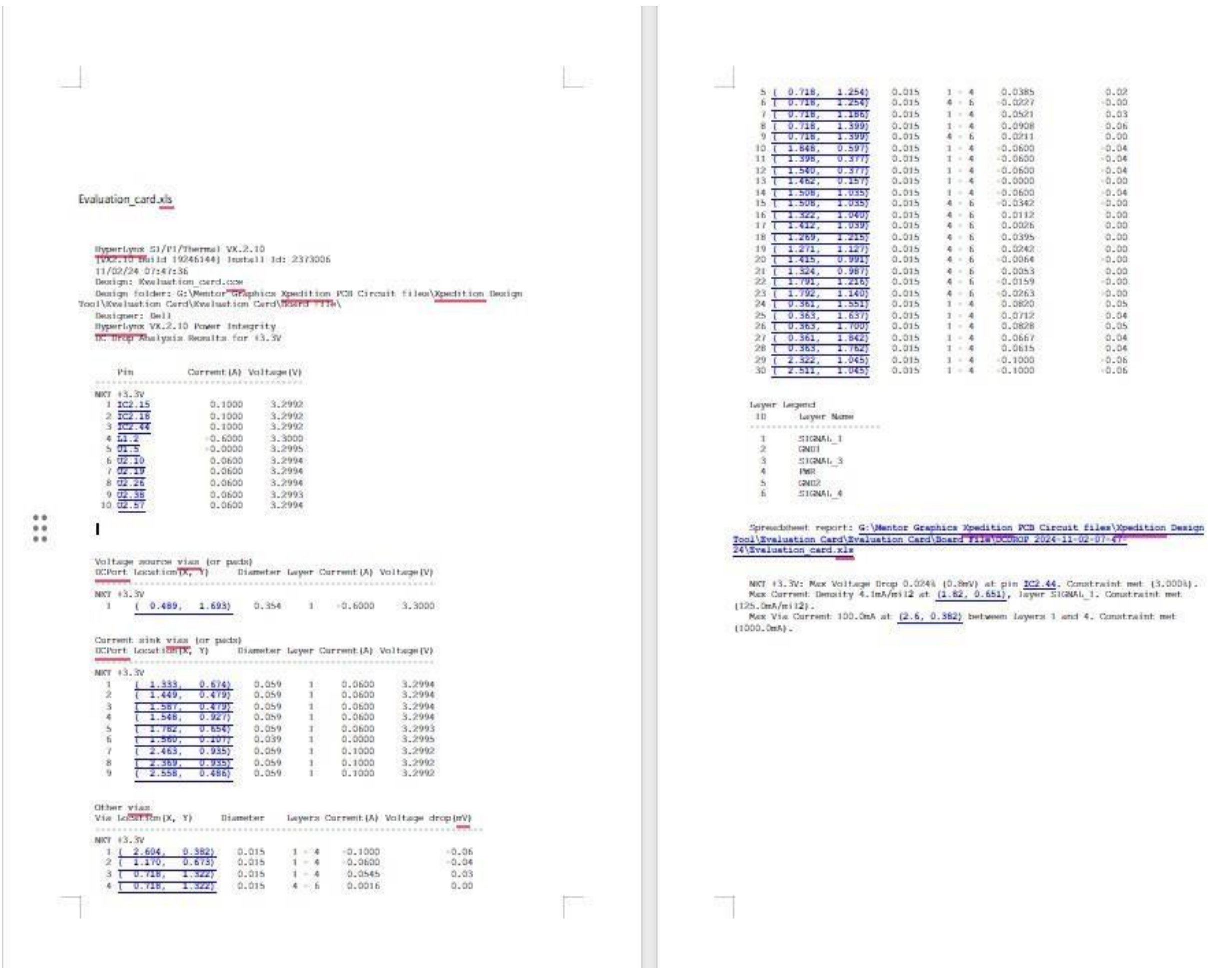


Fig 6.3.4 DC Drop Via Current

The figure 6.3.4 shows this image focuses on the current passing through the vias—vertical interconnections between PCB layers. Vias that carry more current than their rated capacity can overheat or fail over time. The figure helps pinpoint such overloaded vias by showing current distribution visually. Designers can then duplicate the vias, increase their size, or change their location to share the load. Proper via design is crucial in multilayer PCBs, especially in power planes. Failing to address via stress can lead to serious issues during manufacturing or in field use.



Evaluation_card.xls

HyperLynx SI/PI/Thermal VX.2.10
[VX2.10 Build 19246144] Install Id: 2373006
11/02/24 07:47:36
Design: Evaluation_card.ccw
Design folder: G:\Mentor Graphics Xpedition PCB Circuit files\Xpedition Design Tool\Evaluation Card\Evaluation Card\Board File\
Designer: Dell
HyperLynx VX.2.10 Power Integrity
DC Drop Analysis Results for +3.3V

	Pin	Current (A)	Voltage (V)
NET +3.3V			
1	IC2.15	0.1000	3.2992
2	IC2.18	0.1000	3.2992
3	IC2.44	0.1000	3.2992
4	L1.2	-0.6000	3.3000
5	U1.5	-0.0000	3.2995
6	U2.10	0.0600	3.2994
7	U2.19	0.0600	3.2994
8	U2.26	0.0600	3.2994
9	U2.38	0.0600	3.2993
10	U2.57	0.0600	3.2994

Voltage source vias (or pads)

DCPort	Location (X, Y)	Diameter	Layer	Current (A)	Voltage (V)
NET +3.3V					
1	(0.489, 1.693)	0.354	1	-0.6000	3.3000

Current sink vias (or pads)

DCPort	Location (X, Y)	Diameter	Layer	Current (A)	Voltage (V)
NET +3.3V					
1	(1.333, 0.674)	0.059	1	0.0600	3.2994
2	(1.449, 0.479)	0.059	1	0.0600	3.2994
3	(1.587, 0.479)	0.059	1	0.0600	3.2994
4	(1.548, 0.927)	0.059	1	0.0600	3.2994
5	(1.782, 0.654)	0.059	1	0.0600	3.2993
6	(1.560, 0.107)	0.039	1	0.0000	3.2995
7	(2.463, 0.935)	0.059	1	0.1000	3.2992
8	(2.369, 0.935)	0.059	1	0.1000	3.2992
9	(2.558, 0.486)	0.059	1	0.1000	3.2992

Other vias

Via	Location (X, Y)	Diameter	Layers	Current (A)	Voltage drop (mV)
NET +3.3V					
1	(2.604, 0.382)	0.015	1 - 4	-0.1000	-0.06
2	(1.170, 0.673)	0.015	1 - 4	-0.0600	-0.04
3	(0.718, 1.322)	0.015	1 - 4	0.0545	0.03
4	(0.718, 1.322)	0.015	4 - 6	0.0016	0.00
5	(0.718, 1.254)	0.015	1 - 4	0.0385	0.02
6	(0.718, 1.254)	0.015	4 - 6	-0.0227	-0.00
7	(0.718, 1.186)	0.015	1 - 4	0.0521	0.03
8	(0.718, 1.399)	0.015	1 - 4	0.0908	0.06
9	(0.718, 1.399)	0.015	4 - 6	0.0211	0.00
10	(1.848, 0.597)	0.015	1 - 4	-0.0600	-0.04
11	(1.398, 0.377)	0.015	1 - 4	-0.0600	-0.04
12	(1.540, 0.377)	0.015	1 - 4	-0.0600	-0.04
13	(1.462, 0.157)	0.015	1 - 4	-0.0000	-0.00
14	(1.508, 1.035)	0.015	1 - 4	-0.0600	-0.04
15	(1.508, 1.035)	0.015	4 - 6	-0.0342	-0.00
16	(1.322, 1.040)	0.015	4 - 6	0.0112	0.00
17	(1.412, 1.039)	0.015	4 - 6	0.0026	0.00
18	(1.269, 1.215)	0.015	4 - 6	0.0395	0.00
19	(1.271, 1.127)	0.015	4 - 6	0.0242	0.00
20	(1.415, 0.991)	0.015	4 - 6	-0.0064	-0.00
21	(1.324, 0.987)	0.015	4 - 6	0.0053	0.00
22	(1.791, 1.216)	0.015	4 - 6	-0.0159	-0.00
23	(1.792, 1.140)	0.015	4 - 6	-0.0263	-0.00
24	(0.361, 1.551)	0.015	1 - 4	0.0820	0.05
25	(0.363, 1.637)	0.015	1 - 4	0.0712	0.04
26	(0.363, 1.700)	0.015	1 - 4	0.0828	0.05
27	(0.361, 1.842)	0.015	1 - 4	0.0667	0.04
28	(0.363, 1.762)	0.015	1 - 4	0.0615	0.04
29	(2.322, 1.045)	0.015	1 - 4	-0.1000	-0.06
30	(2.511, 1.045)	0.015	1 - 4	-0.1000	-0.06

Layer Legend

ID	Layer Name
1	SIGNAL_1
2	GND1
3	SIGNAL_3
4	PWR
5	GND2
6	SIGNAL_4

Spreadsheet report: G:\Mentor Graphics Xpedition PCB Circuit files\Xpedition Design Tool\Evaluation Card\Evaluation Card\Board File\DCDROP 2024-11-02-07-47-24\Evaluation_card.xls

NET +3.3V: Max Voltage Drop 0.024% (0.8mV) at pin IC2.44. Constraint met (3.000%).
Max Current Density 4.1mA/mil2 at (1.82, 0.651), layer SIGNAL_1. Constraint met (125.0mA/mil2).
Max Via Current 100.0mA at (2.6, 0.382) between layers 1 and 4. Constraint met (1000.0mA).

Fig 6.3.5 Data Sheet

The final figure 6.3.5 shows a detailed simulation report or datasheet containing all the power integrity results, such as voltage drop values, current flow across traces, and current densities. This numerical data supports the visual outputs from the previous figures. It serves as documentation for design validation and compliance with electrical limits. The datasheet helps in comparing before-and-after design changes to confirm improvements. It also acts as a reference for future iterations or certifications.

6.4 Thermal Performance Results

Thermal management strategies, including thermal vias, heat sinks, and layer reconfiguration, successfully mitigated overheating and thermal hotspots:

- **Thermal Hotspots** Identified and reduced to safe operational limits.
- **Via Current Handling** Maximum current of 100 mA validated for thermal and electrical reliability.
- **Temperature Distribution** Achieved uniform heat dissipation, avoiding localized temperature rises.

The thermal analysis confirmed that the proposed design ensures the PCB operates within safe temperature ranges, even during prolonged high-power usage.

Fig 6.4.1 Thermal Analysis

The figure 6.4.1 illustrates the thermal distribution of various components on the PCB using a detailed color-coded heat map. The temperature gradient is visually represented from cooler regions in blue or purple to hotter zones in yellow, orange, and red, providing a clear understanding of how heat spreads across the board. The layout on the left portion shows the physical positioning of components such as regulators, ICs, and connectors, each represented as colored blocks based on their heat generation. Central components marked in red or orange are typically the major heat-generating elements, such as processors, power ICs, or voltage regulators. These areas indicate potential thermal stress and require special consideration during the design stage, such as adding heat sinks, copper pours, or thermal vias. Cooler regions marked in purple or blue suggest efficient heat dissipation or components with low power consumption.

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 CONCLUSION

This study successfully addressed Signal Integrity (SI), Power Integrity (PI), and thermal management challenges in PCBs for Electric Vehicles (EVs) and Uninterruptible Power Supplies (UPS). Using advanced design techniques and HyperLynx VX.2.10 simulations, the optimized PCB design achieved improved reliability, efficiency, and compliance with IPC-2221 and IPC-6012 standards.

SI issues like reflections, crosstalk, and EMI were mitigated through impedance matching, controlled routing, and differential signal paths, ensuring high-frequency signal fidelity. PI improvements included optimized power planes and decoupling capacitors, minimizing voltage drops (0.024%) and achieving uniform current density (4.1 mA/mil^2). Effective thermal management using vias, heat sinks, and reconfigured layers kept operating temperatures safe.This integrated approach validated solutions, reduced prototyping costs, and demonstrated a robust framework for high-performance PCB design in critical applications.

7.2 FUTURE WORK

This study's findings provide a strong foundation for developing robust and efficient PCBs, but further exploration is essential. Real-world testing under actual operating conditions will validate simulation results and uncover practical limitations. Additionally, advanced materials like aluminum-backed laminates or flexible substrates could significantly enhance thermal and electrical performance, paving the way for next-generation designs.

Future work can leverage emerging technologies such as machine learning and AI to optimize signal integrity, power integrity, and thermal behavior, reducing design cycles and improving precision. Scaling these solutions to complex PCB designs, including multi-layered boards for autonomous vehicles or industrial UPS systems, will address challenges like higher component density and mixed-signal systems. These advancements will support the evolving demands of modern electronic systems and drive progress in EV and UPS technologies.

REFERENCES

[1] Z. Xia, Y. Luo, Y. Qi, J. Fan and X. Ye, "PCB-Level Thermal & SI/PI Co-Analysis: Progress and Directions," *2022 Asia-Pacific International Symposium on Electromagnetic Compatibility (APEMC)*, Beijing, China, 2022, pp. 627–629, doi: 10.1109/APEMC53576.2022.9888294.
Available: https://ieeexplore.ieee.org/document/9888294

[2] M. Schierholz *et al*., "SI/PI-Database of PCB-Based Interconnects for Machine Learning Applications," *IEEE Access*, vol. 9, pp. 34423–34432, 2021, doi: 10.1109/ACCESS.2021.3061788.
Available: https://ieeexplore.ieee.org/document/9361755

[3] Y. Shen, H. Wang, F. Blaabjerg, H. Zhao and T. Long, "Thermal Modeling and Design Optimization of PCB Vias and Pads," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 882–900, Jan. 2020, doi: 10.1109/TPEL.2019.2915029.
Available: https://ieeexplore.ieee.org/document/8706634

[4] K. Sanjitha, V. Panduranga and S. Mallesh, "Thermal Analysis of Different Components on the PCB Using ANSYS Software," in V. K. Gunjan, P. N. Suganthan, J. Haase and A. Kumar (eds.), *Cybernetics, Cognition and Machine Learning Applications*, Algorithms for Intelligent Systems, Springer, Singapore, 2023.
Available: https://link.springer.com/chapter/10.1007/978-981-19-1484-3_17

[5] S.-H. You *et al*., "Advanced Fan-Out Package SI/PI/Thermal Performance Analysis of Novel RDL Packages," *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, San Diego, CA, USA, 2018, pp. 1295–1301.
Available: https://ieeexplore.ieee.org/document/8429712

[6] Y. Guo *et al*., "Far-End Crosstalk Control Strategy for High-Volume High-Speed PCB Manufacturing: The Concept of Critical Resin Content Percent," *2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, Raleigh, NC, USA, 2021, pp. 820–824, doi: 10.1109/EMC/SI/PI/EMCEurope52599.2021.9559363.
Available: https://ieeexplore.ieee.org/document/9559363

[7] F. Zhao *et al*., "Application of Thermal Network Approach to Electrical-Thermal Co-Simulation and Chip-Package-Board Extraction," *2018 34th Thermal Measurement, Modeling & Management Symposium (SEMI-THERM)*, San Jose, CA, USA, 2018, pp. 1–7, doi: 10.1109/SEMI-THERM.2018.8357345.
Available: https://ieeexplore.ieee.org/document/8357345

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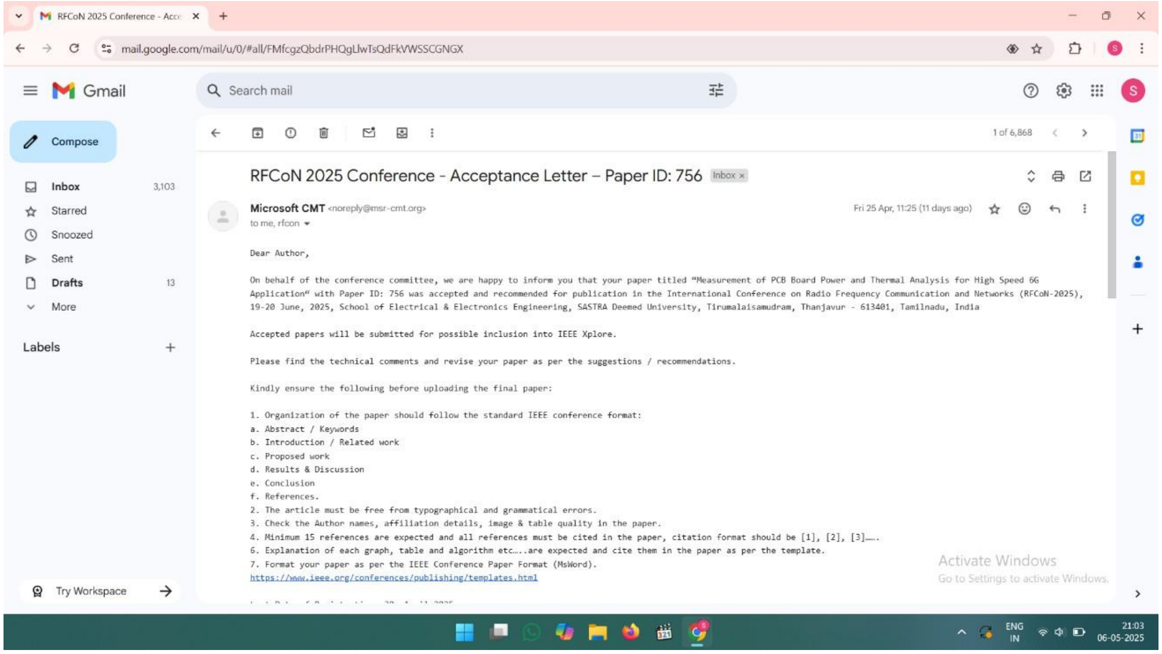

RFCoN 2025 Conference - Acceptance Letter – Paper ID: 756

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to me, rfcon
Fri 25 Apr, 11:25 (11 days ago)

Dear Author,

On behalf of the conference committee, we are happy to inform you that your paper titled "Measurement of PCB Board Power and Thermal Analysis for High Speed 6G Application" with Paper ID: 756 was accepted and recommended for publication in the International Conference on Radio Frequency Communication and Networks (RFCoN-2025), 19-20 June, 2025, School of Electrical & Electronics Engineering, SASTRA Deemed University, Tirumalaisamudram, Thanjavur - 613401, Tamilnadu, India

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3. Check the Author names, affiliation details, image & table quality in the paper.
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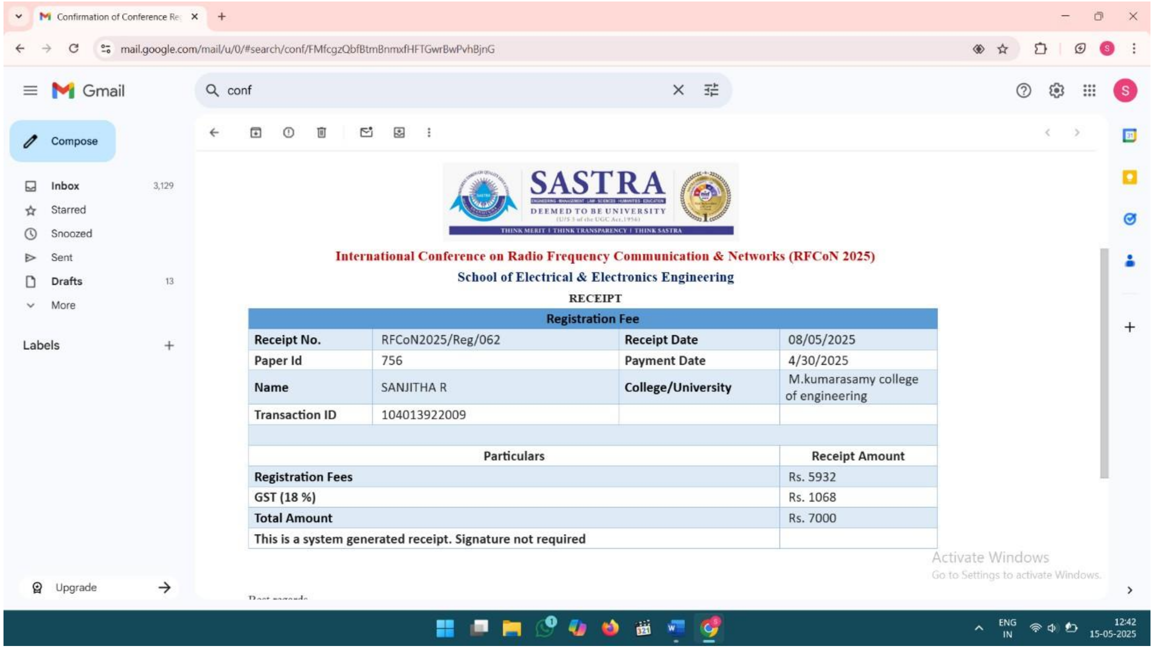
6. Explanation of each graph, table and algorithm etc…..are expected and cite them in the paper as per the template.
7. Format your paper as per the IEEE Conference Paper Format (MsWord).
https://www.ieee.org/conferences/publishing/templates.html



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School of Electrical & Electronics Engineering
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