An FGPA Based General Purpose DAQ Module for the KLOE-2 Experiment

P. Branchini, A. Budano, A. Balla, M. Beretta, P. Ciambrone, and E. De Lucia

***Abstract*—A general purpose FPGA based DAQ module has been developed. This module has been built around a Virtex-4 FPGA and it is able to acquire up to 1024 different channels distributed over 10 slave cards. The module has an optical interface, a RS-232 port, a USB and a Gigabit Interface. The KLOE-2 experiment is going to use this module to acquire data from the Inner tracker. An embedded processor (Power PC) is present on the FPGA and a telnet server has been developed and installed. A new general purpose data taking system has been based on this new module to acquire the Inner Tracker. The system is presently working at LNF (Laboratori Nazionali di Frascati).**

***Index Terms*—Data acquisition, GEM, trigger.**

I. Introduction

THIS document describes a prototype of Data Acquisition System (DAQ) for the Inner Tracker (IT) of the KLOE-2 experiment at the Frascati ϕ-factory DAφNE, an e^-e^+ collider operated at the energy of 1020 MeV.

After the completion of the KLOE data taking [1], a proposal has been presented for a physics program to be carried out with an upgraded KLOE detector, KLOE-2 [2], at an upgraded DAφNE machine, which has been assumed to deliver an integrated luminosity of O(20) fb^{-1}. A new interaction region will be implemented by the Accelerator Division in Frascati with the goal of reaching a luminosity of $5 \times 10^{32}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$.

The KLOE-2 physics program will be focused on physics coming from the Interaction Point (IP), where the ϕ-meson is produced. Its decays into K_S, $K^{\pm}$, η and η' decays as well as $K_S - K_L$ interference and search for physics beyond the Standard Model will be studied in this environment. The improvement in the reconstruction performance for tracks near the interaction region is then of fundamental importance for the accomplishment of this physics program.

The Inner Tracker (IT) [3] will be placed between the beam pipe and the DC inner wall. The proposed solution consists of four independent tracking layers, each providing a 3-D reconstruction of space points along the track with a 2-D readout. The innermost layer is placed at 12.7 cm from the beam line, corresponding to 20 τ_S, K_S lifetime, avoiding to spoil the $\mathrm{K_S} - \mathrm{K_L}$ interference pattern. We have chosen to realize each layer as a cylindrical-GEM detector (CGEM) [4]. A 3D model of the IT detector can be observed in Fig. 1.

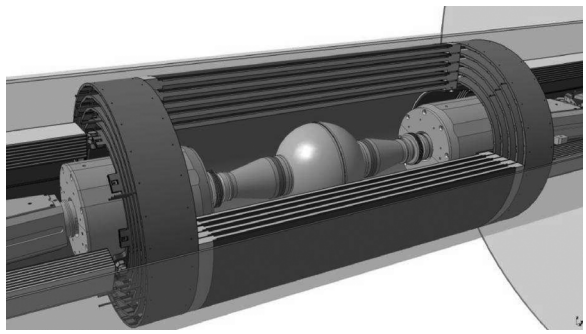

Fig. 1. Design of the KLOE-2 interaction region, showing the new inner tracker and low-angle calorimeters.

In order to integrate the IT within the KLOE DAQ the following must be taken into account: since the Level 1 trigger is delayed by about 200 ns with respect to the Bunch Crossing (BX), the IT discriminated signals must be properly stretched to be acquired. To fulfill the mentioned requirements a novel 64 channels front-end ASIC prototype, named GASTONE (Gem Amplifier Shaper Tracking ON Events) [5], has been developed; this version is a mixed analog-digital circuit, consisting of 64 analog channels followed by a digital section implementing the slow control and readout interface.

The amplified and shaped signals are digitized and serially read out using both edges of a 50 MHz clock, achieving a 100 Mbps transfer rate. The maximum trigger rate of the KLOE-2 experiment will be 10 kHz. The number of channels of the IT is less than 30000. Each channel is coded in a single bit value (ON/OFF). Their acquisition is partitioned in 24 DAQ chains each equipped with an OGE (Off Gastone Electronics) board. Therefore the maximum throughput per board, without using the zero suppression algorithm, is less than 1.5 MB/s.

II. The IT DAQ Test Stand

In this paper we presents the first experimental setup that we have realized in order to test the final IT DAQ System. In particular we have used as detector a telescope of five layers of planar triple-GEMs detectors with 650 μm pitch (more details can be found in [3] and [4]). The five detectors are equally spaced between each other, with the chamber with XY read out placed at the center (see left Fig. 2). The entire setup is 1 meter long.

The acquisition system is composed by three electronic systems: the front-end boards (Gastone card), the OGE board, and the on-line Farm System.

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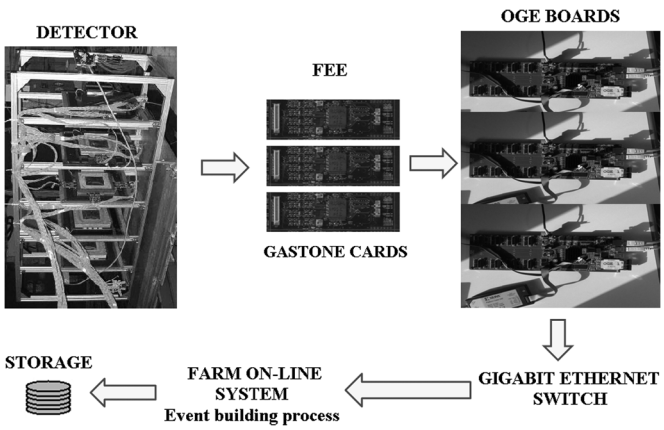

Fig. 2. The Architecture of the DAQ System: the detector is made by 5 GEM layers. The detector is acquired using the Gastone cards interconnected to the OGE Boards. Then using the Ethernet connection the data in the OGE Board are sent to the Farm on-line system. Finally the data are written to the storage disks.

Each Gastone Card can process signals coming from a total of 128 channels of the detector and is connected to the OGE, using a three meter long twisted pair cable (13 pairs).

The OGE board has been designed to set the front-end parameters, deliver the power supply and download data from up to eight Gastone cards (1024 channels). The OGE board performs also a first level event building.

Using an address logic it is possible to set the parameters of OGE boards and Gastone cards.

The stand alone OGE boards are based on a Xilinx Virtex 4FX FPGA (Field Programmable Gate Array). An embedded IBM Power PC (PPC405) runs at 300 MHz on the FPGA. All the peripherals are connected to the processor through the PLB46 (Processor Local Bus) bus running at 100 MHz.

The processor is interfaced with the external world through four different peripherals: the 2 Gb/s Optical Port and Gigabit Ethernet to deliver data to the on line farm; full speed USB2 and RS232 are implemented only for debugging and testing purposes. Moreover, this core, when enabled, performs zero suppression algorithm. Afterwards data are stored in a FIFO and sent to the DAQ either via 2 Gb/s optical link [6], [7] or using the 1 Gb/s Ethernet link.

The FPGA embedded memory connected to the Power PC is 64 Kbyte in total. This memory is exploited to store the data coming from the Gastone Cards (56 Kbyte) and part of the instructions (8 Kbyte).

Due to the complexity of the operations to be performed, the code size of the acquisition software is greater than the processor memory available on-chip (8 Kbyte).

A boot loader had to be implemented to download the instructions of the acquisition software from the flash memory to an external DDR2 memory. The CPU on the FPGA fetches the instructions directly from the DDR2. The need for the boot loader is the main disadvantage of this architecture.

The layout of the full system is shown in Fig. 2, with the OGE board connected to the DAQ system by the Ethernet interface.

A PC based DAQ system equipped with a Gigabit Ethernet interface is used as Farm system and multiple OGE boards are also used in the DAQ for testing the event building algorithm.

III. DAQ Software Architecture

In order to acquire data events from a single OGE board, in the FPGA chip we have built a telnet server that listens to the Ethernet port using the TCP/IP protocol using the internal driver of the Power PC core with Linux. This server allows to manage the board and all Gastone cards connected to it. In particular it's possible to set and read all the registers belonging to specific components by sending a specific command to the server, returning as output the value of this register. The registers are memory mapped into the PPC405 processor addressing space. This allows us to set the Gastone chip parameters such as thresholds, masked channels and pulse signal amplitude, and to read the acquisition parameters such as trigger count. A single TCP socket is established for each OGE board. Data are delivered to the Farm through this TCP socket stream. We have written a data collection process named L2GET which is in charge of collecting data streams coming from different OGE boards. Moreover this process stores the data of a FIFO structured shared memory.

Finally a Farm process (named farmbuild) performs event building functions. This process accesses the data from the shared memory filled by all the L2GETs processes and builds the event by merging all the fragments delivered by the different sources.

IV. Run Control

In order to manage the DAQ system and configure the Front-end Electronics (FEE), a simple Graphical User Interface (GUI) was built. This GUI named "Run Control" was written in Java and allows us to program the OGE board and the 16 Gastone chips hosted on each board.

The Application Window is logically divided into three areas: an area with buttons to manage the DAQ system process, a second area which checks the DAQ parameters and finally the text box, in white, in the lower part of the window. This part allows to read messages coming from the DAQ system. There is also the possibility to configure the FEE such as Gastone Cards and some other options on the OGE Board. A snapshot of the windows application is shown in Fig. 3.

A Java class was implemented to start the appropriate DAQ command with ssh remote login. In this way the computer where the control process runs can be independent from the DAQ system computers. The application give the possibility to select among several type of runs: Production run, Pulse run and Calibration run.

The Production run allows us to set the correct parameters on the Front-ends and starts the DAQ process to acquire the physics events. A pulsing system has been implemented on the Gastone card and the pulse amplitude can be set optimizing the signal to noise ratio. The Pulse run sets the corresponding parameters on the Gastone cards and on the OGE boards in order to pulse the odd (or even) channels: this feature is used for debugging the Front-end electronic. Finally the Calibration run allows to find the best thresholds for the Gastone chips, by setting a specific value for the delivered pulsing signal and by varying the thresholds for the single channels until only half of the events overcome the thresholds (50% occupancy).

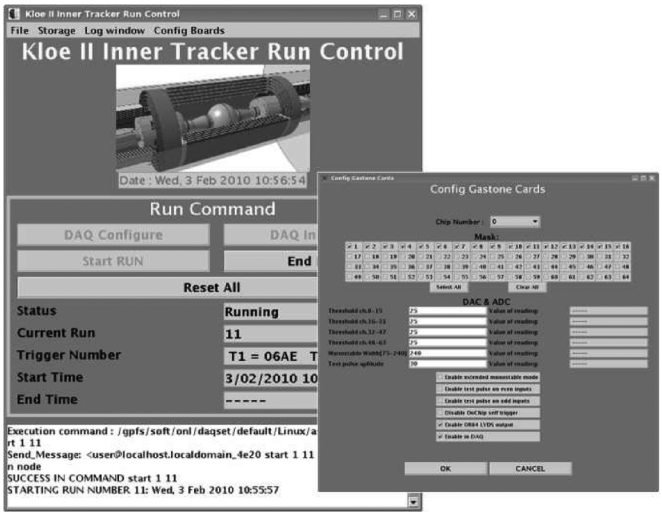

Fig. 3. A snapshot of the Run Control Application. This application is used for managing the full DAQ System and for configuring the parameters of the Gastone Cards and the OGE Board.

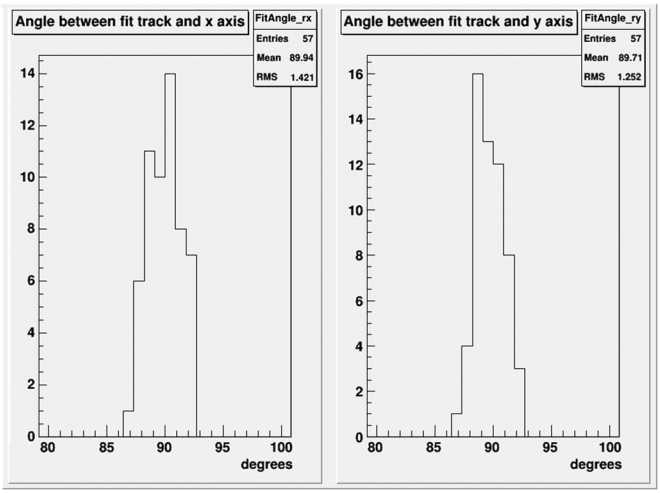

Fig. 4. Angular distribution of the track. The track are built by using the 2nd and 3rd layers.

V. DAQ Performance

The DAQ systems is made by 16 Gastone Cards and 2 OGE Boards, needed for acquiring the full detector.

We have measured a value of up to 300 kB/s of data coming from each OGE board. The throughput is limited because the OGE board can store only one single event into the data FIFO. The TCP transfer then takes place for one event at the time: a new event cannot be stored into the FIFO memory before the memory itself is emptied.

In order to test the data acquisition and the detector we have collected cosmic-ray events. The Gastone chip can deliver a discriminated signal based on the OR of the read out channels (OR64). A trigger has been asserted only when the OR64 signals delivered from the first and last chamber was present within a 100 ns window.

Pulse runs were routinely done to debug the setup before starting long cosmic runs.

Finally we have analyzed the data in order to track the trajectory of cosmic-ray events in our detector. In Fig. 4. we show the angular distribution of the tracks.

The tracks are reconstructed using the second and third layers. The average value of the angle of about 90 degree and its root mean square of about 1.5 degree reflect the setup of the chambers with two $4.16 \times 4.16\ \mathrm{cm}^2$ areas instrumented with Gastone readout at a distance of 50 cm.

VI. Future Development

In order to increase DAQ performance we intend to increase the current FIFO memory on the OGE board. The data FIFO will be stored on the external memory. Therefore we will store up to 1000 events onto the memory. In this way we will be able to transfer several events at the time thus overcoming the experienced bandwidth limitation. The architecture discussed is used only for testing purposes and will not be used to deliver data to the optical link already present on the board. A dedicated hardware present on the board is in charge of retrieving data from the memory buffer and delivering them to the optical link.

A new board, named Concentrator Board (CB), is under test. This board has 16 optical ports to acquire 16 OGE boards and an FPGA to perform the event building procedure [8]. The VME interface in the CB will be used for managing/acquiring this board.

VII. Conclusion

The Gastone cards and OGE Boards have been integrated successfully in a single test stand. The design was reliable and easy to use. We have found the Power PC architecture powerful enough for our debugging software architecture. The full DAQ System has been running smoothly since then. An offline analysis program has been written to analyze and monitor collected data.

This general purpose DAQ system can be used to acquire data from other detectors. In KLOE-2 it will be used to collect data from other detectors foreseen in the upgrade [9].

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