VLSI

PROJECT

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Roll. No: 2020102061

Objective:

Designing 4-bit Carry look ahead adder. And we need to consider Lamda=0.09 micro-meter, Wp=1.8 micro-meter and Wn=0.9 micro-meter.

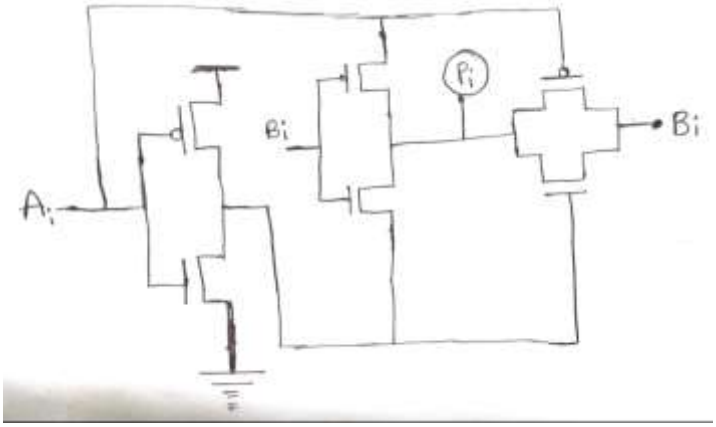
Structure for the adder:

CLA Adder: If the numbers to be added are a4a3a2a1 and b4b3b2b1, then the propagate and generate signals for each bit position can be defined as Pi=Ai ⊕ Bi and Gi=Ai.Bi

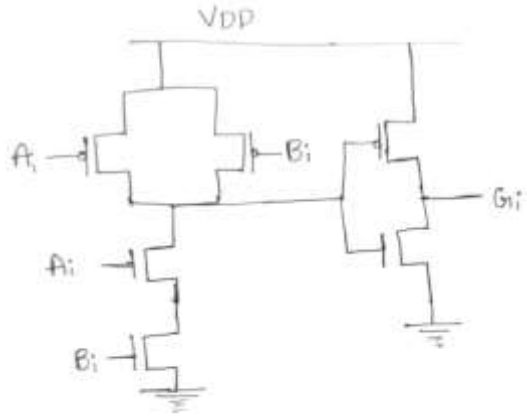
- P1=A1⊕ B1, G1=A1.B1
- P2=A2⊕ B2, G2=A2.B2
- P3=A3⊕ B3, G3=A3.B3
- P4=A4⊕ B4, G4=A4.B4

- Transistor level circuits for the above are as follows and I considered the same way in ngspice:

Pi=Ai XOR Bi



Gi=Ai.Bi



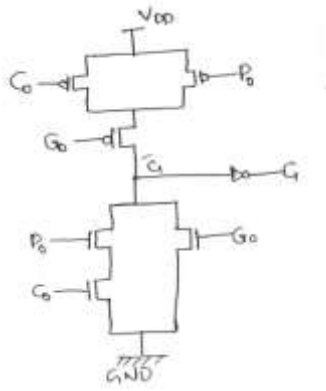
The carry out of the cith bit position can be written as:

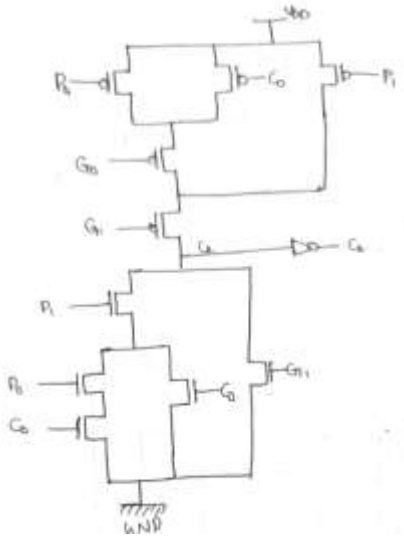
C_(i+1) =(PiCi)+Gi; Here we consider input C1=0.

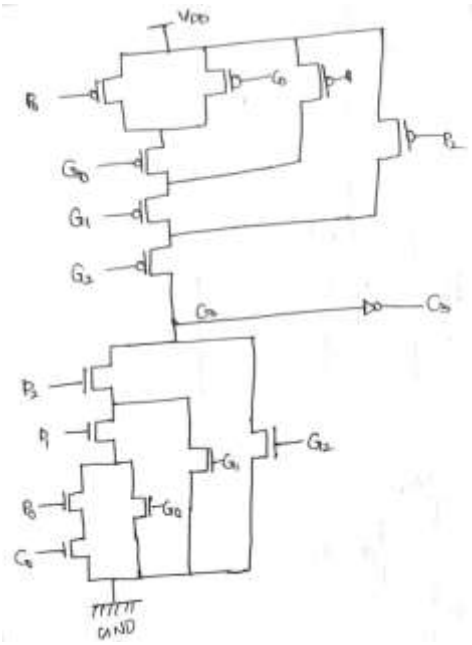
- C2=P1C1+G1; as C1=0 then C2=G1
- C3=P2C2+G2=P2(P1C1+G1) +G2=P1P2C1+P2G1+G2; as C1=0 then C3=P2G1+G2
- C4=P3C3+G3=P3(P1P2C1+P2G1+G2) +G3=P3P2P1C1+P3P2G1+P3G2+G3; as C1=0 then C4=P3P2G1+P3G2+G3
- C5=P4C4+G4=P4(P1P2P3C1+P2P3G1+P3G2+G3) +G4; If C1=0 then C5=P2P3P4G1+P3P4G2+P4G3+G4

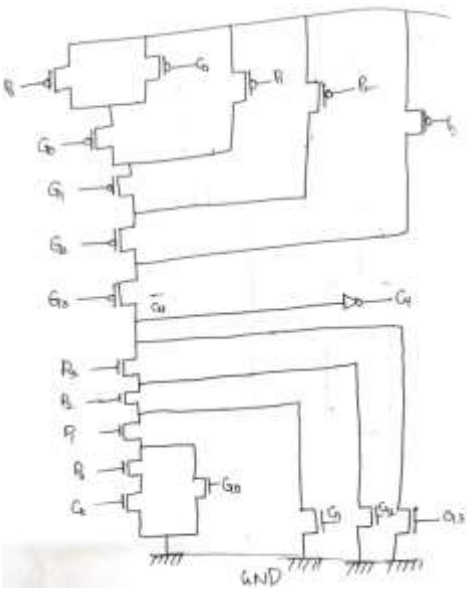
Transistor level circuits for the above Carries are as follows:

In circuit diagrams, I considered the input carry as C0 and drawn for C1, C2, C3 and C4. (Similar to that of C2 C3 C4 C5 wrote above)




Vdd
GND

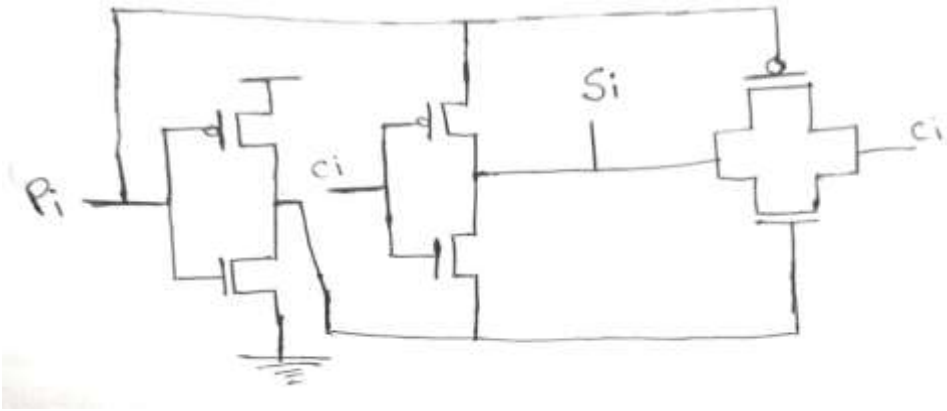

Vdd
GND


GND

- Sum can be expressed as follows: Si=Pi ⊕ Ci

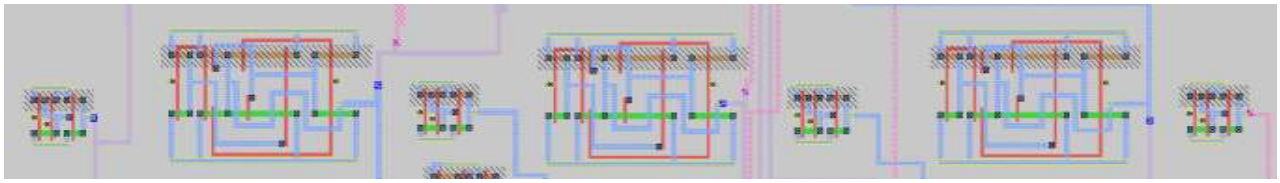
- S1=P1 ⊕ C1
- S2=P2 ⊕ C2
- S3=P3 ⊕ C3
- S4=P4 ⊕ C4

The circuit looks as below:



Topology and sizing:

- First, we need **propagate and generate** signals. Thus, we need 4 XOR and 4 AND gates.



- The area for this is 208*184.

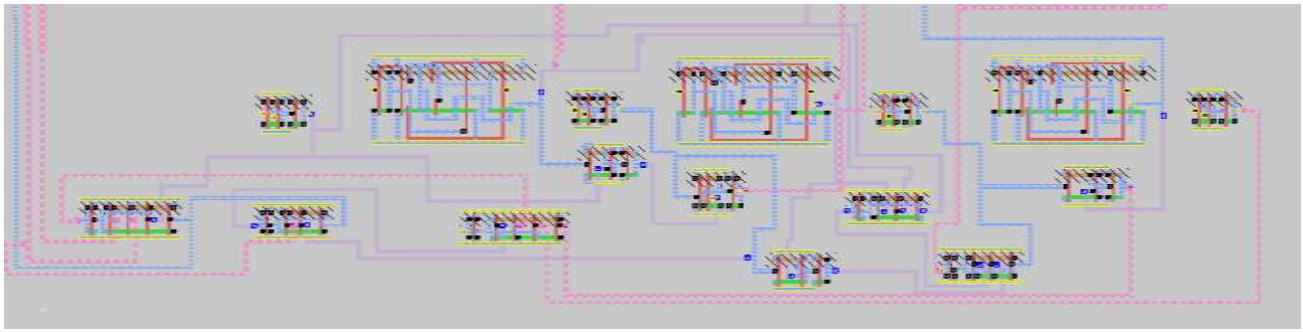
- For **Carry block**:

→ For C2: We already know that C2 = G1 as C1=0. S0, we directly used one 'AND' for G1.

→ For C3: We know that C3= P2G1+G2 as C1=0. So, here we use one 'AND' for inputs G1 and P2(P2 need one XOR and G1 need one AND) and one 'OR' for inputs G2 and P2G1.

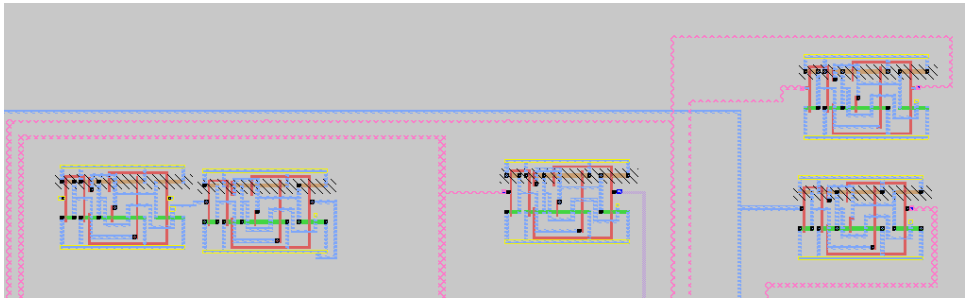
→ For C4: We know that C4= P3P2G1+P3G2+G3 as C1=0. We need one two input 'AND', one three input 'AND' and one three input OR.

→ For C5: We know that C5=P2P3P4G1+P3P4G2+P4G3+G4 as C1=0.So, here we use 1 two input 'AND', 1 three input 'AND', 1 four input 'AND' and 1 four input 'OR' gate.



- For **Sum block:**

→ For S1: We know that S1= P1 ⊕ C1. So, we need 1 XOR.
→ For S2: We know that S2= P2 ⊕ C2. So, we need 1 XOR.
→ For S3: We know that S3= P3 ⊕ C3. So, we need 1 XOR.
→ For S4: We know that S4= P4 ⊕ C4. So, we need 1 XOR.



- So, the entire layout sizing is as follows:

Sizing:

width x height (llx, lly), (urx, ury) area (units^2)

microns: 112.14 x 58.05 (-3.96, 0.27), (108.18, 58.32) 6509.73

lambda: 1246 x 645 (-44, 3), (1202, 648) 803670

Verification of each block using NGSpice:

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1. For Propagate and Generate:

- I considered the input carry as C0 and drawn for C1, C2, C3 and C4. (Similar to that of C2 C3 C4 C5 wrote above)

Code:

Netlist for Propagator's and Generators:

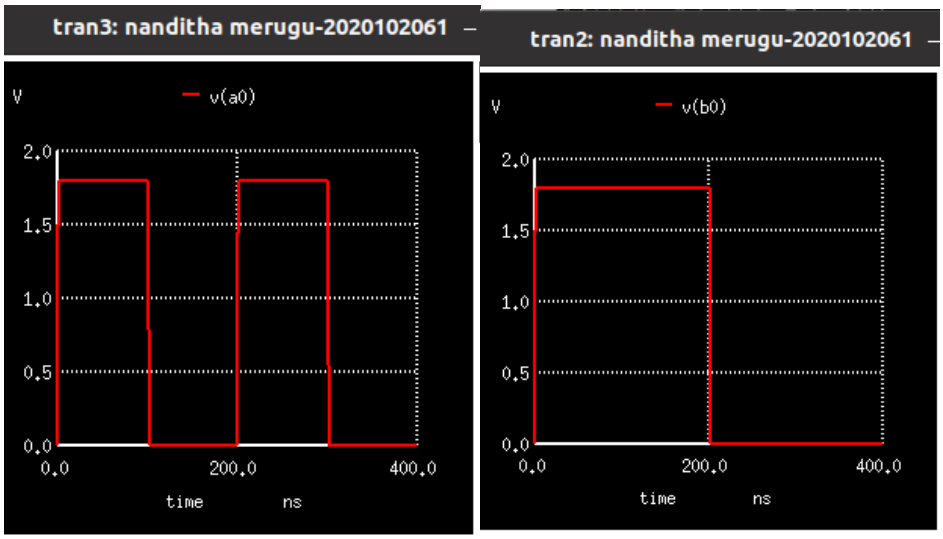
```
.include TSMC_180nm.txt
.param supply = 1.8

VCC net1 GND supply

*G0 = A0.B0
MP9 o1 A0 net1 net1 CMOSP W=1.8u L=180nm
MP10 o1 B0 net1 net1 CMOSP W=1.8u L=180nm
MN9 o1 A0 o2 GND CMOSN W=0.9u L=180nm
MN10 o2 B0 GND GND CMOSN W=0.9u L=180nm
MP11 G0 o1 net1 net1 CMOSP W=1.8u L=180nm
MN11 G0 o1 GND GND CMOSN W=0.9u L=180nm

*G1=A1.B1
MP12 o3 A1 net1 net1 CMOSP W=1.8u L=180nm
MP13 o3 B1 net1 net1 CMOSP W=1.8u L=180nm
MN12 o3 A1 o4 GND CMOSN W=0.9u L=180nm
MN13 o4 B1 GND GND CMOSN W=0.9u L=180nm
MP14 G1 o3 net1 net1 CMOSP W=1.8u L=180nm
MN14 G1 o3 GND GND CMOSN W=0.9u L=180nm

*G2=A2.B2
MP15 o5 A2 net1 net1 CMOSP W=1.8u L=180nm
MP16 o5 B2 net1 net1 CMOSP W=1.8u L=180nm
MN15 o5 A2 o6 GND CMOSN W=0.9u L=180nm
MN16 o6 B2 GND GND CMOSN W=0.9u L=180nm
MP17 G2 o5 net1 net1 CMOSP W=1.8u L=180nm
MN17 G2 o5 GND GND CMOSN W=0.9u L=180nm

*G3=A3.B3
MP18 o7 A3 net1 net1 CMOSP W=1.8u L=180nm
MP19 o7 B3 net1 net1 CMOSP W=1.8u L=180nm
MN18 o7 A3 o8 GND CMOSN W=0.9u L=180nm
MN19 o8 B3 GND GND CMOSN W=0.9u L=180nm
MP20 G3 o7 net1 net1 CMOSP W=1.8u L=180nm
MN20 G3 o7 GND GND CMOSN W=0.9u L=180nm

*P0=A0 XOR B0
MP21 o9 A0 net1 net1 CMOSP W=1.8u L=180nm
MN21 o9 A0 GND GND CMOSN W=0.9u L=180nm
MP22 P0 B0 A0 net1 CMOSP W=1.8u L=180nm
MN22 P0 B0 o9 GND CMOSN W=0.9u L=180nm
MP23 P0 A0 B0 net1 CMOSP W=1.8u L=180nm
MN23 B0 o9 P0 GND CMOSN W=0.9u L=180nm
```

```
*P1=A1 XOR B1
MP24 o10 A1 net1 net1 CMOSP W=1.8u L=180nm
MN24 o10 A1 GND GND CMOSN W=0.9u L=180nm
MP25 P1 B1 A1 net1 CMOSP W=1.8u L=180nm
MN25 P1 B1 o10 GND CMOSN W=0.9u L=180nm
MP26 P1 A1 B1 net1 CMOSP W=1.8u L=180nm
MN26 B1 o10 P1 GND CMOSN W=0.9u L=180nm

*P2=A2 XOR B2
MP27 o11 A2 net1 net1 CMOSP W=1.8u L=180nm
MN27 o11 A2 GND GND CMOSN W=0.9u L=180nm
MP28 P2 B2 A2 net1 CMOSP W=1.8u L=180nm
MN28 P2 B2 o11 GND CMOSN W=0.9u L=180nm
MP29 P2 A2 B2 net1 CMOSP W=1.8u L=180nm
MN29 B2 o11 P2 GND CMOSN W=0.9u L=180nm

*P3=A3 XOR B3
MP30 o12 A3 net1 net1 CMOSP W=1.8u L=180nm
MN30 o12 A3 GND GND CMOSN W=0.9u L=180nm
MP31 P3 B3 A3 net1 CMOSP W=1.8u L=180nm
MN31 P3 B3 o12 GND CMOSN W=0.9u L=180nm
MP32 P3 A3 B3 net1 CMOSP W=1.8u L=180nm
MN32 B3 o12 P3 GND CMOSN W=0.9u L=180nm

Vin1 A0 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin2 B0 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)
Vin3 A1 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin4 B1 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)
Vin5 A2 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin6 B2 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)
Vin7 A3 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin8 B3 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)
Vin9 C0 GND pulse (0 0 0 0.5p 0.5p 0.2u 0.4u)

Cap1 G0 GND 0.1p
Cap2 G1 GND 0.1p
Cap3 G2 GND 0.1p
Cap4 G3 GND 0.1p
Cap5 P0 GND 0.1p
Cap6 P1 GND 0.1p
Cap7 P2 GND 0.1p
Cap8 P3 GND 0.1p

.tran 1n 0.4u
.control
run

set curplottitle="Nanditha Merugu-2020102061"
```

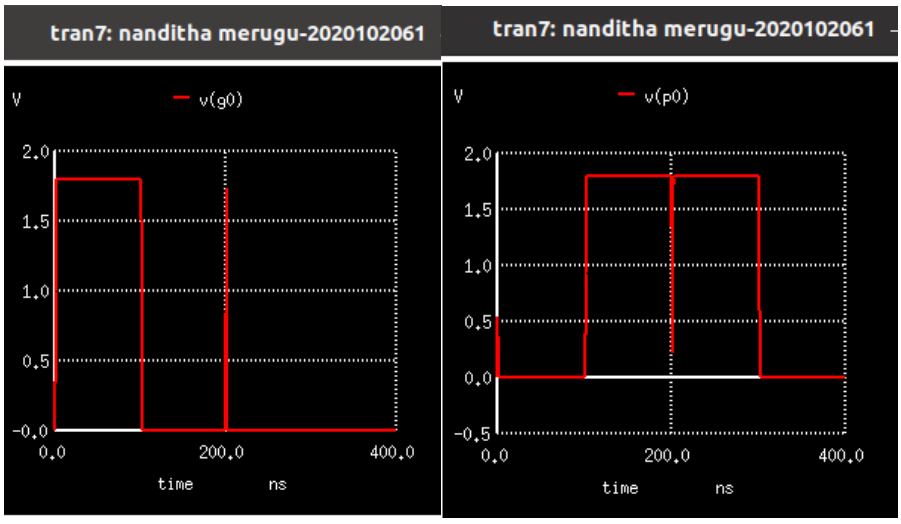
```
plot v(A2)
set curplottitle="Nanditha Merugu-2020102061"
plot v(B2)
set curplottitle="Nanditha Merugu-2020102061"
plot v(G2)
set curplottitle="Nanditha Merugu-2020102061"
plot v(P2)

.endc
.end
```

Plots:

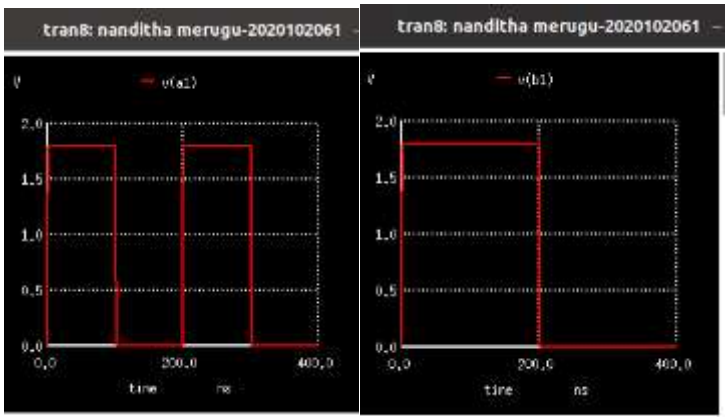
A0 and B0



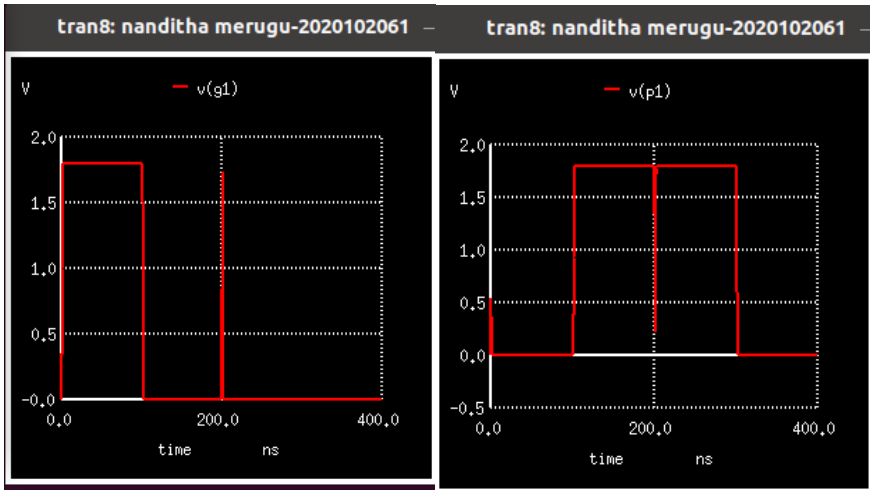
G0=A0.B0 and P0=A0 XOR B0



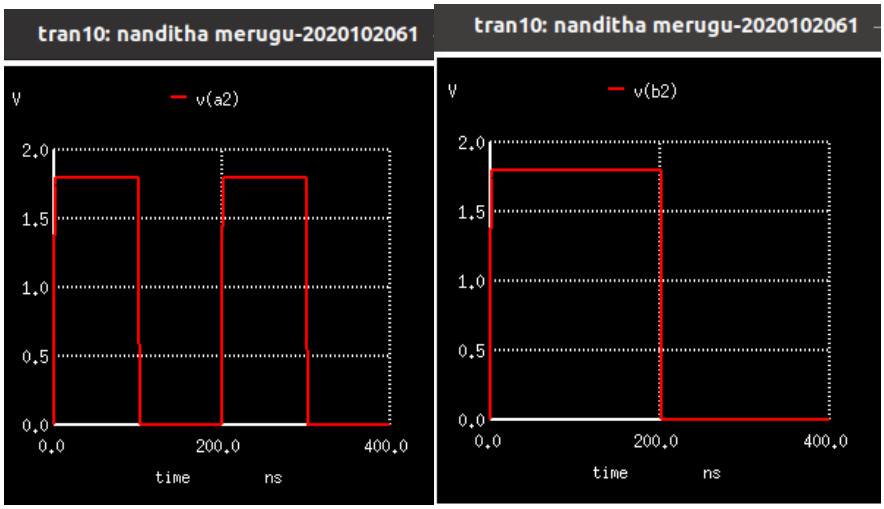
A1 and B1



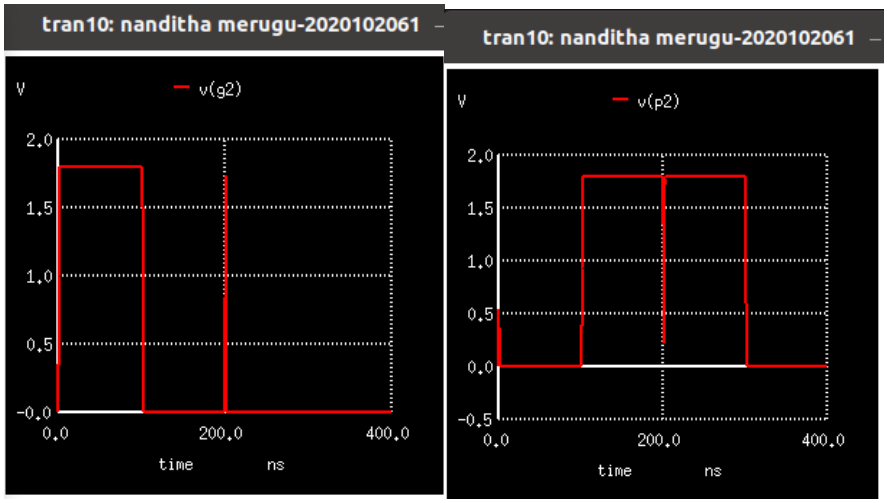
G1=A1.B1 and P1=A1 XOR B1



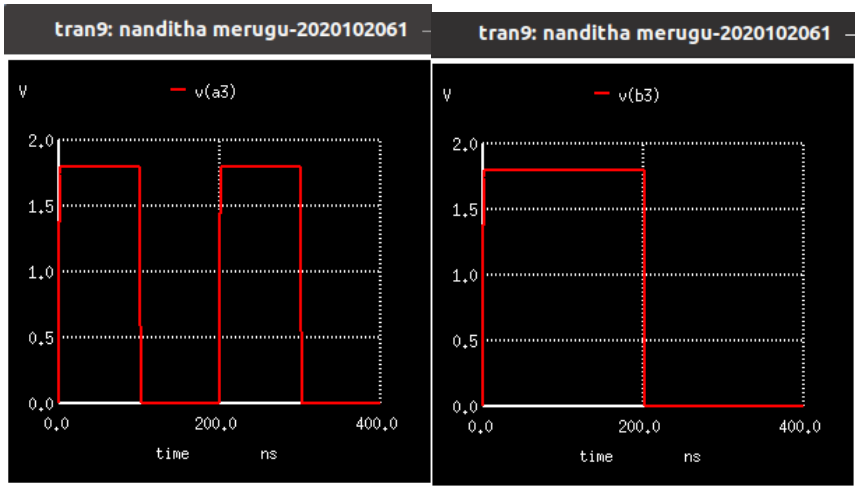
A2 and B2



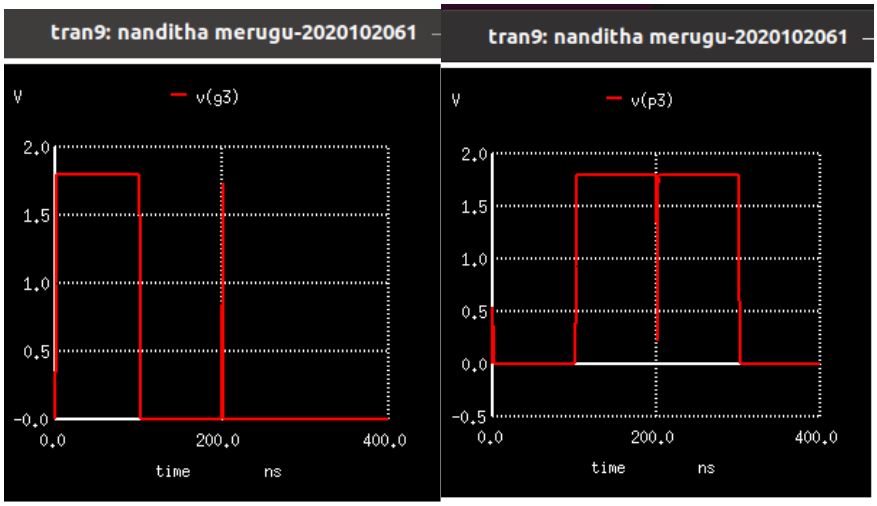
G2=A2.B2 and P2=A2 XOR B2



A3 and B3



G3=A3.B3 and P3=A3 XOR B3



XOR

0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

I used this Truth-table to verify the plots of Propagate's. And all are found to be correct.

AND

0	**0**	**0**
0	**1**	**0**
1	**0**	**0**
1	**1**	**1**

I used this Truth-table to verify plots of generate's. And all are found to be correct.

2. For Carry and Sum:

Netlist for Carry and Sum:

```
.include TSMC_180nm.txt
.param supply = 1.8

VCC net1 GND supply


*G0
MP9 o1 A0 net1 net1 CMOSP W=1.8u L=180nm
MP10 o1 B0 net1 net1 CMOSP W=1.8u L=180nm
MN9 o1 A0 o2 GND CMOSN W=0.9u L=180nm
MN10 o2 B0 GND GND CMOSN W=0.9u L=180nm
MP11 G0 o1 net1 net1 CMOSP W=1.8u L=180nm
MN11 G0 o1 GND GND CMOSN W=0.9u L=180nm

*G1
MP12 o3 A1 net1 net1 CMOSP W=1.8u L=180nm
MP13 o3 B1 net1 net1 CMOSP W=1.8u L=180nm
MN12 o3 A1 o4 GND CMOSN W=0.9u L=180nm
MN13 o4 B1 GND GND CMOSN W=0.9u L=180nm
MP14 G1 o3 net1 net1 CMOSP W=1.8u L=180nm
MN14 G1 o3 GND GND CMOSN W=0.9u L=180nm

*G2
MP15 o5 A2 net1 net1 CMOSP W=1.8u L=180nm
MP16 o5 B2 net1 net1 CMOSP W=1.8u L=180nm
```

```
MN15 o5 A2 o6 GND CMOSN W=0.9u L=180nm
MN16 o6 B2 GND GND CMOSN W=0.9u L=180nm
MP17 G2 o5 net1 net1 CMOSP W=1.8u L=180nm
MN17 G2 o5 GND GND CMOSN W=0.9u L=180nm

*G3
MP18 o7 A3 net1 net1 CMOSP W=1.8u L=180nm
MP19 o7 B3 net1 net1 CMOSP W=1.8u L=180nm
MN18 o7 A3 o8 GND CMOSN W=0.9u L=180nm
MN19 o8 B3 GND GND CMOSN W=0.9u L=180nm
MP20 G3 o7 net1 net1 CMOSP W=1.8u L=180nm
MN20 G3 o7 GND GND CMOSN W=0.9u L=180nm

*P0
MP21 o9 A0 net1 net1 CMOSP W=1.8u L=180nm
MN21 o9 A0 GND GND CMOSN W=0.9u L=180nm
MP22 P0 B0 A0 net1 CMOSP W=1.8u L=180nm
MN22 P0 B0 o9 GND CMOSN W=0.9u L=180nm
MP23 P0 A0 B0 net1 CMOSP W=1.8u L=180nm
MN23 B0 o9 P0 GND CMOSN W=0.9u L=180nm

*P1
MP24 o10 A1 net1 net1 CMOSP W=1.8u L=180nm
MN24 o10 A1 GND GND CMOSN W=0.9u L=180nm
MP25 P1 B1 A1 net1 CMOSP W=1.8u L=180nm
MN25 P1 B1 o10 GND CMOSN W=0.9u L=180nm
MP26 P1 A1 B1 net1 CMOSP W=1.8u L=180nm
MN26 B1 o10 P1 GND CMOSN W=0.9u L=180nm

*P2
MP27 o11 A2 net1 net1 CMOSP W=1.8u L=180nm
MN27 o11 A2 GND GND CMOSN W=0.9u L=180nm
MP28 P2 B2 A2 net1 CMOSP W=1.8u L=180nm
MN28 P2 B2 o11 GND CMOSN W=0.9u L=180nm
MP29 P2 A2 B2 net1 CMOSP W=1.8u L=180nm
MN29 B2 o11 P2 GND CMOSN W=0.9u L=180nm

*P3
MP30 o12 A3 net1 net1 CMOSP W=1.8u L=180nm
MN30 o12 A3 GND GND CMOSN W=0.9u L=180nm
MP31 P3 B3 A3 net1 CMOSP W=1.8u L=180nm
MN31 P3 B3 o12 GND CMOSN W=0.9u L=180nm
MP32 P3 A3 B3 net1 CMOSP W=1.8u L=180nm
MN32 B3 o12 P3 GND CMOSN W=0.9u L=180nm

*C1=G0+P0C0
MP33 o13 C0 net1 net1 CMOSP W=1.8u L=180nm
MP34 o13 P0 net1 net1 CMOSP W=1.8u L=180nm
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```
MP35 o14 G0 o13 net1 CMOSP W=1.8u L=180nm
MN33 o14 P0 o15 GND CMOSN W=0.9u L=180nm
MN34 o15 C0 GND GND CMOSN W=0.9u L=180nm
MN35 o14 G0 GND GND CMOSN W=0.9u L=180nm
MP36 C1 o14 net1 net1 CMOSP W=1.8u L=180nm
MN36 C1 o14 GND GND CMOSN W=0.9u L=180nm

*C2=G1+P1C1=G1+P1(G0+POC0)
MP37 o16 P0 net1 net1 CMOSP W=1.8u L=180nm
MP38 o16 C0 net1 net1 CMOSP W=1.8u L=180nm
MP39 o17 G0 o16 net1 CMOSP W=1.8u L=180nm
MP40 o17 P1 net1 net1 CMOSP W=1.8u L=180nm
MP41 o18 G1 o17 net1 CMOSP W=1.8u L=180nm
MN37 o18 P1 o19 GND CMOSN W=0.9u L=180nm
MN38 019 P0 o20 GND CMOSN W=0.9u L=180nm
MN39 o20 C0 GND GND CMOSN W=0.9u L=180nm
MN40 o19 G0 GND GND CMOSN W=0.9u L=180nm
MN41 o18 G1 GND GND CMOSN W=0.9u L=180nm
MP42 C2 o18 net1 net1 CMOSP W=1.8u L=180nm
MN42 C2 o18 GND GND CMOSN W=0.9u L=180nm

*C3=G2+P2C2=G2+P2(G1+P1C1)=G2+P2[G1+P1(G0+P0C0)]
MP43 o21 P0 net1 net1 CMOSP W=1.8u L=180nm
MP44 o22 G0 o21 net1 CMOSP W=1.8u L=180nm
MP45 o23 G1 o22 net1 CMOSP W=1.8u L=180nm
MP46 o24 G2 o23 net1 CMOSP W=1.8u L=180nm
MP47 o21 C0 net1 net1 CMOSP W=1.8u L=180nm
MP48 o22 P1 net1 net1 CMOSP W=1.8u L=180nm
MP49 o23 P2 net1 net1 CMOSP W=1.8u L=180nm
MN43 o24 P2 o25 GND CMOSN W=0.9u L=180nm
MN44 o25 P1 o26 GND CMOSN W=0.9u L=180nm
MN45 o26 P0 o27 GND CMOSN W=0.9u L=180nm
MN46 o27 C0 GND GND CMOSN W=0.9u L=180nm
MN47 o26 G0 GND GND CMOSN W=0.9u L=180nm
MN48 o25 G1 GND GND CMOSN W=0.9u L=180nm
MN49 o24 G2 GND GND CMOSN W=0.9u L=180nm
MP50 C3 o24 net1 net1 CMOSP W=1.8u L=180nm
MN50 C3 o24 GND GND CMOSN W=0.9u L=180nm

*C4=G3+P3C3=G3+P3[G2+P2[G1+P1(G0+P0C0)]]
MP51 o28 P0 net1 net1 CMOSP W=1.8u L=180nm
MP52 o28 C0 net1 net1 CMOSP W=1.8u L=180nm
MP53 o29 G0 o28 net1 CMOSP W=1.8u L=180nm
MP54 o30 G1 o29 net1 CMOSP W=1.8u L=180nm
MP55 o31 G2 o30 net1 CMOSP W=1.8u L=180nm
MP56 o32 G3 o31 net1 CMOSP W=1.8u L=180nm
MP57 o29 P1 net1 net1 CMOSP W=1.8u L=180nm
MP58 o30 P2 net1 net1 CMOSP W=1.8u L=180nm
```

```
MP59 o31 P3 net1 net1 CMOSP W=1.8u L=180nm
MN51 o32 P3 o33 GND CMOSN W=0.9u L=180nm
MN52 o33 P2 o34 GND CMOSN W=0.9u L=180nm
MN53 o34 P1 o35 GND CMOSN W=0.9u L=180nm
MN54 o35 P0 o36 GND CMOSN W=0.9u L=180nm
MN55 o36 C0 GND GND CMOSN W=0.9u L=180nm
MN56 o32 G3 GND GND CMOSN W=0.9u L=180nm
MN57 o33 G2 GND GND CMOSN W=0.9u L=180nm
MN58 o34 G1 GND GND CMOSN W=0.9u L=180nm
MN59 o35 G0 GND GND CMOSN W=0.9u L=180nm
MP60 C4 o32 net1 net1 CMOSP W=1.8u L=180nm
MN60 C4 o32 GND GND CMOSN W=0.9u L=180nm



**S0=C0 XOR P0
MP61 o40 C0 net1 net1 CMOSP W=1.8u L=180nm
MN61 o40 C0 GND GND CMOSN W=0.9u L=180nm
MP62 S0 P0 C0 net1 CMOSP W=1.8u L=180nm
MN62 S0 P0 o40 GND CMOSN W=0.9u L=180nm
MP63 S0 C0 P0 net1 CMOSP W=1.8u L=180nm
MN63 P0 o40 S0 GND CMOSN W=0.9u L=180nm

**S1=C1 XOR P1
MP64 o41 C1 net1 net1 CMOSP W=1.8u L=180nm
MN64 o41 C1 GND GND CMOSN W=0.9u L=180nm
MP65 S1 P1 C1 net1 CMOSP W=1.8u L=180nm
MN65 S1 P1 o41 GND CMOSN W=0.9u L=180nm
MP66 S1 C1 P1 net1 CMOSP W=1.8u L=180nm
MN66 P1 o41 S1 GND CMOSN W=0.9u L=180nm

**S2=C2 XOR P2
MP67 o42 C2 net1 net1 CMOSP W=1.8u L=180nm
MN67 o42 C2 GND GND CMOSN W=0.9u L=180nm
MP68 S2 P2 C2 net1 CMOSP W=1.8u L=180nm
MN68 S2 P2 o42 GND CMOSN W=0.9u L=180nm
MP69 S2 C2 P2 net1 CMOSP W=1.8u L=180nm
MN69 P2 o42 S2 GND CMOSN W=0.9u L=180nm

**S3=C3 XOR P3
MP70 o43 C3 net1 net1 CMOSP W=1.8u L=180nm
MN70 o43 C3 GND GND CMOSN W=0.9u L=180nm
MP71 S3 P3 C3 net1 CMOSP W=1.8u L=180nm
MN71 S3 P3 o43 GND CMOSN W=0.9u L=180nm
MP72 S3 C3 P3 net1 CMOSP W=1.8u L=180nm
MN72 P3 o43 S3 GND CMOSN W=0.9u L=180nm

Vin1 A0 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin2 B0 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)
```

```
Vin3 A1 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin4 B1 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)
Vin5 A2 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin6 B2 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)
Vin7 A3 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin8 B3 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)
Vin9 C0 GND pulse (0 0 0 0.5p 0.5p 0.2u 0.4u)

Cap1 C1 GND 0.1p
Cap2 C2 GND 0.1p
Cap3 C3 GND 0.1p
Cap4 C4 GND 0.1p
Cap5 S0 GND 0.1p
Cap6 S1 GND 0.1p
Cap7 S2 GND 0.1p
Cap8 S3 GND 0.1p

.tran 1n 0.4u
.control
run

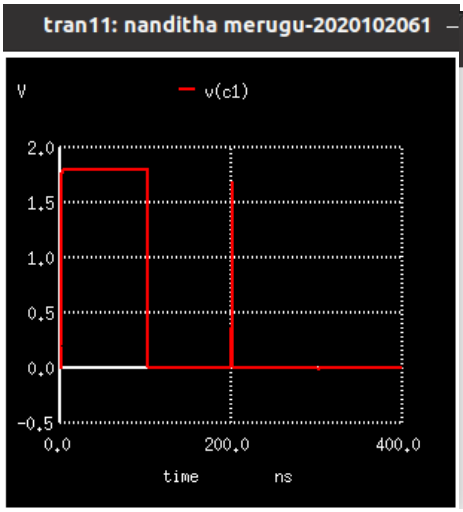
set curplottitle="Nanditha Merugu-2020102061"
plot v(C1)
set curplottitle="Nanditha Merugu-2020102061"
plot v(C2)
set curplottitle="Nanditha Merugu-2020102061"
plot v(C3)
set curplottitle="Nanditha Merugu-2020102061"
plot v(C4)
set curplottitle="Nanditha Merugu-2020102061"
plot v(S0)
set curplottitle="Nanditha Merugu-2020102061"
plot v(S1)
set curplottitle="Nanditha Merugu-2020102061"
plot v(S2)
set curplottitle="Nanditha Merugu-2020102061"
plot v(S3)
set curplottitle="Nanditha Merugu-2020102061"

.endc
.end
```

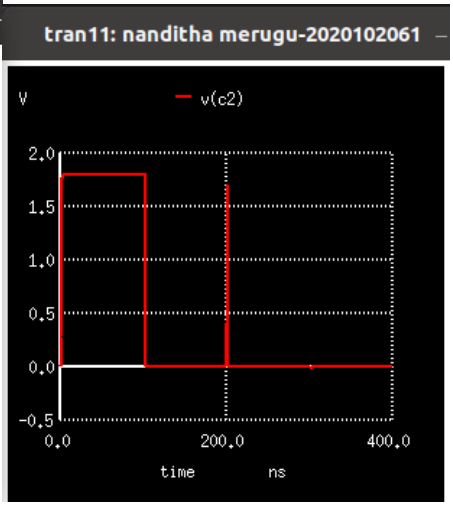
Plots:

(a) Carry Block:

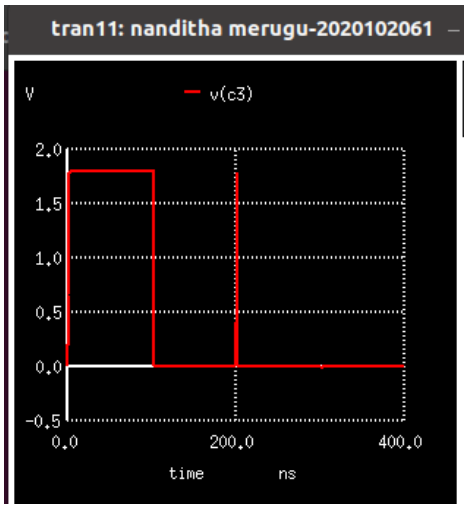
C1=G0 as C0=0



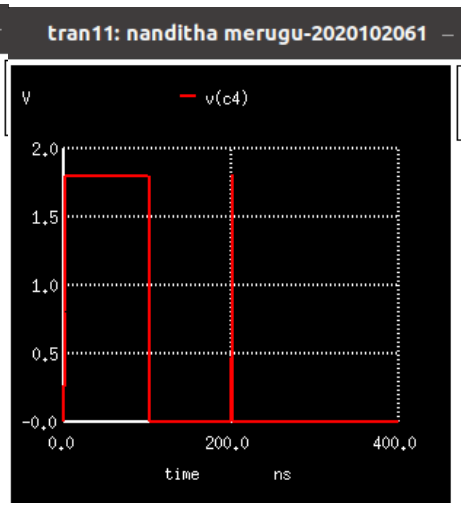
C2=G1+P1G0 as C0=0



C3=G2+P2G1+P2P1G0

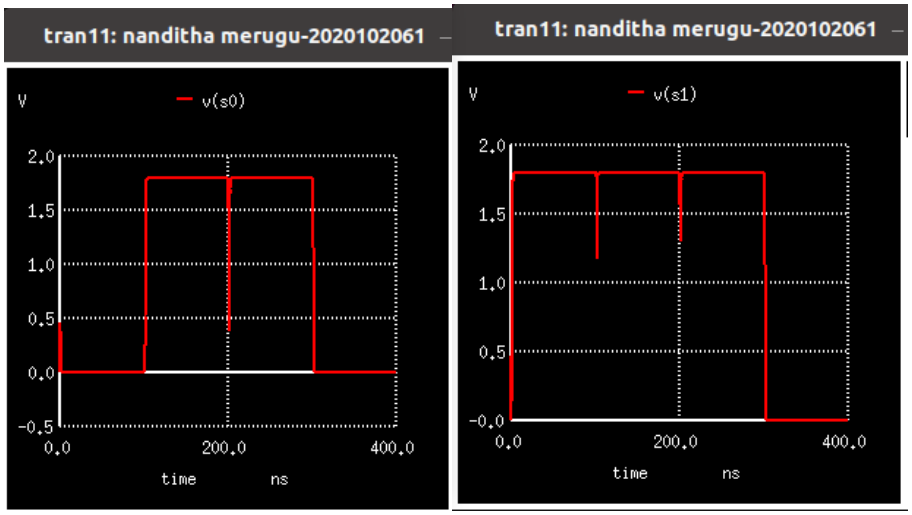


C4=G3+P3G2+P2P3G1+P3P2P1G0

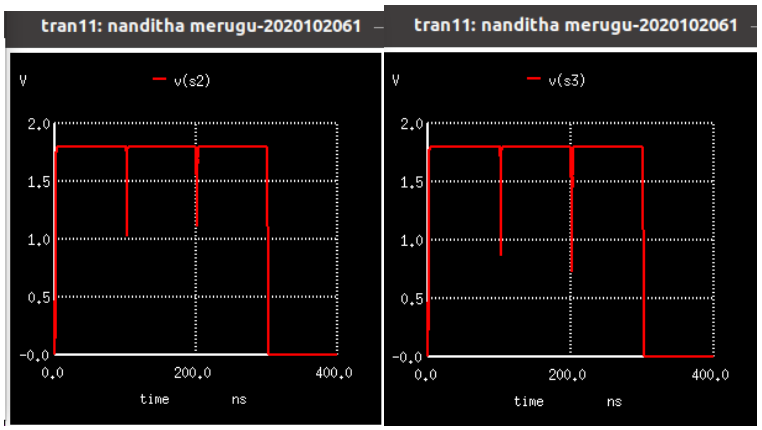


(b) Sum Block

S0=P0 XOR C0 S1=P1 XOR C1



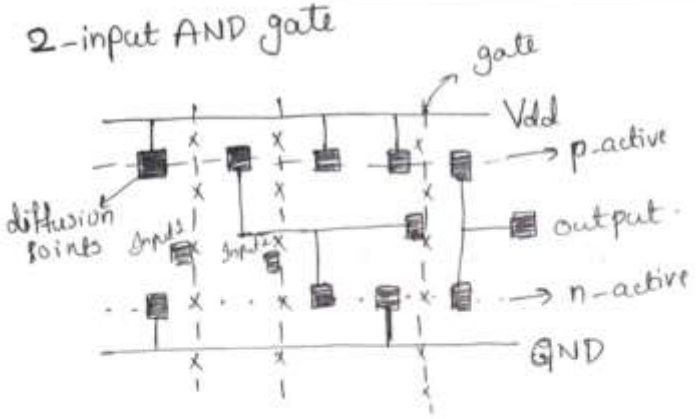
S2=P2 XOR C2 S3=P3 XOR C3



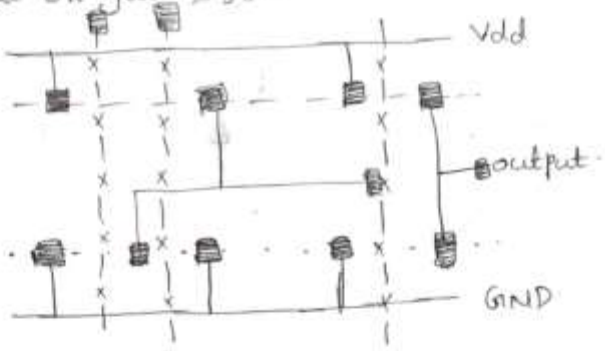
I also verified all the readings and plots of Carry and Sum using propagate and Generate signals. All the above plots are verified using truth table and they are correct.

Stick Diagrams:

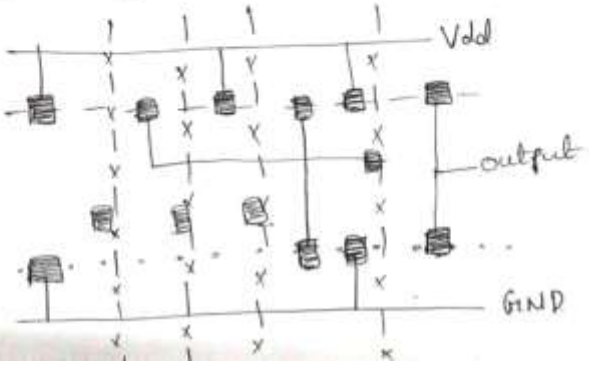
2-input AND gate



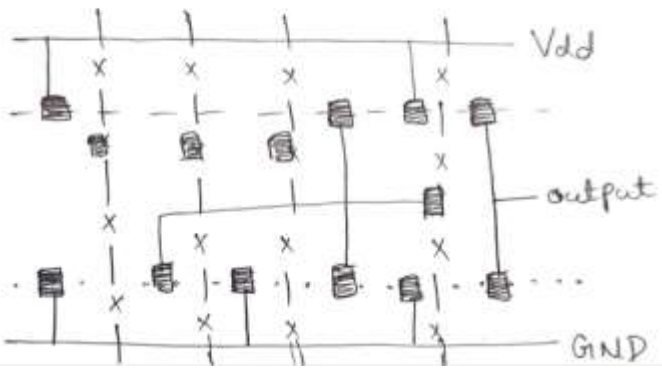
2-input OR gate → Inputs.



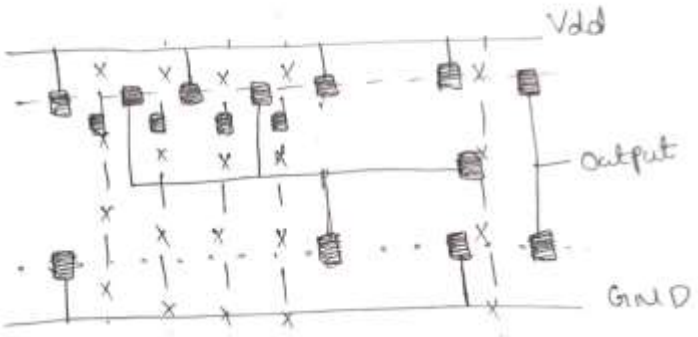
3-input AND gate



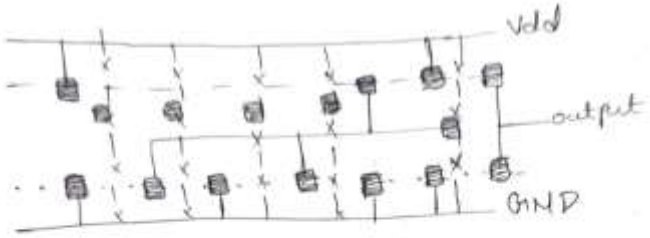
3-input OR gate:-



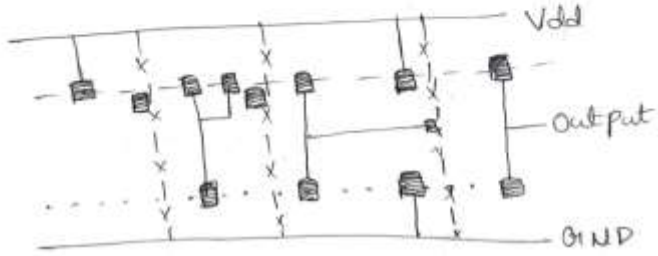
4-input AND gate



4-input OR gate-



XOR gate:-

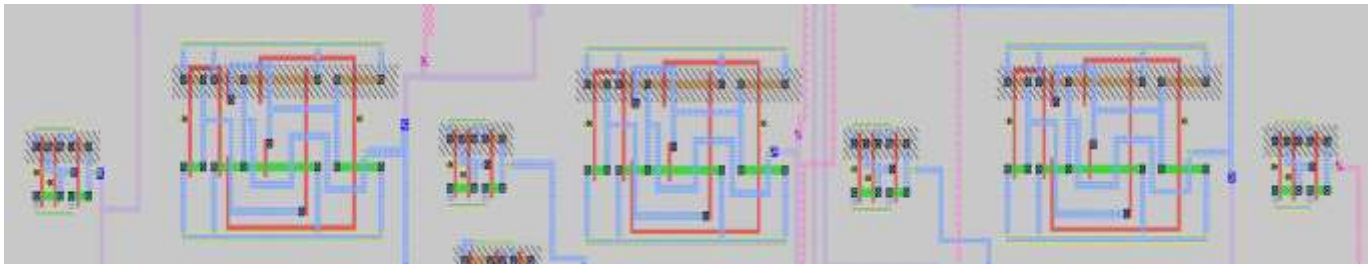


Layout of each block in Magic:

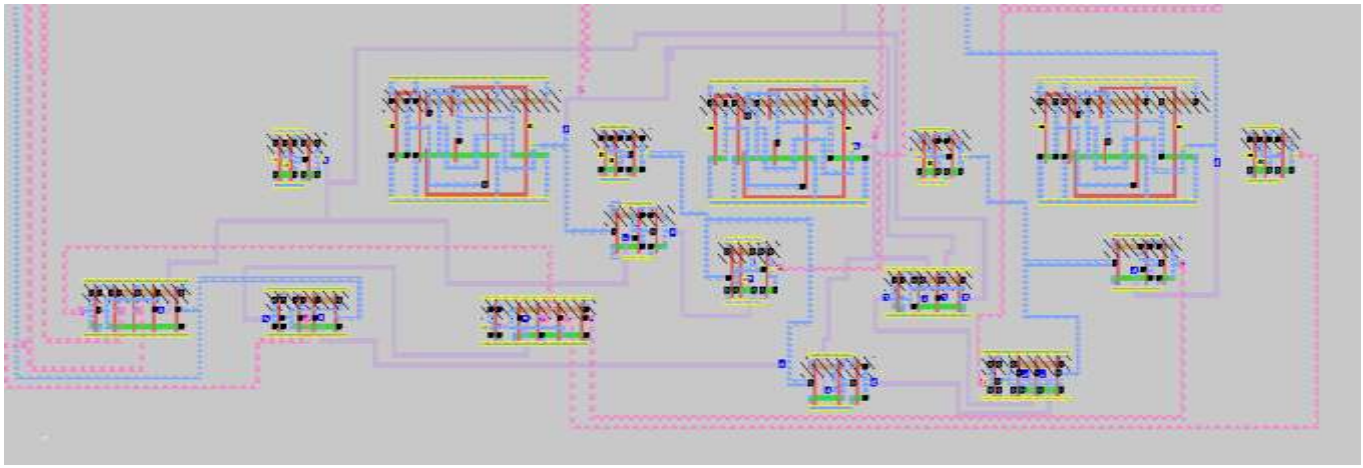
1. For Propagate and Generate:

For propagate, we use XOR gate. And for generate we use AND gate.

Below picture contains, G1 P2 G2 P3 G3

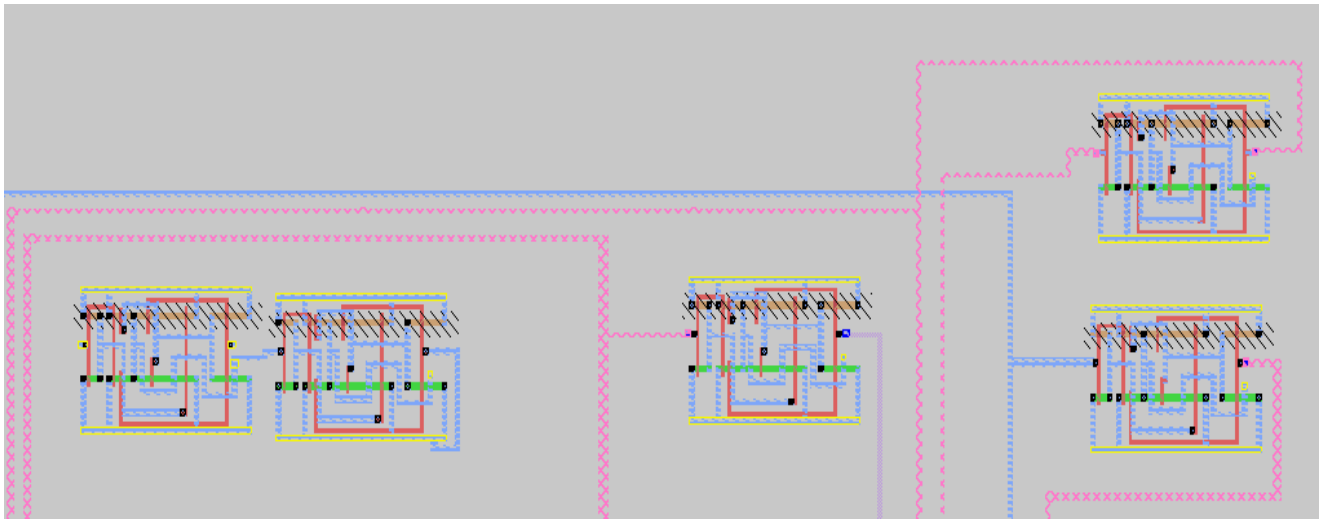


2. Carry



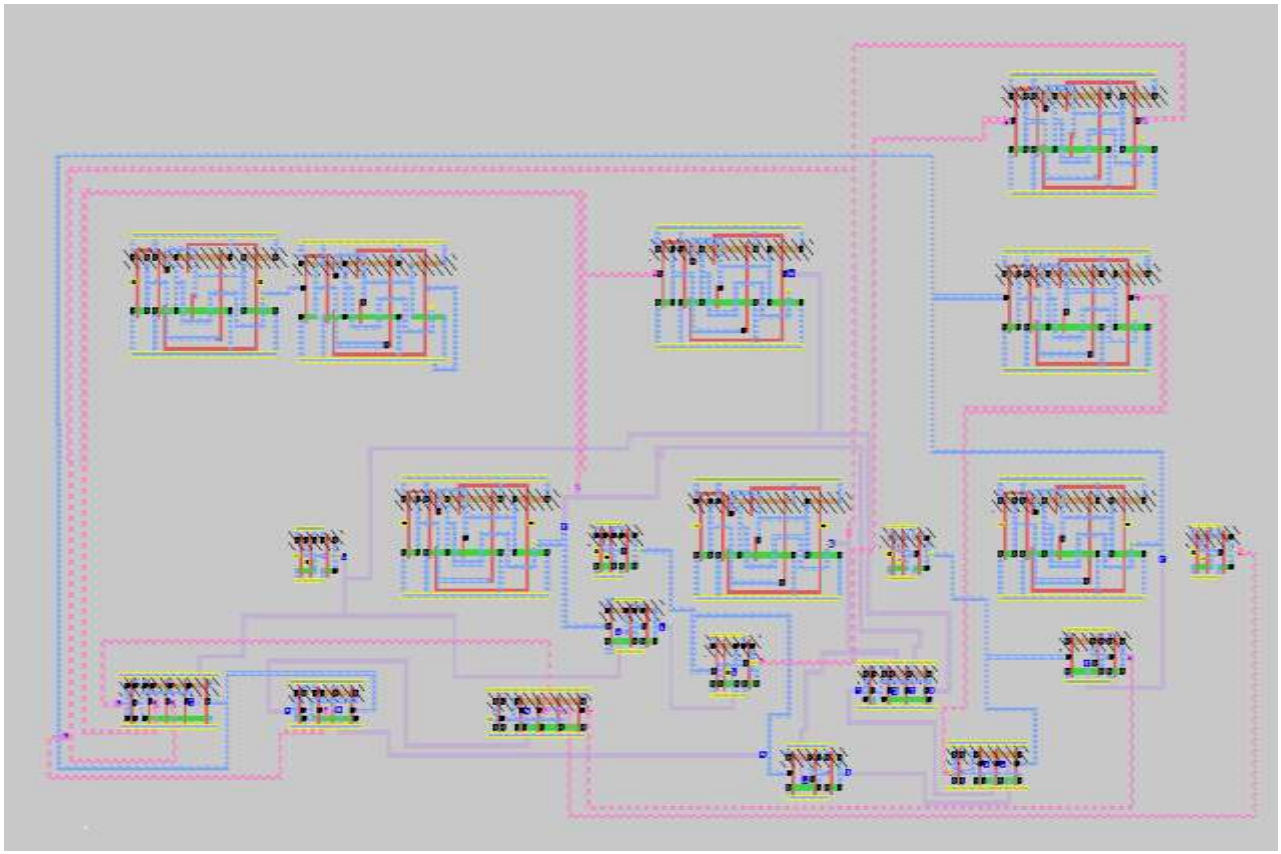
3. Sum

Below picture contains, P1 S1 S2 S3 S4



Post Layout:

The below is the post layout for the 4-bit Carry look ahead adder.



- Here, Inputs are: A4A3A2A1 and B4B3B2B1. Input Carry is C1. And we consider C1=0.
- Outputs:
- C2=G1
- C3= P2G1+G2
- C4= P3P2G1+P3G2+G3
- C5= P2P3P4G1+P3P4G2+P4G3+G4
- S1=P1 XOR C1
- S2=P2 XOR C2 as C1=0 then S2=P2 XOR G1
- S3=P3 XOR C3
- S4=P4 XOR C4
- We get Code that is generated from the post layout design and then we verify it using ngspice.
- We give the same input format as given in the netlist to verify the post layout with the pre-layout.

Code:

```
* SPICE3 file created from carry1.ext - technology: scmos
.include TSMC_180nm.txt
.param supply = 1.8
.option scale=0.09u
```

```
VSD VDD GND supply
M1000 a_956_557# C3 VDD w_942_594# CMOSP w=4 l=2
+  ad=44 pd=30 as=2268 ps=1686
M1001 a_978_601# C3 VDD w_942_594# CMOSP w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1002 S3 a_982_591# a_978_601# w_942_594# CMOSP w=4 l=2
+  ad=88 pd=52 as=0 ps=0
M1003 a_1008_601# P3 S3 w_942_594# CMOSP w=4 l=2
+  ad=128 pd=72 as=0 ps=0
M1004 VDD a_956_557# a_1008_601# w_942_594# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1005 VDD P3 a_982_591# w_942_594# CMOSP w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1006 a_956_557# C3 GND Gnd CMOSN w=4 l=2
+  ad=44 pd=30 as=2112 ps=1552
M1007 a_978_557# C3 GND Gnd CMOSN w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1008 S3 P3 a_978_557# Gnd CMOSN w=4 l=2
+  ad=104 pd=60 as=0 ps=0
M1009 a_1012_557# a_982_591# S3 Gnd CMOSN w=4 l=2
+  ad=112 pd=64 as=0 ps=0
M1010 GND a_956_557# a_1012_557# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1011 GND P3 a_982_591# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1012 a_594_431# P2 VDD w_580_468# CMOSP w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1013 a_616_475# P2 VDD w_580_468# CMOSP w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1014 S2 a_620_465# a_616_475# w_580_468# CMOSP w=4 l=2
+  ad=88 pd=52 as=0 ps=0
M1015 a_646_475# G1 S2 w_580_468# CMOSP w=4 l=2
+  ad=128 pd=72 as=0 ps=0
M1016 VDD a_594_431# a_646_475# w_580_468# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1017 VDD G1 a_620_465# w_580_468# CMOSP w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1018 a_55_424# A1 VDD w_41_461# CMOSP w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1019 a_77_468# A1 VDD w_41_461# CMOSP w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1020 a_83_424# a_81_458# a_77_468# w_41_461# CMOSP w=4 l=2
+  ad=88 pd=52 as=0 ps=0
M1021 a_107_468# B1 a_83_424# w_41_461# CMOSP w=4 l=2
+  ad=128 pd=72 as=0 ps=0
M1022 VDD a_55_424# a_107_468# w_41_461# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
```

```
M1023 VDD B1 a_81_458# w_41_461# CMOSP w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1024 a_228_419# a_83_424# VDD w_214_456# CMOSP w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1025 a_250_463# a_83_424# VDD w_214_456# CMOSP w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1026 S1 a_254_453# a_250_463# w_214_456# CMOSP w=4 l=2
+  ad=88 pd=52 as=0 ps=0
M1027 a_280_463# GND S1 w_214_456# CMOSP w=4 l=2
+  ad=128 pd=72 as=0 ps=0
M1028 VDD a_228_419# a_280_463# w_214_456# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1029 VDD GND a_254_453# w_214_456# CMOSP w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1030 a_55_424# A1 GND Gnd CMOSN w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1031 a_77_424# A1 GND Gnd CMOSN w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1032 a_83_424# B1 a_77_424# Gnd CMOSN w=4 l=2
+  ad=104 pd=60 as=0 ps=0
M1033 a_111_424# a_81_458# a_83_424# Gnd CMOSN w=4 l=2
+  ad=112 pd=64 as=0 ps=0
M1034 GND a_55_424# a_111_424# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1035 GND B1 a_81_458# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1036 a_949_411# P4 VDD w_935_448# CMOSP w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1037 a_971_455# P4 VDD w_935_448# CMOSP w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1038 S4 a_975_445# a_971_455# w_935_448# CMOSP w=4 l=2
+  ad=88 pd=52 as=0 ps=0
M1039 a_1001_455# C4 S4 w_935_448# CMOSP w=4 l=2
+  ad=128 pd=72 as=0 ps=0
M1040 VDD a_949_411# a_1001_455# w_935_448# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1041 VDD C4 a_975_445# w_935_448# CMOSP w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1042 a_594_431# P2 GND Gnd CMOSN w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1043 a_616_431# P2 GND Gnd CMOSN w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1044 S2 G1 a_616_431# Gnd CMOSN w=4 l=2
+  ad=104 pd=60 as=0 ps=0
M1045 a_650_431# a_620_465# S2 Gnd CMOSN w=4 l=2
+  ad=112 pd=64 as=0 ps=0
M1046 GND a_594_431# a_650_431# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
```

```
M1047 GND G1 a_620_465# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1048 a_228_419# a_83_424# GND Gnd CMOSN w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1049 a_250_419# a_83_424# GND Gnd CMOSN w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1050 S1 GND a_250_419# Gnd CMOSN w=4 l=2
+  ad=104 pd=60 as=0 ps=0
M1051 a_284_419# a_254_453# S1 Gnd CMOSN w=4 l=2
+  ad=112 pd=64 as=0 ps=0
M1052 GND a_228_419# a_284_419# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1053 GND GND a_254_453# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1054 a_949_411# P4 GND Gnd CMOSN w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1055 a_971_411# P4 GND Gnd CMOSN w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1056 S4 C4 a_971_411# Gnd CMOSN w=4 l=2
+  ad=104 pd=60 as=0 ps=0
M1057 a_1005_411# a_975_445# S4 Gnd CMOSN w=4 l=2
+  ad=112 pd=64 as=0 ps=0
M1058 GND a_949_411# a_1005_411# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1059 GND C4 a_975_445# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1060 a_333_225# A2 VDD w_319_262# CMOSP w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1061 a_355_269# A2 VDD w_319_262# CMOSP w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1062 P2 a_359_259# a_355_269# w_319_262# CMOSP w=4 l=2
+  ad=88 pd=52 as=0 ps=0
M1063 a_385_269# B2 P2 w_319_262# CMOSP w=4 l=2
+  ad=128 pd=72 as=0 ps=0
M1064 VDD a_333_225# a_385_269# w_319_262# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1065 VDD B2 a_359_259# w_319_262# CMOSP w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1066 a_223_235# A1 VDD w_210_229# CMOSP w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1067 VDD B1 a_223_235# w_210_229# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1068 G1 a_223_235# VDD w_210_229# CMOSP w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1069 a_633_223# A3 VDD w_619_260# CMOSP w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1070 a_655_267# A3 VDD w_619_260# CMOSP w=4 l=2
+  ad=16 pd=16 as=0 ps=0
```

```
M1071 P3 a_659_257# a_655_267# w_619_260# CMOSP w=4 l=2
+  ad=88 pd=52 as=0 ps=0
M1072 a_685_267# B3 P3 w_619_260# CMOSP w=4 l=2
+  ad=128 pd=72 as=0 ps=0
M1073 VDD a_633_223# a_685_267# w_619_260# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1074 VDD B3 a_659_257# w_619_260# CMOSP w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1075 a_945_224# A4 VDD w_931_261# CMOSP w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1076 a_967_268# A4 VDD w_931_261# CMOSP w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1077 P4 a_971_258# a_967_268# w_931_261# CMOSP w=4 l=2
+  ad=88 pd=52 as=0 ps=0
M1078 a_997_268# B4 P4 w_931_261# CMOSP w=4 l=2
+  ad=128 pd=72 as=0 ps=0
M1079 VDD a_945_224# a_997_268# w_931_261# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1080 VDD B4 a_971_258# w_931_261# CMOSP w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1081 a_530_239# A2 VDD w_517_233# CMOSP w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1082 VDD B2 a_530_239# w_517_233# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1083 G2 a_530_239# VDD w_517_233# CMOSP w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1084 a_333_225# A2 GND Gnd CMOSN w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1085 a_355_225# A2 GND Gnd CMOSN w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1086 P2 B2 a_355_225# Gnd CMOSN w=4 l=2
+  ad=104 pd=60 as=0 ps=0
M1087 a_389_225# a_359_259# P2 Gnd CMOSN w=4 l=2
+  ad=112 pd=64 as=0 ps=0
M1088 GND a_333_225# a_389_225# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1089 GND B2 a_359_259# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1090 a_223_210# A1 GND Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1091 a_223_235# B1 a_223_210# Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1092 G1 a_223_235# GND Gnd CMOSN w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1093 a_830_237# A3 VDD w_817_231# CMOSP w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1094 VDD B3 a_830_237# w_817_231# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
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M1095 G3 a_830_237# VDD w_817_231# CMOSP w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1096 a_633_223# A3 GND Gnd CMOSN w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1097 a_655_223# A3 GND Gnd CMOSN w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1098 P3 B3 a_655_223# Gnd CMOSN w=4 l=2
+  ad=104 pd=60 as=0 ps=0
M1099 a_689_223# a_659_257# P3 Gnd CMOSN w=4 l=2
+  ad=112 pd=64 as=0 ps=0
M1100 GND a_633_223# a_689_223# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1101 GND B3 a_659_257# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1102 a_530_214# A2 GND Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1103 a_530_239# B2 a_530_214# Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1104 G2 a_530_239# GND Gnd CMOSN w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1105 a_1142_238# A4 VDD w_1129_232# CMOSP w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1106 VDD B4 a_1142_238# w_1129_232# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1107 G4 a_1142_238# VDD w_1129_232# CMOSP w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1108 a_945_224# A4 GND Gnd CMOSN w=4 l=2
+  ad=44 pd=30 as=0 ps=0
M1109 a_967_224# A4 GND Gnd CMOSN w=4 l=2
+  ad=16 pd=16 as=0 ps=0
M1110 P4 B4 a_967_224# Gnd CMOSN w=4 l=2
+  ad=104 pd=60 as=0 ps=0
M1111 a_1001_224# a_971_258# P4 Gnd CMOSN w=4 l=2
+  ad=112 pd=64 as=0 ps=0
M1112 GND a_945_224# a_1001_224# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1113 GND B4 a_971_258# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=56 ps=36
M1114 a_830_212# A3 GND Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1115 a_830_237# B3 a_830_212# Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1116 G3 a_830_237# GND Gnd CMOSN w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1117 a_1142_213# A4 GND Gnd CMOSN w=4 l=2
+  ad=32 pd=24 as=0 ps=0
M1118 a_1142_238# B4 a_1142_213# Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
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M1119 G4 a_1142_238# GND Gnd CMOSN w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1120 a_541_177# P2 VDD w_528_171# CMOSP w=4 l=2
+  ad=72 pd=44 as=0 ps=0
M1121 VDD G1 a_541_177# w_528_171# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1122 B a_541_177# VDD w_528_171# CMOSP w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1123 a_541_152# P2 GND Gnd CMOSN w=4 l=2
+  ad=72 pd=44 as=0 ps=0
M1124 a_541_177# G1 a_541_152# Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1125 B a_541_177# GND Gnd CMOSN w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1126 a_1013_152# G3 VDD w_1000_146# CMOSP w=4 l=2
+  ad=100 pd=58 as=0 ps=0
M1127 VDD P4 a_1013_152# w_1000_146# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1128 a_506_78# a_1013_152# VDD w_1000_146# CMOSP w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1129 a_649_148# G2 VDD w_636_141# CMOSP w=4 l=2
+  ad=24 pd=20 as=0 ps=0
M1130 a_649_117# B a_649_148# w_636_141# CMOSP w=4 l=2
+  ad=52 pd=34 as=0 ps=0
M1131 C3 a_649_117# VDD w_636_141# CMOSP w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1132 VDD a_804_101# a_799_104# w_793_119# CMOSP w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1133 a_804_101# P3 VDD w_793_119# CMOSP w=4 l=2
+  ad=84 pd=58 as=0 ps=0
M1134 VDD P2 a_804_101# w_793_119# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1135 a_804_101# G1 VDD w_793_119# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1136 a_1013_127# G3 GND Gnd CMOSN w=4 l=2
+  ad=100 pd=58 as=0 ps=0
M1137 a_1013_152# P4 a_1013_127# Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1138 a_506_78# a_1013_152# GND Gnd CMOSN w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1139 VDD a_47_85# a_42_88# w_36_109# CMOSP w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1140 a_47_85# P2 VDD w_36_109# CMOSP w=4 l=2
+  ad=144 pd=88 as=0 ps=0
M1141 VDD P3 a_47_85# w_36_109# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1142 a_47_85# G1 VDD w_36_109# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
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M1143 VDD P4 a_47_85# w_36_109# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1144 a_649_117# G2 GND Gnd CMOSN w=4 l=2
+  ad=24 pd=20 as=0 ps=0
M1145 GND B a_649_117# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1146 C3 a_649_117# GND Gnd CMOSN w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1147 VDD a_220_85# a_215_88# w_209_103# CMOSP w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1148 a_220_85# P3 VDD w_209_103# CMOSP w=4 l=2
+  ad=68 pd=50 as=0 ps=0
M1149 VDD G2 a_220_85# w_209_103# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1150 a_220_85# P4 VDD w_209_103# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1151 VDD a_424_78# C5 w_413_96# CMOSP w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1152 a_448_102# a_215_88# a_424_78# w_413_96# CMOSP w=4 l=2
+  ad=64 pd=40 as=20 ps=18
M1153 a_466_102# a_42_88# a_448_102# w_413_96# CMOSP w=4 l=2
+  ad=72 pd=44 as=0 ps=0
M1154 a_486_102# G4 a_466_102# w_413_96# CMOSP w=4 l=2
+  ad=80 pd=48 as=0 ps=0
M1155 VDD a_506_78# a_486_102# w_413_96# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1156 GND a_804_101# a_799_104# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1157 a_825_104# P3 a_804_101# Gnd CMOSN w=4 l=2
+  ad=64 pd=40 as=20 ps=18
M1158 a_843_104# P2 a_825_104# Gnd CMOSN w=4 l=2
+  ad=72 pd=44 as=0 ps=0
M1159 GND G1 a_843_104# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1160 GND a_47_85# a_42_88# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1161 a_67_88# P2 a_47_85# Gnd CMOSN w=4 l=2
+  ad=64 pd=40 as=20 ps=18
M1162 a_85_88# P3 a_67_88# Gnd CMOSN w=4 l=2
+  ad=68 pd=42 as=0 ps=0
M1163 a_104_88# G1 a_85_88# Gnd CMOSN w=4 l=2
+  ad=80 pd=48 as=0 ps=0
M1164 GND P4 a_104_88# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1165 GND a_220_85# a_215_88# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1166 a_241_88# P3 a_220_85# Gnd CMOSN w=4 l=2
+  ad=48 pd=32 as=20 ps=18
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M1167 a_255_88# G2 a_241_88# Gnd CMOSN w=4 l=2
+  ad=72 pd=44 as=0 ps=0
M1168 GND P4 a_255_88# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1169 GND a_424_78# C5 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1170 a_424_78# a_215_88# GND Gnd CMOSN w=4 l=2
+  ad=144 pd=88 as=0 ps=0
M1171 GND a_42_88# a_424_78# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1172 a_424_78# G4 GND Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1173 GND a_506_78# a_424_78# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1174 a_727_56# G2 VDD w_714_50# CMOSP w=4 l=2
+  ad=84 pd=50 as=0 ps=0
M1175 VDD P3 a_727_56# w_714_50# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1176 a_767_31# a_727_56# VDD w_714_50# CMOSP w=4 l=2
+  ad=36 pd=26 as=0 ps=0
M1177 VDD a_895_34# C4 w_884_52# CMOSP w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1178 a_919_58# a_799_104# a_895_34# w_884_52# CMOSP w=4 l=2
+  ad=60 pd=38 as=20 ps=18
M1179 a_936_58# a_767_31# a_919_58# w_884_52# CMOSP w=4 l=2
+  ad=72 pd=44 as=0 ps=0
M1180 VDD G3 a_936_58# w_884_52# CMOSP w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1181 GND a_895_34# C4 Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1182 a_895_34# a_799_104# GND Gnd CMOSN w=4 l=2
+  ad=80 pd=56 as=0 ps=0
M1183 GND a_767_31# a_895_34# Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1184 a_895_34# G3 GND Gnd CMOSN w=4 l=2
+  ad=0 pd=0 as=0 ps=0
M1185 a_727_31# G2 GND Gnd CMOSN w=4 l=2
+  ad=84 pd=50 as=0 ps=0
M1186 a_727_56# P3 a_727_31# Gnd CMOSN w=4 l=2
+  ad=20 pd=18 as=0 ps=0
M1187 a_767_31# a_727_56# GND Gnd CMOSN w=4 l=2
+  ad=36 pd=26 as=0 ps=0
C0 a_982_591# a_956_557# 0.08fF
C1 P3 S3 0.06fF
C2 a_659_257# A3 0.07fF
C3 a_830_237# VDD 0.09fF
C4 w_214_456# VDD 0.10fF
C5 P4 a_949_411# 0.06fF
```

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C6 w_517_233# B2 0.06fF
C7 w_793_119# P3 0.16fF
C8 G1 a_47_85# 0.16fF
C9 GND a_895_34# 0.34fF
C10 GND a_799_104# 0.18fF
C11 w_209_103# VDD 0.14fF
C12 a_359_259# A2 0.07fF
C13 VDD a_424_78# 0.07fF
C14 P3 a_47_85# 0.18fF
C15 S4 a_1005_411# 0.02fF
C16 a_895_34# a_767_31# 0.25fF
C17 C4 G3 0.04fF
C18 S4 GND 0.22fF
C19 w_931_261# a_945_224# 0.11fF
C20 VDD a_804_101# 0.21fF
C21 a_767_31# a_799_104# 0.22fF
C22 w_817_231# G3 0.03fF
C23 w_931_261# B4 0.17fF
C24 a_81_458# B1 0.08fF
C25 a_55_424# A1 0.06fF
C26 G1 w_210_229# 0.03fF
C27 a_83_424# w_214_456# 0.27fF
C28 VDD a_1013_152# 0.06fF
C29 A2 VDD 0.08fF
C30 G2 a_255_88# 0.00fF
C31 w_528_171# a_541_177# 0.09fF
C32 P2 a_594_431# 0.06fF
C33 G4 a_424_78# 0.15fF
C34 P4 w_209_103# 0.06fF
C35 G2 a_506_78# 0.05fF
C36 a_633_223# GND 0.04fF
C37 a_81_458# w_41_461# 0.22fF
C38 C4 a_895_34# 0.05fF
C39 w_517_233# VDD 0.10fF
C40 w_884_52# G3 0.09fF
C41 a_659_257# VDD 0.19fF
C42 P2 w_793_119# 0.16fF
C43 P4 a_1013_152# 0.20fF
C44 a_633_223# A3 0.06fF
C45 G3 VDD 0.07fF
C46 w_580_468# VDD 0.10fF
C47 C4 S4 0.06fF
C48 a_975_445# a_949_411# 0.08fF
C49 B3 a_830_237# 0.20fF
C50 w_209_103# P3 0.06fF
C51 a_971_258# a_997_268# 0.02fF
C52 P2 a_47_85# 0.22fF
C53 G1 a_804_101# 0.14fF
```

```
C54 GND a_767_31# 0.09fF
C55 P2 a_389_225# 0.02fF
C56 w_413_96# VDD 0.15fF
C57 w_884_52# a_895_34# 0.10fF
C58 w_714_50# a_767_31# 0.03fF
C59 S4 w_935_448# 0.03fF
C60 a_333_225# A2 0.06fF
C61 w_884_52# a_799_104# 0.16fF
C62 P3 a_804_101# 0.27fF
C63 A1 B1 0.06fF
C64 a_254_453# S1 0.44fF
C65 B2 GND 0.08fF
C66 a_895_34# VDD 0.07fF
C67 VDD a_799_104# 0.07fF
C68 w_1000_146# a_506_78# 0.03fF
C69 a_55_424# B1 0.40fF
C70 G2 a_220_85# 0.18fF
C71 a_223_235# GND 0.07fF
C72 w_41_461# A1 0.27fF
C73 C4 GND 0.17fF
C74 w_413_96# G4 0.14fF
C75 w_528_171# B 0.03fF
C76 G1 S2 0.06fF
C77 G1 w_580_468# 0.17fF
C78 a_55_424# w_41_461# 0.11fF
C79 P3 a_659_257# 0.44fF
C80 A2 a_530_239# 0.02fF
C81 w_942_594# S3 0.03fF
C82 a_633_223# VDD 0.04fF
C83 w_817_231# A3 0.06fF
C84 a_982_591# S3 0.44fF
C85 a_659_257# B3 0.08fF
C86 w_517_233# a_530_239# 0.09fF
C87 P2 a_804_101# 0.25fF
C88 GND VDD 0.08fF
C89 w_319_262# A2 0.27fF
C90 w_714_50# VDD 0.11fF
C91 w_884_52# a_767_31# 0.16fF
C92 a_359_259# B2 0.08fF
C93 w_36_109# a_42_88# 0.03fF
C94 a_83_424# a_111_424# 0.02fF
C95 a_254_453# a_280_463# 0.02fF
C96 a_228_419# S1 0.27fF
C97 C4 w_935_448# 0.17fF
C98 A3 VDD 0.08fF
C99 GND G4 0.06fF
C100 G2 a_215_88# 0.27fF
C101 w_41_461# B1 0.17fF
```

```
C102 a_254_453# w_214_456# 0.22fF
C103 P4 GND 0.42fF
C104 w_636_141# B 0.07fF
C105 B2 VDD 0.08fF
C106 C4 w_884_52# 0.03fF
C107 a_83_424# GND 0.26fF
C108 P2 w_580_468# 0.27fF
C109 a_223_235# VDD 0.09fF
C110 C4 VDD 0.15fF
C111 B a_649_117# 0.25fF
C112 G2 B 0.13fF
C113 P3 a_633_223# 0.27fF
C114 P4 a_1013_127# 0.00fF
C115 a_333_225# GND 0.04fF
C116 G1 GND 0.25fF
C117 w_817_231# VDD 0.10fF
C118 a_982_591# a_1008_601# 0.02fF
C119 a_956_557# S3 0.27fF
C120 a_633_223# B3 0.40fF
C121 w_935_448# VDD 0.10fF
C122 P3 GND 0.46fF
C123 a_975_445# S4 0.44fF
C124 a_359_259# VDD 0.19fF
C125 w_714_50# P3 0.20fF
C126 C4 P4 0.07fF
C127 B3 GND 0.08fF
C128 P2 a_67_88# 0.00fF
C129 w_884_52# VDD 0.13fF
C130 a_333_225# B2 0.40fF
C131 a_659_257# a_685_267# 0.02fF
C132 a_530_239# GND 0.07fF
C133 P3 a_85_88# 0.00fF
C134 w_210_229# A1 0.06fF
C135 P4 w_935_448# 0.27fF
C136 G1 a_223_235# 0.02fF
C137 w_209_103# G2 0.06fF
C138 a_47_85# a_42_88# 0.05fF
C139 A3 B3 0.06fF
C140 a_228_419# w_214_456# 0.11fF
C141 S1 a_284_419# 0.02fF
C142 a_620_465# a_594_431# 0.08fF
C143 a_359_259# a_333_225# 0.08fF
C144 P4 VDD 0.87fF
C145 B2 a_530_239# 0.20fF
C146 P2 GND 0.36fF
C147 P3 a_689_223# 0.02fF
C148 w_817_231# B3 0.06fF
C149 a_83_424# VDD 0.08fF
```

```
C150 a_975_445# a_1001_455# 0.02fF
C151 w_517_233# G2 0.03fF
C152 a_333_225# VDD 0.04fF
C153 G1 VDD 0.14fF
C154 C4 a_975_445# 0.08fF
C155 w_319_262# B2 0.17fF
C156 P3 VDD 0.20fF
C157 P2 B2 0.06fF
C158 a_42_88# a_424_78# 0.18fF
C159 a_220_85# a_215_88# 0.05fF
C160 w_210_229# B1 0.06fF
C161 a_975_445# w_935_448# 0.22fF
C162 B3 VDD 0.08fF
C163 w_36_109# a_47_85# 0.18fF
C164 w_619_260# a_659_257# 0.22fF
C165 a_530_239# VDD 0.09fF
C166 w_1000_146# a_1013_152# 0.09fF
C167 P4 P3 0.15fF
C168 a_945_224# GND 0.04fF
C169 a_254_453# GND 0.08fF
C170 w_319_262# a_359_259# 0.22fF
C171 GND B4 0.08fF
C172 P2 a_359_259# 0.44fF
C173 a_975_445# VDD 0.19fF
C174 a_1013_152# a_506_78# 0.02fF
C175 w_1129_232# VDD 0.10fF
C176 a_971_258# VDD 0.19fF
C177 a_541_177# B 0.02fF
C178 G1 P3 0.05fF
C179 A4 VDD 0.08fF
C180 w_319_262# VDD 0.10fF
C181 w_1000_146# G3 0.06fF
C182 P2 VDD 0.14fF
C183 P4 a_975_445# 0.07fF
C184 w_1129_232# G4 0.03fF
C185 C3 VDD 0.11fF
C186 w_209_103# a_220_85# 0.18fF
C187 w_413_96# a_42_88# 0.14fF
C188 P3 B3 0.06fF
C189 P4 a_971_258# 0.44fF
C190 GND a_649_117# 0.07fF
C191 G2 GND 0.12fF
C192 w_528_171# VDD 0.11fF
C193 P3 a_241_88# 0.00fF
C194 w_413_96# a_506_78# 0.15fF
C195 w_714_50# G2 0.06fF
C196 w_619_260# a_633_223# 0.11fF
C197 S1 w_214_456# 0.03fF
```

```
C198 a_620_465# S2 0.44fF
C199 P4 C3 0.04fF
C200 w_319_262# a_333_225# 0.11fF
C201 a_228_419# GND 0.44fF
C202 a_620_465# w_580_468# 0.22fF
C203 GND a_1142_238# 0.07fF
C204 G1 P2 0.43fF
C205 P2 a_333_225# 0.27fF
C206 a_55_424# GND 0.04fF
C207 a_945_224# VDD 0.04fF
C208 a_254_453# VDD 0.19fF
C209 G1 C3 0.05fF
C210 P2 P3 0.05fF
C211 B4 VDD 0.08fF
C212 a_956_557# GND 0.04fF
C213 w_619_260# A3 0.27fF
C214 a_81_458# VDD 0.19fF
C215 G1 w_528_171# 0.06fF
C216 P3 C3 0.15fF
C217 P4 a_1001_224# 0.02fF
C218 w_942_594# VDD 0.10fF
C219 GND a_42_88# 0.12fF
C220 a_982_591# VDD 0.19fF
C221 G1 a_541_152# 0.01fF
C222 A1 a_223_235# 0.02fF
C223 w_209_103# a_215_88# 0.03fF
C224 P4 a_945_224# 0.27fF
C225 a_215_88# a_424_78# 0.35fF
C226 GND a_506_78# 0.02fF
C227 w_636_141# VDD 0.08fF
C228 P4 B4 0.06fF
C229 w_793_119# a_804_101# 0.19fF
C230 w_1129_232# A4 0.06fF
C231 a_83_424# a_254_453# 0.07fF
C232 a_971_258# A4 0.07fF
C233 VDD a_649_117# 0.07fF
C234 a_620_465# a_646_475# 0.02fF
C235 a_81_458# a_83_424# 0.44fF
C236 a_594_431# S2 0.27fF
C237 B1 GND 0.08fF
C238 a_594_431# w_580_468# 0.11fF
C239 P2 w_319_262# 0.03fF
C240 C5 a_424_78# 0.05fF
C241 a_228_419# VDD 0.04fF
C242 A1 VDD 0.08fF
C243 G2 G4 0.05fF
C244 P2 C3 0.05fF
C245 a_1142_238# VDD 0.09fF
```

```
C246 w_619_260# VDD 0.10fF
C247 w_942_594# P3 0.17fF
C248 a_55_424# VDD 0.04fF
C249 P2 w_528_171# 0.06fF
C250 P3 a_982_591# 0.08fF
C251 GND a_220_85# 0.22fF
C252 a_956_557# VDD 0.04fF
C253 B1 a_223_235# 0.20fF
C254 GND a_727_56# 0.07fF
C255 w_413_96# a_215_88# 0.14fF
C256 a_1142_238# G4 0.02fF
C257 w_1000_146# VDD 0.12fF
C258 w_714_50# a_727_56# 0.09fF
C259 VDD a_42_88# 0.11fF
C260 w_793_119# a_799_104# 0.03fF
C261 P3 G2 0.04fF
C262 a_971_258# a_945_224# 0.08fF
C263 a_83_424# a_228_419# 0.06fF
C264 w_1129_232# B4 0.06fF
C265 GND a_541_177# 0.07fF
C266 a_727_56# a_767_31# 0.02fF
C267 a_971_258# B4 0.08fF
C268 a_945_224# A4 0.06fF
C269 VDD a_506_78# 0.05fF
C270 A4 B4 0.06fF
C271 a_81_458# a_107_468# 0.02fF
C272 a_55_424# a_83_424# 0.27fF
C273 w_413_96# C5 0.03fF
C274 S1 GND 0.28fF
C275 a_466_102# a_42_88# 0.00fF
C276 a_830_237# G3 0.02fF
C277 a_359_259# a_385_269# 0.02fF
C278 P4 w_1000_146# 0.06fF
C279 a_530_239# G2 0.02fF
C280 a_594_431# GND 0.04fF
C281 w_619_260# P3 0.03fF
C282 B1 VDD 0.08fF
C283 G4 a_506_78# 1.34fF
C284 P4 a_506_78# 0.05fF
C285 w_931_261# VDD 0.10fF
C286 S3 GND 0.22fF
C287 w_942_594# C3 0.27fF
C288 a_949_411# S4 0.27fF
C289 w_619_260# B3 0.17fF
C290 a_620_465# VDD 0.19fF
C291 P3 a_956_557# 0.40fF
C292 C3 a_982_591# 0.07fF
C293 G1 a_42_88# 0.16fF
```

```
C294 w_41_461# VDD 0.10fF
C295 GND a_215_88# 0.18fF
C296 w_517_233# A2 0.06fF
C297 w_636_141# C3 0.03fF
C298 w_413_96# a_424_78# 0.10fF
C299 GND a_47_85# 0.18fF
C300 w_36_109# VDD 0.19fF
C301 P4 w_931_261# 0.03fF
C302 VDD a_220_85# 0.21fF
C303 C3 a_649_117# 0.05fF
C304 C3 G2 0.04fF
C305 a_83_424# B1 0.08fF
C306 w_1129_232# a_1142_238# 0.09fF
C307 GND B 0.08fF
C308 a_727_56# VDD 0.06fF
C309 a_945_224# B4 0.40fF
C310 a_949_411# GND 0.04fF
C311 GND C5 0.10fF
C312 A4 a_1142_238# 0.02fF
C313 a_804_101# a_799_104# 0.05fF
C314 S2 w_580_468# 0.03fF
C315 a_83_424# w_41_461# 0.03fF
C316 VDD a_541_177# 0.06fF
C317 G1 a_620_465# 0.08fF
C318 P4 w_36_109# 0.06fF
C319 P4 a_220_85# 0.13fF
C320 GND a_830_237# 0.07fF
C321 w_214_456# GND 0.17fF
C322 a_1012_557# S3 0.02fF
C323 w_942_594# a_982_591# 0.22fF
C324 a_594_431# VDD 0.04fF
C325 G1 w_36_109# 0.20fF
C326 C3 a_956_557# 0.06fF
C327 G3 a_895_34# 0.14fF
C328 C4 a_949_411# 0.40fF
C329 GND a_424_78# 0.34fF
C330 A3 a_830_237# 0.02fF
C331 w_36_109# P3 0.06fF
C332 P3 a_220_85# 0.22fF
C333 GND a_804_101# 0.22fF
C334 w_210_229# a_223_235# 0.09fF
C335 w_793_119# VDD 0.15fF
C336 P3 a_727_56# 0.21fF
C337 a_949_411# w_935_448# 0.11fF
C338 VDD a_215_88# 0.07fF
C339 G1 a_541_177# 0.20fF
C340 a_254_453# a_228_419# 0.08fF
C341 GND a_1013_152# 0.07fF
```

```
C342 w_931_261# a_971_258# 0.22fF
C343 VDD a_47_85# 0.21fF
C344 a_895_34# a_799_104# 0.28fF
C345 w_636_141# a_649_117# 0.10fF
C346 w_636_141# G2 0.07fF
C347 a_659_257# a_633_223# 0.08fF
C348 w_817_231# a_830_237# 0.09fF
C349 a_81_458# A1 0.07fF
C350 w_931_261# A4 0.27fF
C351 B4 a_1142_238# 0.20fF
C352 a_81_458# a_55_424# 0.08fF
C353 G1 a_594_431# 0.40fF
C354 a_949_411# VDD 0.04fF
C355 P2 a_620_465# 0.07fF
C356 G2 a_649_117# 0.05fF
C357 C5 VDD 0.07fF
C358 P4 a_215_88# 0.06fF
C359 S2 GND 0.22fF
C360 S2 a_650_431# 0.02fF
C361 GND G3 0.02fF
C362 A2 B2 0.06fF
C363 w_210_229# VDD 0.10fF
C364 w_942_594# a_956_557# 0.11fF
C365 G1 w_793_119# 0.06fF
C366 P2 w_36_109# 0.06fF
C367 GND Gnd 9.77fF
C368 VDD Gnd 3.84fF
C369 a_767_31# Gnd 1.11fF
C370 a_895_34# Gnd 0.33fF
C371 a_727_56# Gnd 0.11fF
C372 C5 Gnd 0.06fF
C373 a_424_78# Gnd 0.21fF
C374 a_215_88# Gnd 4.73fF
C375 a_220_85# Gnd 0.24fF
C376 a_42_88# Gnd 0.78fF
C377 a_799_104# Gnd 3.06fF
C378 a_804_101# Gnd 0.24fF
C379 a_47_85# Gnd 0.29fF
C380 a_506_78# Gnd 0.92fF
C381 a_649_117# Gnd 0.06fF
C382 a_1013_152# Gnd 0.25fF
C383 B Gnd 0.87fF
C384 a_541_177# Gnd 0.04fF
C385 G4 Gnd 1.12fF
C386 a_1142_238# Gnd 0.09fF
C387 B4 Gnd 1.80fF
C388 A4 Gnd 0.32fF
C389 G3 Gnd 1.44fF
```

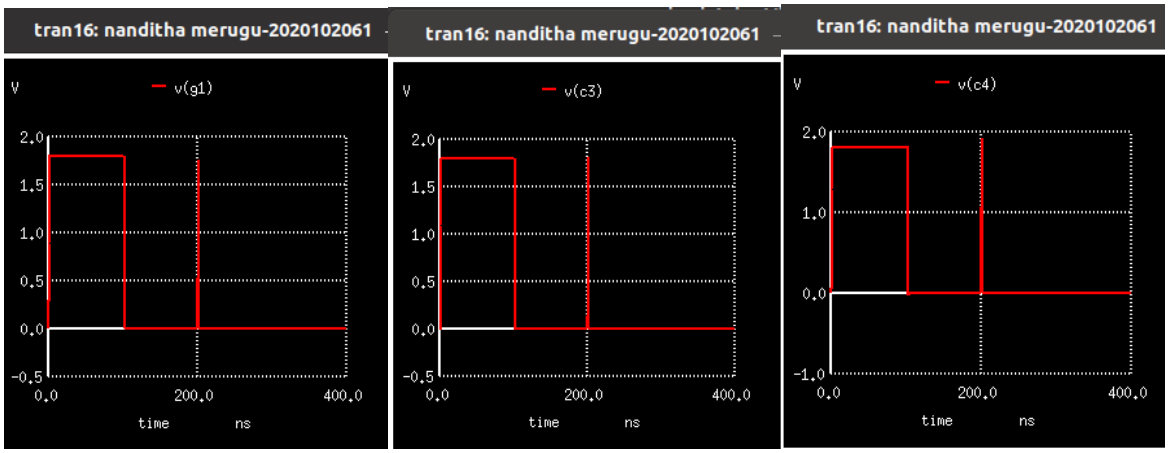
```
C390 a_830_237# Gnd 0.12fF
C391 B3 Gnd 1.75fF
C392 A3 Gnd 0.57fF
C393 G2 Gnd 7.11fF
C394 a_530_239# Gnd 0.13fF
C395 B2 Gnd 1.80fF
C396 A2 Gnd 0.67fF
C397 a_223_235# Gnd 0.19fF
C398 B1 Gnd 1.75fF
C399 A1 Gnd 0.26fF
C400 a_945_224# Gnd 0.13fF
C401 a_971_258# Gnd 0.54fF
C402 a_633_223# Gnd 0.80fF
C403 a_333_225# Gnd 0.19fF
C404 S4 Gnd 0.68fF
C405 a_949_411# Gnd 0.80fF
C406 a_975_445# Gnd 0.54fF
C407 P4 Gnd 11.39fF
C408 C4 Gnd 0.22fF
C409 S1 Gnd 0.68fF
C410 a_228_419# Gnd 0.80fF
C411 a_83_424# Gnd 1.30fF
C412 S2 Gnd 0.68fF
C413 a_594_431# Gnd 0.80fF
C414 a_620_465# Gnd 0.54fF
C415 a_55_424# Gnd 0.80fF
C416 a_81_458# Gnd 0.54fF
C417 P2 Gnd 10.55fF
C418 G1 Gnd 21.47fF
C419 S3 Gnd 0.68fF
C420 a_956_557# Gnd 0.80fF
C421 a_982_591# Gnd 0.54fF
C422 C3 Gnd 0.26fF
C423 P3 Gnd 9.19fF
C424 w_884_52# Gnd 1.25fF
C425 w_714_50# Gnd 0.77fF
C426 w_413_96# Gnd 1.70fF
C427 w_209_103# Gnd 1.24fF
C428 w_793_119# Gnd 1.30fF
C429 w_36_109# Gnd 1.62fF
C430 w_1000_146# Gnd 1.00fF
C431 w_636_141# Gnd 0.44fF
C432 w_528_171# Gnd 0.55fF
C433 w_1129_232# Gnd 0.53fF
C434 w_817_231# Gnd 0.58fF
C435 w_517_233# Gnd 0.58fF
C436 w_210_229# Gnd 0.88fF
C437 w_931_261# Gnd 0.53fF
```

```
C438 w_619_260# Gnd 0.73fF
C439 w_319_262# Gnd 0.73fF
C440 w_935_448# Gnd 2.85fF
C441 w_580_468# Gnd 2.85fF
C442 w_214_456# Gnd 0.82fF
C443 w_41_461# Gnd 2.83fF
C444 w_942_594# Gnd 2.85fF


C446 S2 GND 0.1p
C447 S3 GND 0.1p
C448 S4 GND 0.1p
C449 C5 GND 0.1p

Vin1 A1 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin2 B1 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)
Vin3 A2 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin4 B2 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)
Vin5 A3 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin6 B3 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)
Vin7 A4 GND pulse(0 supply 0 1n 1n 0.1u 0.2u)
Vin8 B4 GND pulse(0 supply 0 1n 1n 0.2u 0.4u)

.tran 1n 0.4u
.control
run

set curplottitle="Nanditha Merugu-2020102061"
plot v(G1)
set curplottitle="Nanditha Merugu-2020102061"
plot v(C2)
set curplottitle="Nanditha Merugu-2020102061"
plot v(S1)
set curplottitle="Nanditha Merugu-2020102061"
plot v(S2)
set curplottitle="Nanditha Merugu-2020102061"
plot v(C3)
set curplottitle="Nanditha Merugu-2020102061"
plot v(S3)
set curplottitle="Nanditha Merugu-2020102061"
plot v(C4)
set curplottitle="Nanditha Merugu-2020102061"
plot v(S4)
set curplottitle="Nanditha Merugu-2020102061"
plot v(C5)
set curplottitle="Nanditha Merugu-2020102061"

.endc
.end
```

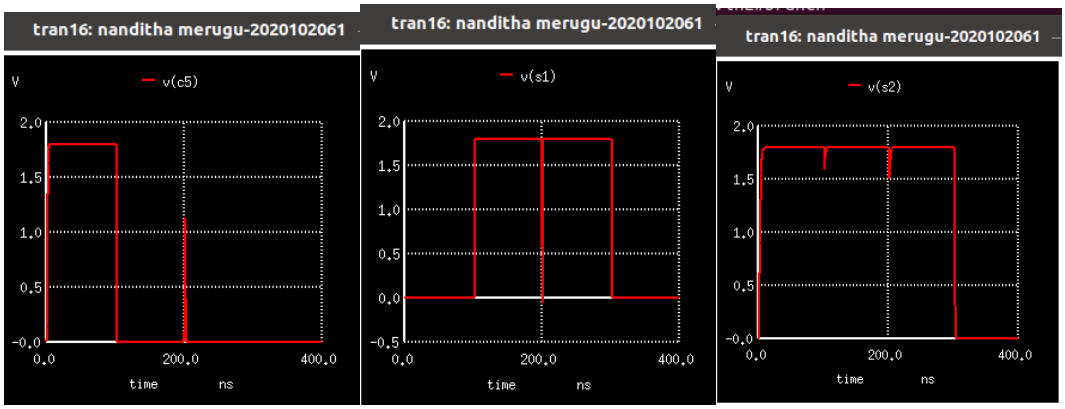
Results:

I considered C1=0;

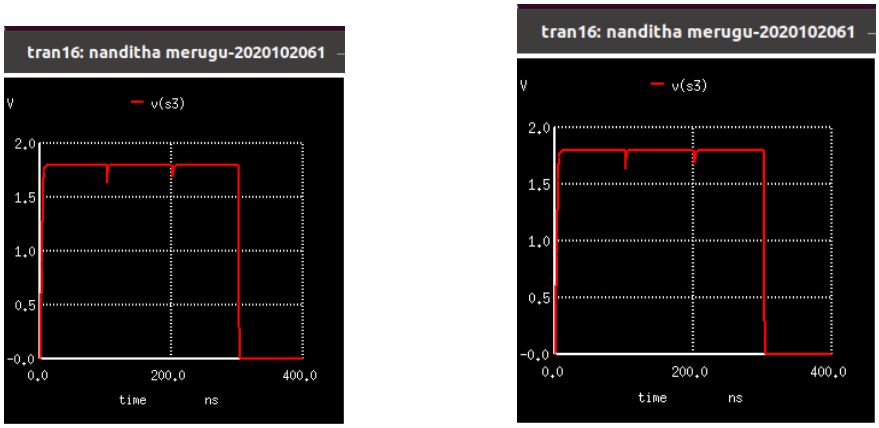
C2=G1 C3 C4



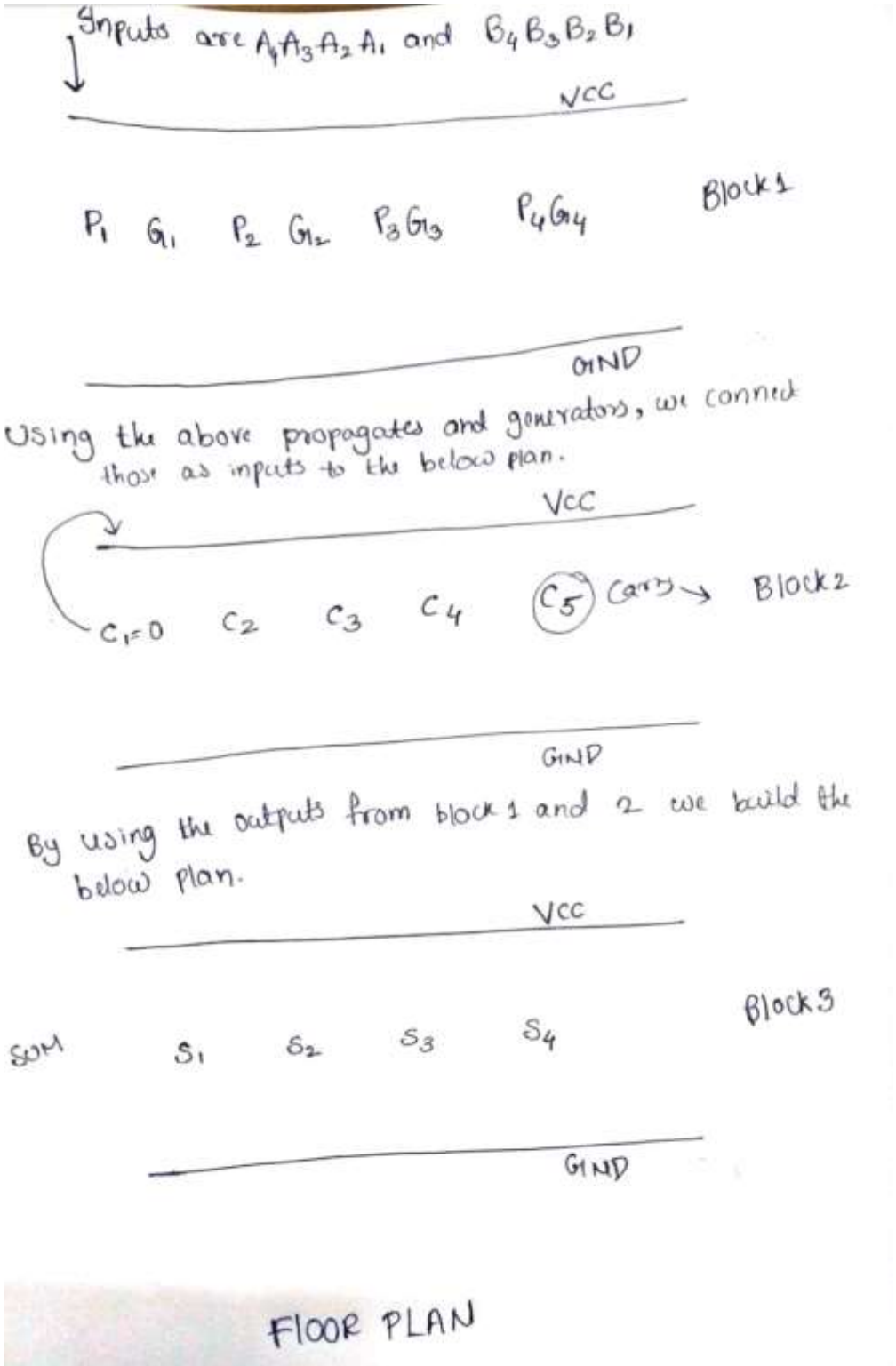
C5 S1 S2



S3 S4

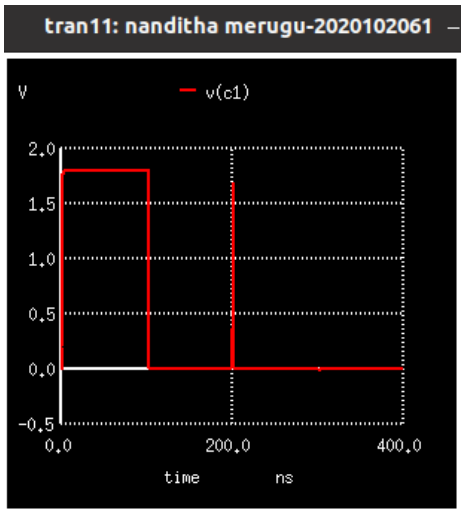
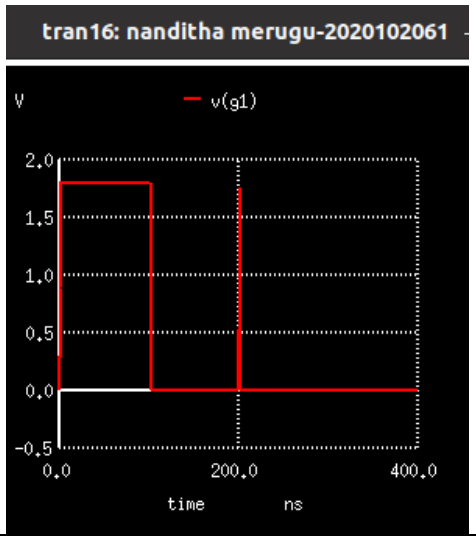
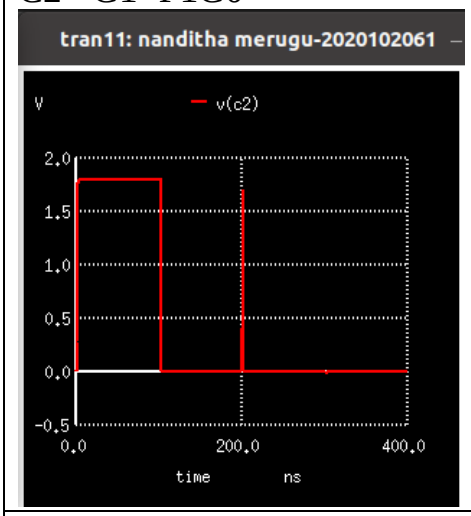
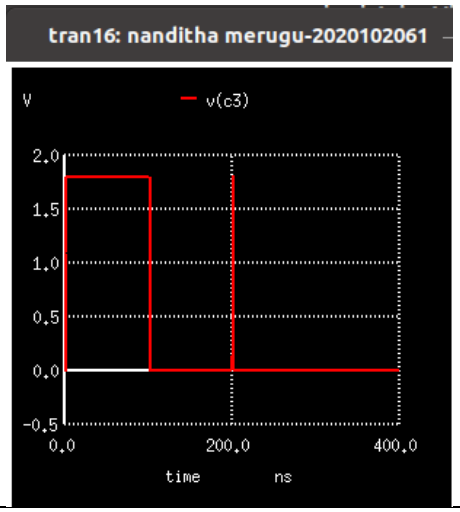


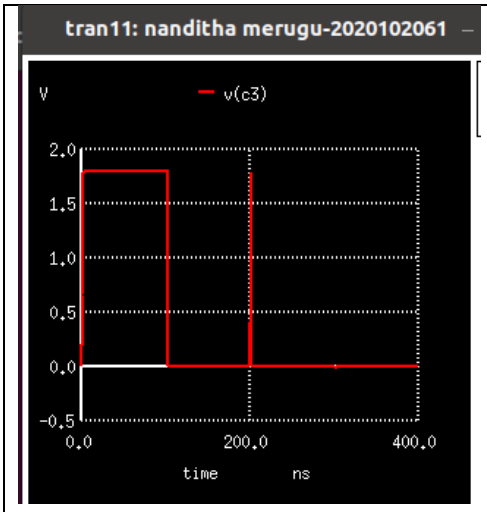
Floor Plan:

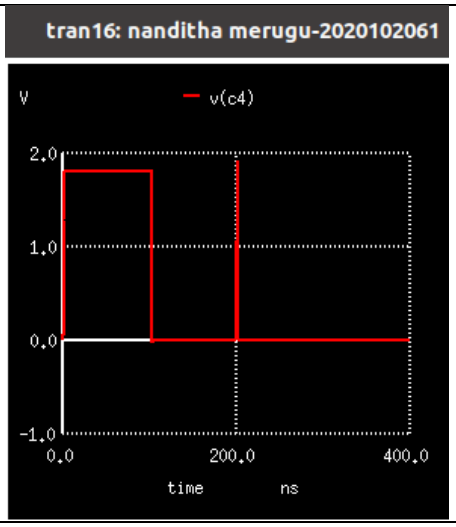


FLOOR PLAN

Comparison between pre and post Layout:

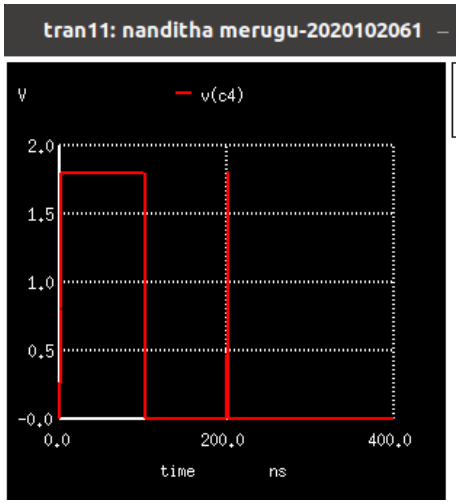
PRE-Layout plots (Here, I considered C0 as input carry) and took it as 0	POST-Layout plots (Here, I considered C1 as input carry) and took it as 0
C0=0	C1=0
C1=G0 	C2=G1 
C2= G1+P1G0 	C3= P2G1+G2 
C3= G2+P2G1+P2P1G0	C4= P3P2G1+P3G2+G3

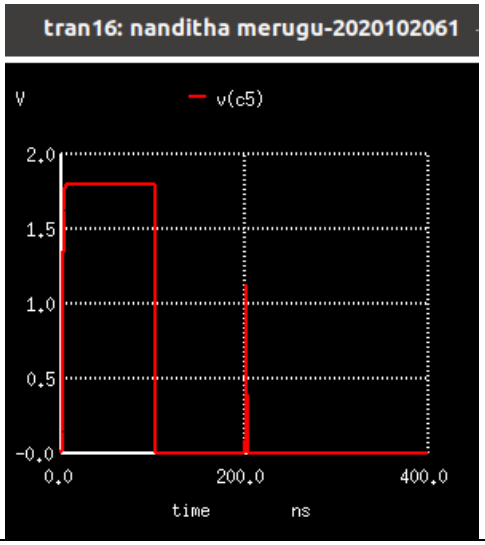




C4= G3+P3G2+P2P3G1+P3P2P1G0

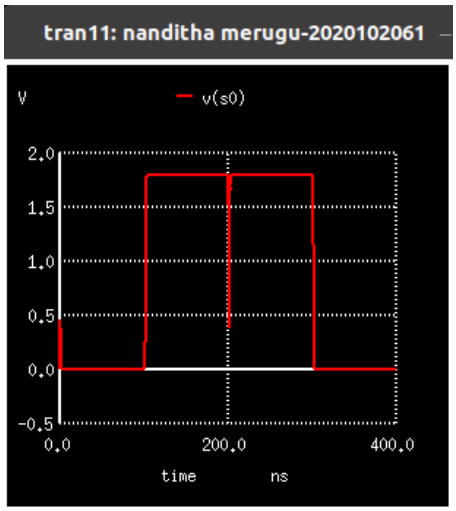
C5=P2P3P4G1+P3P4G2+P4G3+G4

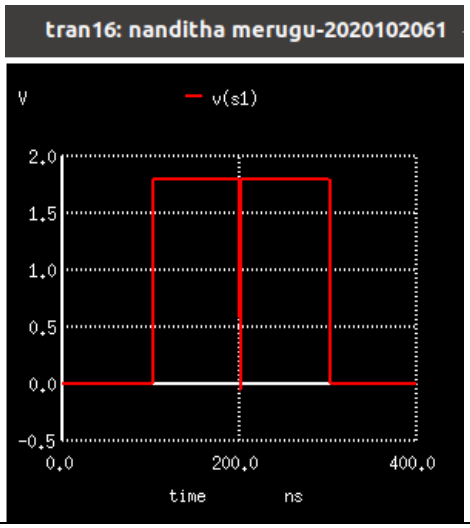




S0= P0 XOR C0

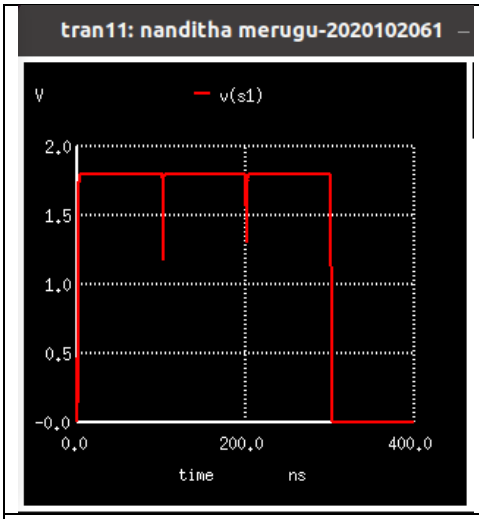
S1=P1 XOR C1

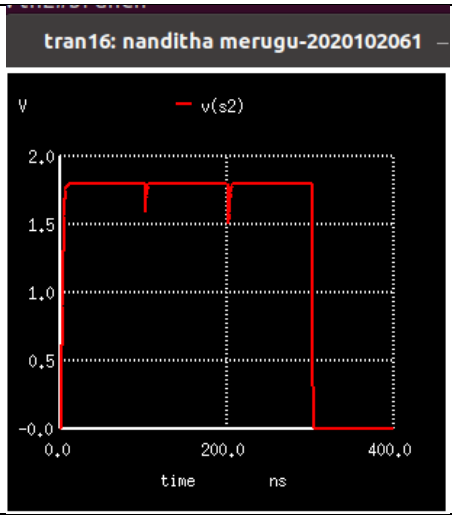




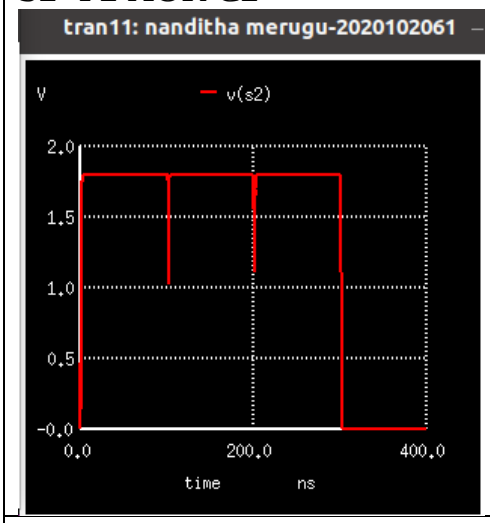
S1=P1 XOR C1

S2 = P2 XOR C2

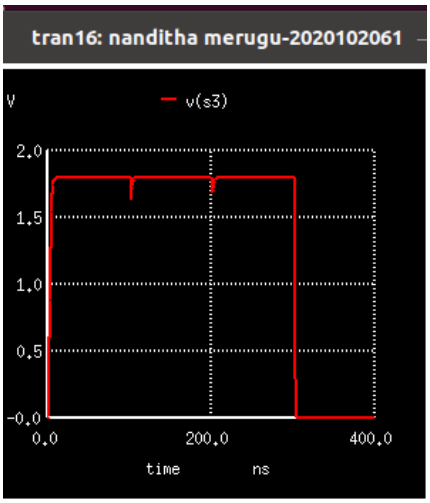




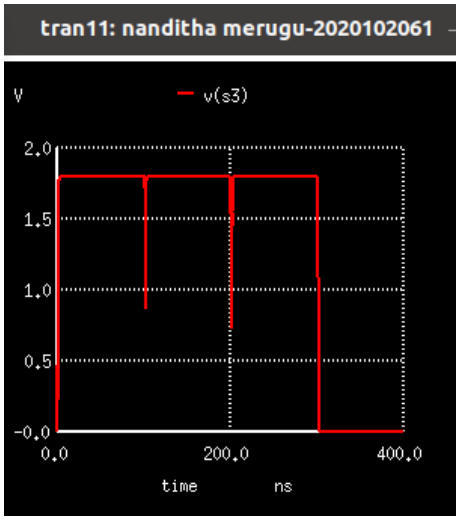
S2=P2 XOR C2



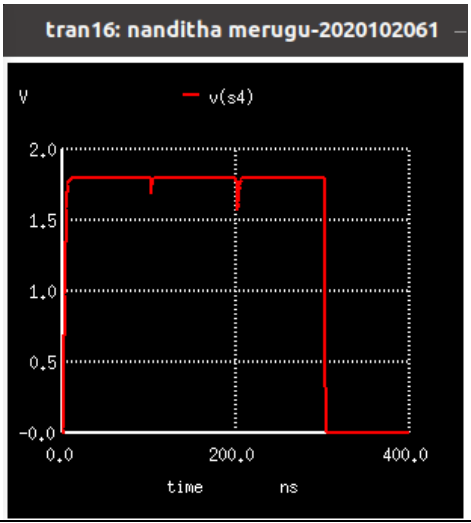
S3=P3 XOR C3



S3=P3 XOR C3



S4=P4 XOR C4



Verilog

Code:

This is the structural modelling part:

```
module Adder1(input A0,input A1,input A2,input A3,input B0,input B1,input
B2,input B3,output C1,output C2,output C3,output C4,output S0,output S1,output
S2,output S3);

wire G0,G1,G2,G3;
wire P0,P1,P2,P3;
wire C1,C2,C3,C4;
//Gi=Ai.Bi and Pi=Ai XOR Bi
and Gate1(G0,A0,B0);
and Gate2(G1,A1,B1);
and Gate3(G2,A2,B2);
and Gate4(G3,A3,B3);
xor Gate5(P0,A0,B0);
xor Gate6(P1,A1,B1);
xor Gate7(P2,A2,B2);
xor Gate8(P3,A3,B3);
wire w1,w2,w3,w4,w5,w6,w7,w8,w9,w10,w11,w12,w13,w14,w15,w16;
// C1=G0+P0C0
assign C1=G0;
// C2=G1+P1C1=G1+P1(G0+P0C0)
and Gate9(w1,P1,G0);
or Gate10(C2,w1,G1);
// C3=G2+P2C2=G2+P2[G1+P1(G0+P0C0)]
and Gate11(w2,P2,P1,G0);
and Gate12(w3,P2,G1);
or Gate13(C3,w2,w3,G2);
// C4=G3+P3C3=G3+P3[G2+P2[G1+P1(G0+P0C0)]]
and Gate14(w4,P3,P2,P1,G0);
and Gate15(w5,P3,P2,G1);
and Gate16(w6,P3,G2);
or Gate17(C4,w4,w5,w6,G3);
//S0=P0 XOR C0
xor Gate18(S0,P0,0);
//S1=P1 XOR C1
xor Gate19(S1,P1,C1);
//S2=P2 XOR C2
xor Gate20(S2,P2,C2);
//S3=P3 XOR C3
xor Gate21(S3,P3,C3);

endmodule
```

This is the testbench:

```
`include "A2.v"

module testbench;

integer i;
reg a0,a1,a2,a3,b0,b1,b2,b3;
wire c1,c2,c3,c4,s0,s1,s2,s3;
Adder1 FC(a0,a1,a2,a3,b0,b1,b2,b3,c1,c2,c3,c4,s0,s1,s2,s3);
initial begin
    $dumpfile("A2_2.vcd");
    $dumpvars(0,testbench);
    $monitor($time,"  a0=%b a1=%b a2=%b a3=%b b0=%b b1=%b b2=%b b3=%b c1=%b
c2=%b c3=%b c4=%b s0=%b s1=%b s2=%b
s3=%b",a0,a1,a2,a3,b0,b1,b2,b3,c1,c2,c3,c4,s0,s1,s2,s3);

    #5 a0=1 ; b0=1 ; a1=1 ; b1=1 ; a2=1 ; b2=1 ; a3=1 ; b3=1;
    #5 a0=1 ; b0=1 ; a1=1 ; b1=1 ; a2=1 ; b2=1 ; a3=1 ; b3=1;
    #5 a0=0 ; a1=0 ; a2=0 ; a3=0 ;
    #5 a0=0 ; a1=0 ; a2=0 ; a3=0 ;
    #5 a0=1 ; a1=1 ; a2=1 ; a3=1 ; b0=0 ; b1=0 ; b2=0 ; b3=0;
    #5 a0=1 ; a1=1 ; a2=1 ; a3=1 ; b0=0 ; b1=0 ; b2=0 ; b3=0;
    #5 a0=0 ; a1=0 ; a2=0 ; a3=0 ;
    #5 $finish;


end

endmodule
```

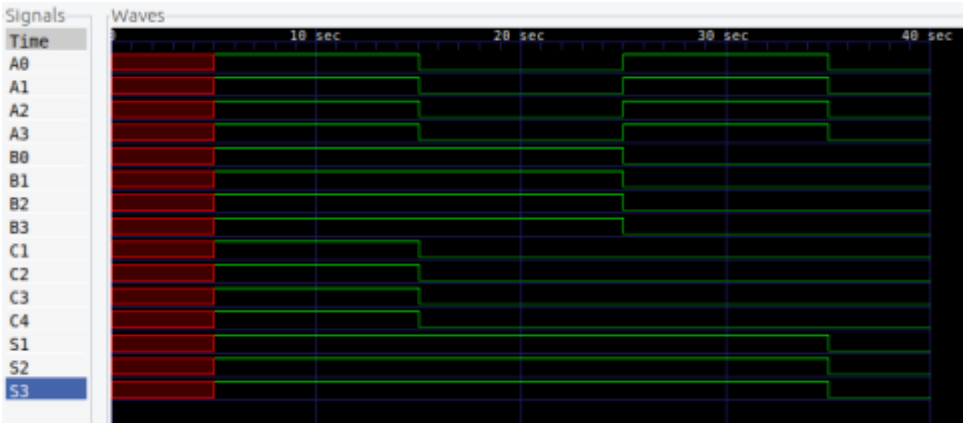
Output in the terminal:

5: a0=1 a1=1 a2=1 a3=1 b0=1 b1=1 b2=1 b3=1 c1=1 c2=1 c3=1 c4=1 s0=0 s1=1 s2=1 s3=1

15: a0=0 a1=0 a2=0 a3=0 b0=1 b1=1 b2=1 b3=1 c1=0 c2=0 c3=0 c4=0 s0=1 s1=1 s2=1 s3=1

25: a0=1 a1=1 a2=1 a3=1 b0=0 b1=0 b2=0 b3=0 c1=0 c2=0 c3=0 c4=0 s0=1 s1=1 s2=1 s3=1

35: a0=0 a1=0 a2=0 a3=0 b0=0 b1=0 b2=0 b3=0 c1=0 c2=0 c3=0 c4=0 s0=0 s1=0 s2=0 s3=0



The green is the actual signal.

- If we compare the results of verilog, ngspice and post layout simularion , all are seen to be same.