TECHNICAL EXPERIENCE DETAILS

DV Project (Personal)

Title	Intent	Outcome and Learnings
Synchronous FIFO	Implement FIFO design and UVM based test bench to validate the design	• Using SV learned to implement below a) FIFO design b) UVM test bench components like Scoreboard, Monitor, Driver, Sequencer, Environment, Agent • Github link: nandu161096/FIFO_UVM_TB_AND_DESIGN
8-bit cipher (Encryption & Decryption)	Implement 8-bit cipher design and UVM based test bench to validate the design	• Using SV learned to implement below a) Pseudo random generator (PRNG) b) Encryption & decryption c) UVM test bench components like Scoreboard, Monitor, Driver, Sequencer, Environment, Agent • Github link: nandu161096/8_BIT_CIPHER

WLAN Firmware - VI team | April 2024 – Present (Qualcomm Chennai)

<table>
<tr><th>General roles and responsibilities</th><th colspan="3">Details of Feature/Project</th></tr>
<tr><td rowspan="4">• Debugged the HW issues raised by SW team and resolved them quickly.
• Reviewing the code changes raised by peer engineers
• Proposed improvements in the VI testing infra to resolve the issues quickly.
• Mentored junior engineers
• Prepared the mid-level design document, test plan for the feature and present it to wider team.</td><td>Feature/Project</td><td>Intent</td><td>Outcome and Learnings</td></tr>
<tr><td>Mixed Mode testing - Feature</td><td>Stress the WLAN HW by
1) Enabling multiple features
2) Randomly changing the Wi-Fi parameters like BW, NSS, MCS.</td><td>• Gained experience using the emulation environment
• Understood the control path and data path in VI’s uFW
• Learned to use rand APIs to choose Wi-Fi parameters randomly.</td></tr>
<tr><td>Themisto 1.0 and 2.0 - Project</td><td rowspan="2">Validate the WLAN features in both pre/post Silicon stage and Silicon stage</td><td>• In both Themisto 1.0 and 2.0, brought up the WLAN features like rate walk, encryption, protection, aggregation via SW for each emulation release.
• Implemented automation infrastructure to execute the test cases automatically and simulation infra to RCA the HW issues.
• Identified 2 HW bugs (Decrypt failure & Decode failure for long packets) in Pre-Silicon stage</td></tr>
<tr><td>Trestles 1.0 - Project</td><td>• Brought up basic rate walk via SW in E1P5 emulation build
• Implemented recipe from DV team and validated the MAP feature.
• As part of MAP feature validation, identified a HW bug related to it.</td></tr>
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Linux Drivers – Network Subsystem Team | June 2022 - April 2024 (Qualcomm Bangalore)

General roles and responsibilities	Details of feature		
	Title	**Intent**	**Outcome and Learnings**
• Sustenance support in the modules like Linux core kernel, ethernet and PPE driver. • Reviewing the code changes raised by peer engineers • Proposed suggestions to improve the performance of the AP • Prepared the design document, test plan for the feature and present it to wider team	Energy related products (ERP) regulations – phase 2	Enter low power mode where there is no activity for 20 minutes in the DUT	• Learned to use interface stats, conntrack details and CPU utilization present in kernel to detect the idle state and enter low power mode
	Energy related products (ERP) regulations – phase 1	• CLI commands in the QSDK to enter and exit low power mode by making the interfaces to up and down respectively • In the low power mode, the energy consumption will be low	• Mastered to implement the CLIs and parsed the input from user • Implemented a user space layer interact with kernel via NL socket
	Passing the traffic via PPE with VLAN over bridge topology (Requested by Customer)	With VLAN over bridge topology, pass the traffic via PPE (Packet processing engine) to improve the performance	• Explored the ECM (Enhanced connection manager) driver for flow creation and learned to configure PPE HW via PPE driver to accelerate the traffic with VLAN over bridge topology.
	Direct Switch Feature	The traffic between ethernet and Wi-fi will flow via hardware to improve the egress rate.	• Executed the test cases suggested by leads and resolved the issues which popped up. • Provided sustenance support for the feature.

Radio Driver/Firmware Sustenance Team | June 2018 – April 2021 (EmbedUR Systems Chennai)

Title & Aim	Roles and Responsibilities
Title: WNBU-Cheetah NXP **AIM:** Provide radio driver /firmware sustenance in CISCO AP (8964 Wi-fi chip based)	• Fixing issues in the wireless radio driver/firmware code based on **Linux OS** • Evaluating and assessing the new feature request • Providing technical guidance, leading and reporting the status of the team to internal manager periodically • Performed Unit testing and conducted code review internally **Issue/Modules worked:** Beacon management, Jitter issue, Mesh, Radio driver initialization, Client connectivity issues, data path & control path

Board Support Package Team | April 2021 – June 2022 (Nokia Chennai)

<table>
<tr><th>General roles and responsibilities</th><th colspan="3">Details of feature</th></tr>
<tr><td rowspan="4">Sustenance support in the BSP modules
Reviewing the code changes raised by peer engineers</td><td>Title</td><td>Intent of the feature</td><td>Outcome and Learnings</td></tr>
<tr><td>Board bring up of OLT based on ARM A-53</td><td>From platform team perspective, bring up the board and start the applications</td><td>Learned how inter core communication works in a SOC by implementing mailbox driver using RPMsg-Lite infrastructure
Compilation of all SW modules using gcc10 tool chain to successfully build the ELF image
Implemented a watch dog timer feature to update master core about the status of slave core</td></tr>
<tr><td>CPU Load measurement</td><td>To compute the CPU load periodically and raise an alarm to the application layer when CPU load is high</td><td>Learned to create a task to compute the CPU load periodically from PCB (process control block) structure
Raise an alarm to the application layer when CPU load is high and clear it when CPU comes to normal
Implemented trace and debug command to raise/clear the alarm for testing</td></tr>
<tr><td>40GBASE-KR4 support in 7250 Switch</td><td>Scope is to operate the switch port in 40G and provide sustenance</td><td>Implemented a state machine between switch and line card to operate the port in 40G
Provided sustenance support till the feature is delivered in main stream</td></tr>
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