Green Arrays™

Product Data Book

EVB001 Evaluation Board for G144A12

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PRELIMINARY DATA

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Contents

1. Introduction

This is the primary reference manual for the EVB001 Evaluation Board. With two GreenArrays G144A12 chips, peripherals sufficient for a complete software and hardware development environment, and a large prototyping area, this highly configurable board is intended to serve both engineers and programmers well in evaluating our chips in all stages of application development.

Initially shipped with eForth in flash, this board is field upgradable with additional system software, such as polyFORTH®. In addition, our Application Notes will use this board as their default platform so that our customers may make immediate use of the hardware and software solutions published in those exercises.

1.1 Related Documents

This book describes an application of GreenArray chips, in particular the GA144. In the interest of avoiding needless and often confusing redundancy, it is designed to be used in combination with other documents.

The general characteristics and programming details for the F18A computers and I/O used in the GA144 are described in a separate document; please refer to *F18A Technology Reference*. The boot protocols supported by the chip are detailed in *Boot Protocols for GreenArrays Chips*. The configuration and electrical characteristics of the chip are documented in *G144A12 Chip Reference.* The current editions of these, along with many other relevant documents and application notes as well as the current edition of this document, may be found on our website at http://www.greenarraychips.com . It is always advisable to ensure that you are using the latest documents before starting work.

1.2 Status of Data Given

The data given herein are *preliminary*. The subject application is under development. Production data may be released in subsequent editions.

1.3 Documentation Conventions

1.3.1 Numbers

Numbers are written in decimal unless otherwise indicated. Hexadecimal values are indicated by explicitly writing "hex" or by preceding the number with the lowercase letter "x". In colorForth coding examples, hexadecimal values are italicized and darkened.

1.3.2 Node coordinates

Each GreenArrays chip is a rectangular array of ***nodes,*** each of which is an F18 computer. By convention these arrays are represented as seen from the top of the silicon die, which is normally the top of the chip package, oriented such that pin 1 is in the upper left corner. Within the array, each node is identified by a three or four digit number denoting its Cartesian coordinates within the array as *yxx* or *yyxx* with the lower left corner node always being designated as node 000. Thus, for a GA144 chip whose computers are configured in an array of 18 columns and 8 rows, the numbers of the nodes in the lower right, upper left, and upper right corners are 017, 700, and 717 respectively.

1.3.3 Register names

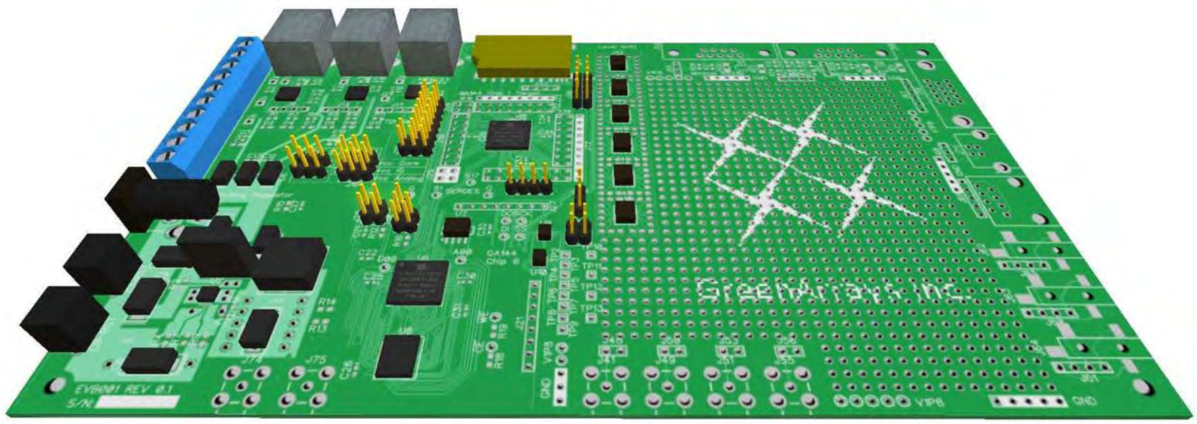
Register names in prose may be used with or without the word "register" and are usually shown in a bold font and capitalized where necessary to avoid ambiguity, such as for example the registers **T S R I A B** and **IO** or **io** .

1.3.4 Bit Numbering

Binary numbers are represented as a horizontal row of bits, numbered consecutively right to left in ascending significance with the least significant bit numbered zero. Thus bit *n* has the binary value 2^n. The notation P9 means bit 9 of register **P**, whose binary value is x200, and T17 means the sign (high order) bit of 18-bit register **T**.

2. Basic Architecture

The purpose of this board is to facilitate evaluation and application prototyping using GreenArrays chips. Because no single I/O complement would be suitable for all likely uses, this board has two GA144 chips: One (called "Host") configured with sufficient I/O for intensive software development, and the other (called "Target") with as little I/O committed as possible so that pure, dedicated applications may be prototyped.



2.1 Highlights

Three FTDI USB to serial chips provide high speed (960 kBaud) communications for interactive software development and general-purpose host communications.

An onboard switching regulator takes power from the USB connectors and/or a conventional "wall wart" power supply. Whichever of these is offering the highest voltage is used by the regulator.

A barrier strip provides for connection of bench power supplies. Each of the power buses of the two GA144 chips may selectively be run from external power in lieu of the onboard regulator, allowing you to run either chip from any desired V_{DD} voltage and also facilitating current measurements.

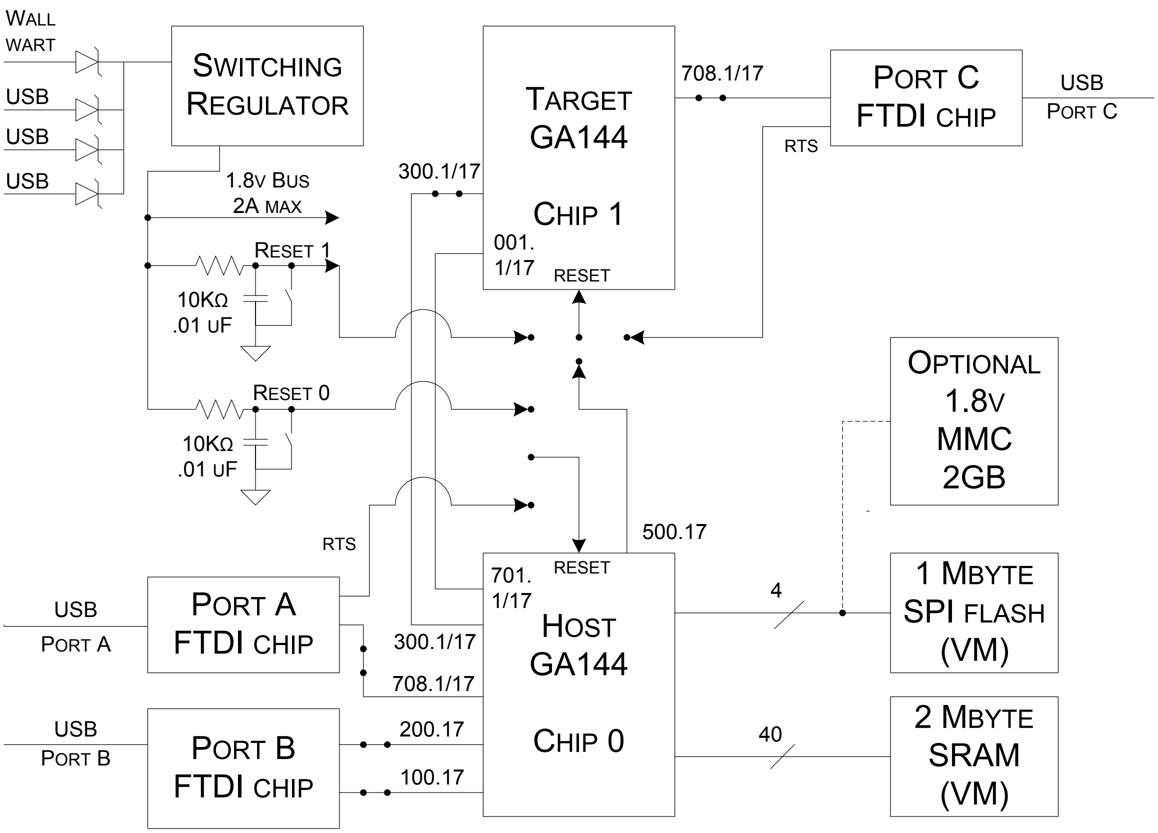
The Host chip is supplied with an SPI boot flash holding 1 MByte of nonvolatile data, an external SRAM with 1 MWord (2 MBytes) of memory; and may optionally use a dual voltage MMC card such as the 2 Gigabyte unit we have selected for in-house use. These memory resources may be used in conjunction with Virtual Machines such as eForth and polyFORTH, or for direct use by your own F18 code.

The Target chip is committed to as few I/O connections as possible. The sources for its reset signal are fully configurable, and with the exception of a SERDES line connecting it with the Host chip, all other communications (two 2-wire serial interfaces) may be disconnected so that the chip is fully isolated and thus all practical I/O is available for any desired use.

Roughly half the board is prototyping area, mainly populated with a grid of plated through holes on 0.1 inch centers. By soldering suitable headers to this grid, you can provide for expansion using various prototyping fixtures such as those made by SchmartBoard. The grid is intentionally large enough to support an 8- or 16-bit PC-104 socket.

The periphery of the prototyping area is provided with hole patterns for many popular connectors, and there are six 8-bit bidirectional level shifters for interfacing with external circuits that may not run on 1.8v. In addition, one 1.8v 2-input OR and three NANDs are available for use in external circuitry.

2.2 Simplified Block Diagram



As delivered, Host chip boots a Virtual Machine such as eForth or polyFORTH from flash and talks to terminal on RS232 port B. Ports A and C are available for IDE operations on Host and Target chips. Target may be fully isolated from Host with the exception of the SERDES connection. Other software options including other Virtual Machines besides eForth will be available for field upgrade.

2.3 Header Orientation

For all single-row headers or hole patterns, pin 1 is at the left as viewed from the top side of the board with USB connectors in the upper left corner; for single column patterns, pin 1 is at the top. For headers with 2 pin short dimensions, pin 1 will be in the lower left corner for horizontally oriented patterns and in the upper left corner for vertical patterns. In the special case of 2x2 patterns, pin 1 is always in the upper left corner. The following diagrams illustrate these orientation conventions and pin numbering:

1	2	3

1
2
3

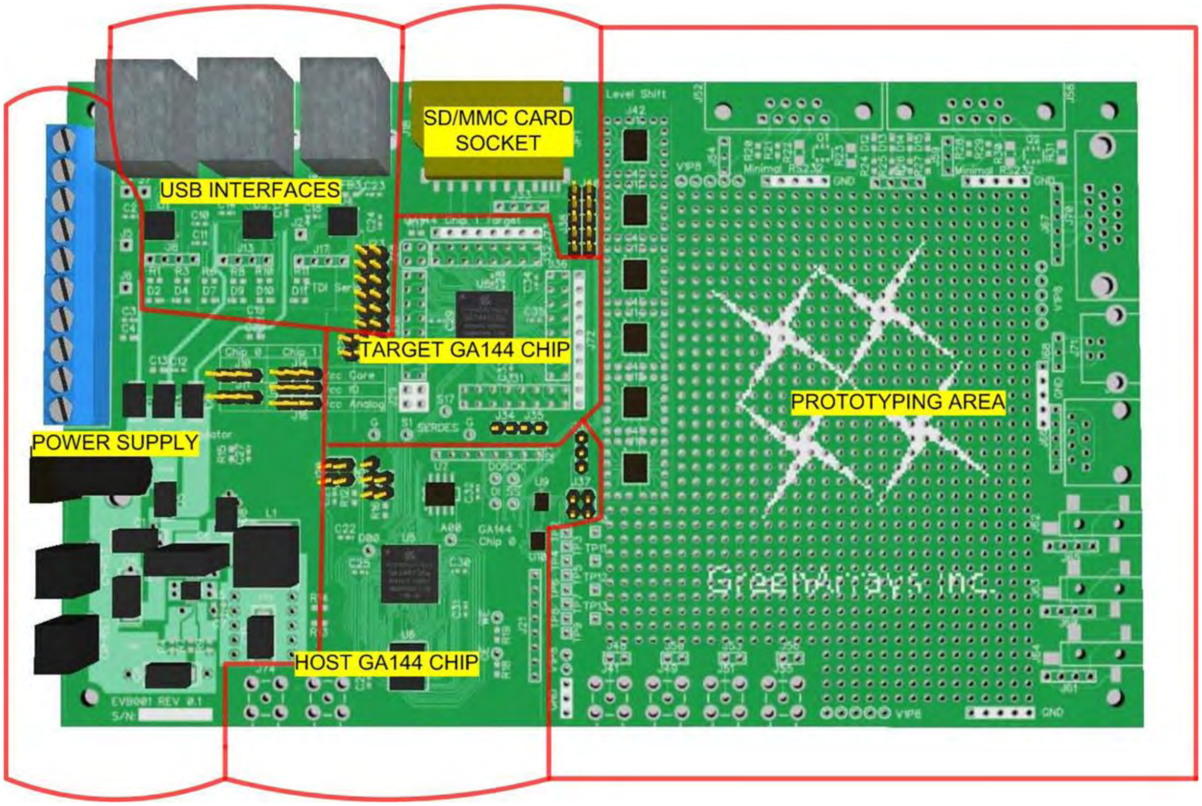
2	4	6
1	3	5

1	2
3	4
5	6

1	2
3	4

2.4 Board Floorplan

This overhead image of the evaluation board shows the spatial relationships among the subdivisions that are discussed in the following sections.



2.5 Software Support

This board is supported by four major classes of software:

1. ***arrayForth*** is presently the principal tool for creation of native code, or microcode, to run directly on the F18 computers in our chips. Included are compilers, simulators, an Interactive Development Environment (IDE), and boot stream generator. arrayForth maintains F18 source code in *colorForth* notation. The arrayForth system itself is written in and runs on colorForth, which may be run on a wide variety of platforms.

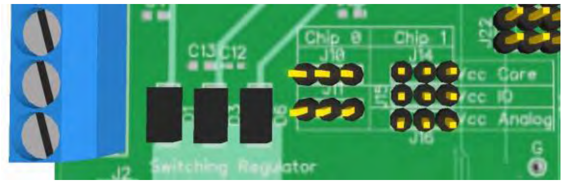
2. ***Virtual Machines*** running in clusters of F18 nodes support high level programming environments whose natures imply external memory resources. Examples are *eForth* and *polyFORTH*. These environments may interact with microcode running in the rest of the chip, supervising their high performance activities. Some environments may also support development of native F18 code as a supplement or complement to arrayForth.

3. ***Host platform applications***, such as enhanced terminal emulators, may be supplied with the virtual machines or other applications that use them.

4. ***Applications provided for this board*** will include source code for arrayForth and/or for specific Virtual Machines, and often hardware configuration or modification instructions, as appropriate.

Software options for GreenArrays chips and boards are continually being developed, and may be obtained from our website.

3. Power Configuration



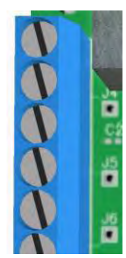
You must ensure there is enough power for the intended use of the board. Minimal USB (80% of 440 mW) is sufficient for eForth/polyFORTH and many typical projects, but power requirements can exceed 400 mW for V_{DD}C (core power) if enough F18A computers are busy simultaneously, and likewise V_{DD}I (I/O power) can be greater than this depending on what you connect to the chips. Several power sources are available in the upper left corner of the board.

3.1 Main 1.8v Bus

Primary 1.8v power is supplied by an onboard fixed voltage regulator fed by an optional "wall wart" and up to three USB connectors. Each source is diode protected from the others so whichever one is supplying the highest voltage will be the one that is used at any given time. Each USB connector communicates with a USB host using an FTDI chip. The power available from each USB connection varies from a minimum of 100 mA at 4.4V to the maximum of 500 mA at 5V; the FTDI chips are configured to request permission to use the maximum to improve flexibility. An efficient (≈78%) switching regulator produces a maximum of 2A at 1.8V for the logic circuitry on the board.

The main 1.8v bus is used to power our side of the FTDI chips, the SPI flash, the Host chip's external SRAM, and the two logic chips used in SPI bus multiplexing. This bus is also the default source of V_{DD}C, V_{DD}I and V_{DD}A for the Host and Target chips. Finally it is available to power the SD/MMC socket, the level shifter chips, and is routed for easy availability in the prototyping area.

3.2 External DC Supplies

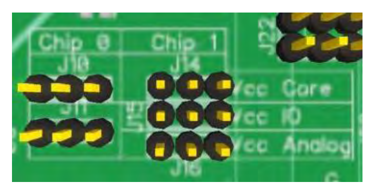


Barrier strip J1 provides for connecting up to five independent external power sources to this board, three of which are free for your use and wiring at J4, J5 and J6, while two have defined uses. Pin 1 may be used as an alternate source for any of the Target chip's V_{DD} buses. Pin 3 may be used as an alternate source for the Host chip's V_{DD}C and/or its V_{DD}I and V_{DD}A. This facilitates operating either or both of the chips at any desired supply voltage. It also provides for applications that require more than 2A of 1.8v.

3.3 Power Selection and Measurement

Five 3-pin headers allow selection of either the main 1.8v bus or an external supply as shown in this table:

Header	Chip	Bus	Pins 1-2 connected	Pins 2-3 connected
J10	Host	V_{DD}C	J1 pin 3	Main 1.8v Bus
J11		V_{DD}I/A		
J14	Target	V_{DD}C	J1 pin 1	
J15		V_{DD}I		
J16		V_{DD}A		



Current may be measured by inserting a shunt or other type ammeter across the desired pair of pins. Some combinations of current and shunt resistance will require use of an adjustable external power supply to give the desired voltage on the chip side of the shunt.

3.4 Other Available Voltages

An unregulated V_{CC} is input to the onboard switching regulator. No contact is provided because the voltage is not controlled. Each FTDI chip that is connected to a USB host can provide up to 50 mA of 3.3v, made available on J7, J12 and J19 for ports A, B and C respectively.

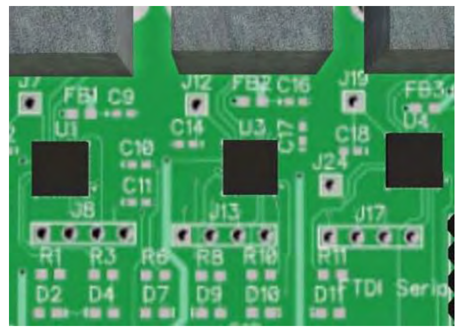
4. USB Interfaces

Three USB device interfaces provide for high speed communications with the GA144 chips. To a host computer each of these normally appears as an asynchronous serial (COM) port. Although each has a specific planned use on this board, their configuration is highly flexible.

4.1 Interface Devices

The devices provided are FT232R chips made by Future Technology Devices International, Ltd. (FTDI). As USB to serial UART devices, their USB side is powered by V_{CC} from the USB host while the side which talks to our chips is powered by the main 1.8v bus regulated on the board. Because the FTDI chips communicate with the GA144s directly using 1.8v CMOS, signals are crisp enough that each interface can run at an effective speed of 921,600 baud.

4.2 Jumpers and Connections



Transmit and receive lines are routed to the Host and Target GA144 chips as described in later sections. Request to Send (RTS) signals from ports A and C are available for chip reset purposes. RTS from port B is available at plated through hole J24.

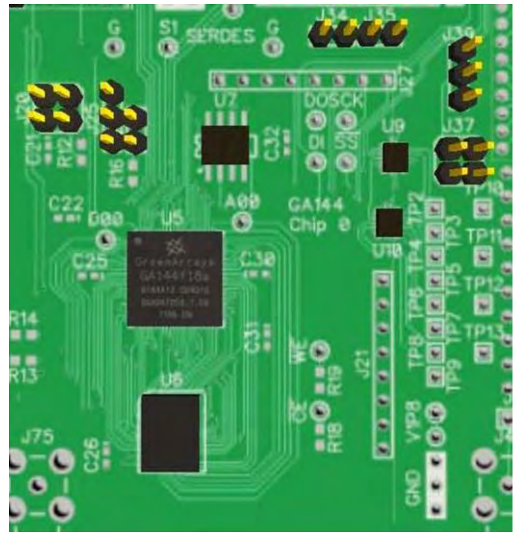
Each FTDI chip is configured to drive transmit and receive activity LEDs D2, D4, D7, D9, D10 and D11 respectively. The remaining three configurable outputs, and the DTR signal, are available at hole patterns J8, J13 and J17 for ports A, B and C respectively. By default two of these outputs are configured with clock signals that may be used for time base purposes.

Each FTDI chip develops 3.3v for internal use. Plated through holes J7, J12 and J19 provide access to this supply from ports A, B and C respectively; up to 50 mA may be drawn from each of these for your circuitry if needed.

4.3 Flash Configuration

The FTDI chips are specially configured for their use on this board. Excellent documentation as well as configuration utilities and drivers are available from the manufacturer at http://www.ftdichip.com/. Please contact us before changing the configuration of your FTDI chips.

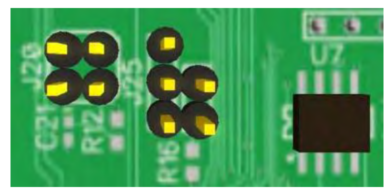
5. Host Chip



The Host chip, designated chip 0 on some of the design documentation, is by default configured as a development system including hardware and software support for a high level language such as eForth or polyFORTH. The photo to the right shows the section of the board housing this powerful system including 144 F18 computers, two USB serial ports, 1 Megaword (2 MBytes) of external SRAM, 8 megabits (1 Mbyte) of bootable SPI flash, and optional provision for using a dual voltage MMC card as onboard mass storage. All connections make use of software defined I/O with minimal or no external circuitry. For example, U9 and U10 are included only to facilitate selection of multiple SPI devices.

Most host pins, other than those used to control SRAM, are available at jumper stakes or hole patterns such as J21 and J27. Several probe points are provided: WE-, CE-, A00 and D00 show SRAM timing; SS, SCK, DO and DI show signals at the SPI flash chip. S1 and S17 may be used, *with great care*, to probe the SERDES connection between Host and Target chips.

5.1 Reset Control

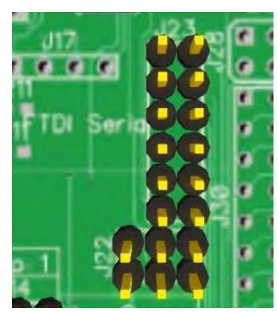


The board has two circuits to generate power-on and pushbutton reset signals, one each for the Host and Target chips. For the Host, this signal terminates at jumper block J20 along with the RTS signal from USB port A (normally used for IDE operations on the Host.) By setting jumpers appropriately, the Host chip may be reset by either, both, or neither of these signals according to the following table:

J20 Pins	
1	2
3	4

J20 pins	Reset Source
None	User provided inputs on pins 1 or 2
1-3	USB port A RTS signal
2-4	Host chip reset circuit / button
1-3 & 2-4	Reset circuit / button or USB port A RTS

5.2 Serial Interfaces



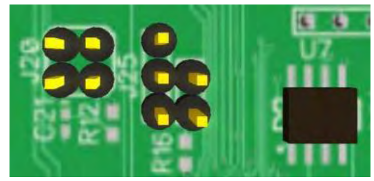
USB port A is intended, by default, to be used for programming of the Host chip using the arrayForth Interactive Development Environment (IDE). Transmit and receive lines may be connected to async boot node 708 by insertion of jumpers in J23. Reset from port A may be connected as shown above. Port B is primarily intended to be used for a serial interface to the eForth or polyFORTH system; it too may be connected to no`des 100 and 200 by insertion of jumpers in J23. The mapping in J23 is as follows:

Signal	USB port	J23 pins		Host pins	USB port	J23 pins		Host pins	USB port	J23 pins		Target pins
Rx to chip	A	1	2	708.17	B	5	6	200.17	C	9	10	708.17
Tx from chip	A	3	4	708.1	B	7	8	100.17	C	11	12	708.1

5.3 SPI Bus and Devices

Node 705 of the host chip is equipped with ROM capable of booting from an external flash memory using the 4-wire SPI interface. Using jumper options, node 705 may be configured to boot from the onboard flash chip. It may also be configured to selectively use other SPI devices under control of node 600 and/or external logic you provide. One option that is explicitly supported is selection of either the SPI flash or a 1.8v MMC card in the SD card socket provided with the board, under program control. Jumpers may also be used to completely disconnect node 705 from any of these things so its four pins are free for other application use.

5.3.1 SPI Flash and Booting



Jumper block J25 controls SPI flash chip reset and booting options according to the following table:

J25 pins	J26 pins	Configuration
Don't Care	IN	Pulls Node 705 pin high. Node 705 does not attempt boot nor does it drive any of its pins.
Don't Care	OUT	Node 705 attempts reading flash and if validity checks pass it processes boot frame(s) from that device.
1-2	Don't Care	Flash chip is held in reset; all its pins are at high impedance so that node 705's pins are available for other use.
2-3	Don't Care	Flash chip is reset by the Host chip's reset circuit/button and, if both J20 jumpers are inserted, by USB port A RTS.

J25	J26
1	
2	1
3	2

Evaluation boards are shipped with a high-level virtual machine set to boot from flash. New software is initially loaded into flash using the arrayForth IDE; the procedure for doing this requires use of J26.

For other uses of the flash by software packages such as eForth and polyFORTH, and for software installation procedures, see the documentation for each software package..

For low-level application use, see arrayForth source code and application notes.

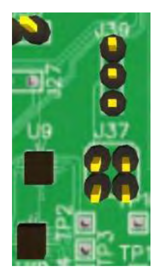
5.3.2 MMC Card Mass Storage

The SD card socket also accepts MMC cards, and because dual voltage MMC cards support 1.8v VDD and signaling logic levels, such cards may be directly controlled by the GA144. polyFORTH is configured by default to make use of such an MMC card as mass storage, and the board's jumpers are set by default to enable this. The MMC card may be used for backup, data logging, and transport of code or data between evaluation boards or other computers.

5.3.3 Enabling MMC Card Selection

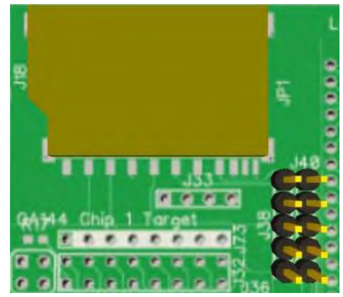
Two jumper blocks configure simple external circuitry for selecting between multiple SPI devices on the 4-wire bus controlled by node 705. The standard configurations are as follow:

J39	J37	
1	1	2
2	3	4
3		



J39 pins	J37 pins	Configuration
2-3	1-2, 3-4	SPI Flash is always selected. Node 600 unused.
1-2	1-2, 3-4	Node 600 selects SPI flash when its pin is low (reset condition), or MMC card when the pin is high.

5.3.4 Connecting MMC Power and Signals to SD Socket



The selection logic described in section 5.3.3 drives signals that terminate in J40 near the SD card socket, along with 1.8v for V_{DD} on MMC cards. To configure the SD socket to use these signals and power a dual voltage MMC card, install five jumpers between each pin of J40 and the corresponding pin of J38.

5.4 SRAM

The external SRAM may be used with the virtual machines supporting high level languages, in which SRAM control software is inherently present, or it may be used directly by F18 applications. In the latter case, one option is to employ the SRAM control cluster (four nodes) supplied with arrayForth. Alternatively you may write your own. No optioning nor interface circuitry is needed; probe points are provided to facilitate I/O software development.

5.5 Connections to Target

Host SERDES node 701 is hardwired to Target node 001 with probe points. This connection may be used for programming or otherwise communicating with the Target, to evaluate the SERDES, and to explore and develop protocols.

Host node 500 drives a signal that connects to the jumper block as one source of reset signal for the Target chip.

Host node 300 may be connected to Target node 300; this allows the Host to boot the Target using 2-wire synchronous protocol.

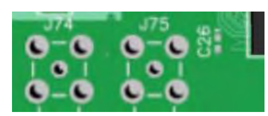
5.6 Summary of Host Pin Usage

Although many Host pins are committed to SRAM control, a good number remain available for application use.

5.6.1 Committed by Layout

All 40 pins of nodes 7, 8 and 9 are committed to SRAM control. Only four of these lines are available for probing. SERDES lines from node 701 are committed to Target communication.

5.6.2 Uncommitted



All ten Analog I/O pins are uncommitted, as are the GPIO pins of nodes 217, 317, 417, 517 and 715. These 15 pins are available on hole patterns J21 and J27.

Node 001.1 and .17 (SERDES data and clock) are available at SMA patterns J74 and J75 respectively.

5.6.3 Conditionally Available

Nodes 100 and 200 are committed only if eForth or polyFORTH is used; otherwise their GPIO pins are available. *All of the pins in this section are accessible at plated through holes or at jumper blocks.*

Node 300 has two GPIO pins which are available unless you require them for Target communication.

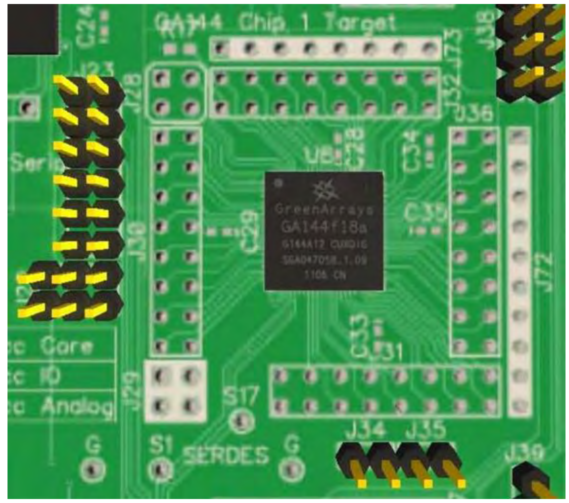
Node 500 has one GPIO pin that's available unless you need to use it for Target reset.

Node 600 has one GPIO pin that's available if you are not using the MMC card option.

Node 705 has four GPIO pins that are committed for SPI bus control, but if that is not needed the SPI chips can be disabled and all four pins are available. (Pin 17 must still be pulled high if you wish to prevent boot validity check when the chip is reset.)

Node 708 is normally used for arrayForth IDE but if not required these are available for asynchronous boot or any other desired use.

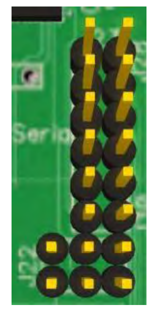
6. Target Chip



The Target chip, designated chip 1 on some of the design documentation, is configured in such a way that it may be booted and debugged, but otherwise all of its pins are available for your application. One possible use is as an I/O or computational expander for the Host chip. However the key reason for providing the Target chip on this evaluation board is to address your need to prototype a full application for a dedicated GreenArrays chip without having to lay out a board or disconnect a great deal of evaluation circuitry.

All but seven of the Target I/O pins are completely uncommitted, and are available in hole patterns J30, J31, J32 and J36 as shown in the picture at right. Of those seven, all but two may be disconnected with jumpers to isolate the Target chip for use in a dedicated application prototype.

6.1 Reset Control



J22		
2	4	6
1	3	5

Target reset is configured using J22 to the left of the chip. The three pins on the top edge of the header (2, 4 and 6) are connected in parallel to the RESET- pin of the Target chip. The other three pins are connected with reset sources that may be combined as a summing point. Pin 1 is connected to Host chip node 500; pin 3 is connected to USB port C RTS- line (low when RS232 signal would be low); and pin5 is connected to the power-on and pushbutton reset circuit for the Target chip.

6.2 Serial Interface

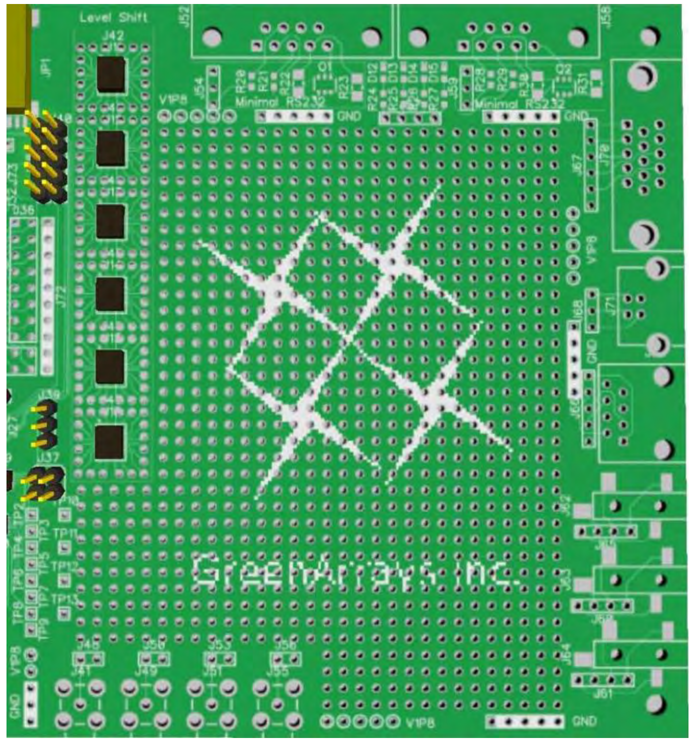
USB port C is available to be used for programming the Target chip using the arrayForth IDE. Transmit and receive lines may be connected to async boot node 708 by insertion of jumpers 9-10 and 11-12 of J23 located above the J22 reset control jumper, as shown earlier in section 5.2.

6.3 Host Chip Communications

As noted earlier, Host SERDES node 701 is hardwired to target node 001 with probe points as shown to the right.

Host node 300 may be connected with Target node 300 for booting or other communications. This is enabled by inserting jumpers J34 and J35 to the right of the SERDES probe points.

7. Prototyping Area



Half of the evaluation board's area is available for your use in building any desired circuitry. We have made this as flexible as feasible for a broad range of projects. The area is covered with patterns of plated through holes to which you may solder components, connectors, headers and so on as necessary. On the grounds that it is simpler and easier to solder multi-pin devices onto a board than it is to remove such devices when they are in the way, we supply an assortment of connectors and headers in a separate bag for your use.

GreenArrays expects to use this evaluation board as the primary platform for design exercises that will be published on our website as Application Notes suggesting ways to make good use of this area.

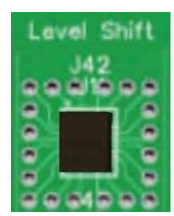
7.1 Plated-through Hole Grid

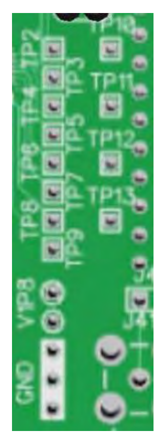
The large grid of plated through holes, on 0.1" centers, gives almost unlimited flexibility in breadboarding your circuits. The area is compatible with many common technologies that may be used to attach components, interfaces, or expand the area further by soldering 0.1" headers to the board in suitable patterns. These options will be expanded upon later.

7.2 Power, Ground and Signals

Hole patterns carrying the main 1.8v bus and common ground are available surrounding the prototyping area. Other supply voltages such as 3.3v from the FTDI chips or user supplied voltages from the J1 barrier strip must be hand wired, as must any other signals such as those from GA144 pins.

7.3 Convenience Circuits





For interfacing to devices with signal voltages other than the 1.8v native to the GA144, there are six 8-bit bidirectional level shifter chips in the prototyping area. These are Texas Instruments [TXB0108 devices in RGY packages] and for maximum flexibility none of their pins are connected except ground (pin 11 and die attach paddle.) You may use each of these chips to interface between 1.2 to 3.6v on the A port and 1.65 to 5.5v on the B port by connecting suitable supply voltages to each of the chip's two V_{CC} pins.

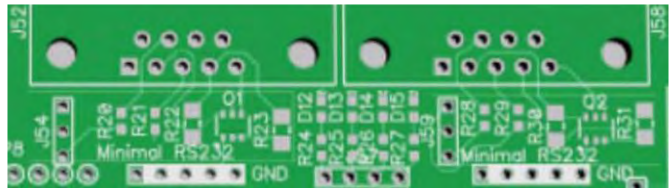
In addition, there are four uncommitted 2-input, 1.8v CMOS logic gates available for your use. These are located between the Host chip and the hole grid of the prototyping area. The table below identifies the connections and gate types.

Inputs		Output	Gate Type
TP4	TP5	TP11	2-input NAND
TP6	TP7	TP12	
TP8	TP9	TP13	
TP2	TP3	TP10	2-input OR

7.4 Optional Connector Hole Patterns

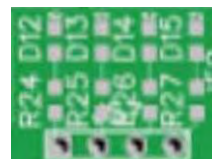
Unpopulated hole patterns are provided along the edges of the prototyping area for various connectors. Some connectors are supplied with the evaluation board so that you may solder in any that you require.

7.4.1 DB9 Connectors



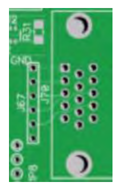
To interface with RS-232 devices, there are two female DB9 patterns. For your convenience, these are equipped with minimalist RS232 interfaces that may be used with our chips: Data receive and RTS signals are simply connected to GA144 pins through current limiting resistors, while data transmit is done with a pair of inverting N transistors powered by the Data Terminal Ready (DTR) line from the RS232 device. If these circuits don't do the trick, the components may be desoldered and direct connection made to the DB9 pins. Pins 1 of J54 and J59 are received data going to the GA144, pins 2 are transmit from the GA144, and pins 3 are incoming RTS. The inactive state of each of these RS232 lines is low.

7.4.2 General-Purpose LEDs



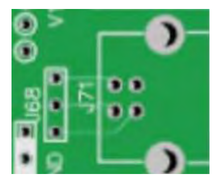
Located between the two DB9 patterns are four general-purpose LEDs, which may be turned on by supplying them with 1.8 volts on the geometrically corresponding pin of the adjacent pattern J57.

7.4.3 VGA Connector



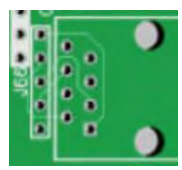
A pattern for a female 15-pin D shell provides the means for driving a VGA display directly from the GA144. Terminating resistor networks must be added if the device requires them.

7.4.4 USB Connector



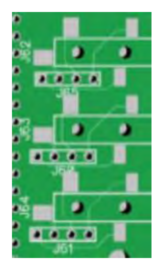
To facilitate development of USB device hardware and software, provision is made for attaching a USB type B receptacle to the prototyping area. Some interface circuitry will probably be needed.

7.4.5 RJ48 Connector



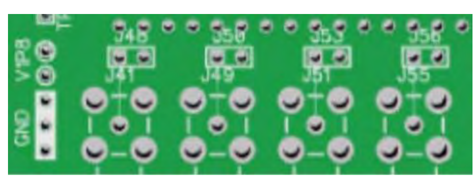
For development of 10baseT and perhaps other Ethernet interfaces, a pattern is provided for an RJ48 receptacle. Like USB, we expect that some minimal interface circuitry will be required as well.

7.4.6 Audio Connectors



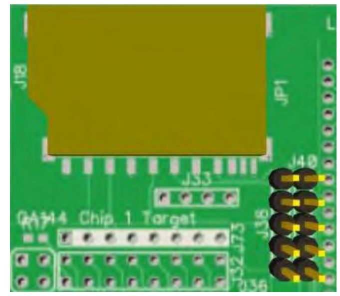
For analog audio input/output development, up to three 3.5mm stereo TRS receptacles may be soldered to patterns provided on the prototyping area.

7.4.7 SMA RF Connectors



At higher frequencies, RF connectors are more suitable for carrying signals on and off the evaluation board. Accordingly we provide five hole patterns for mounting SMA connectors, chosen for their small size and ready availability.

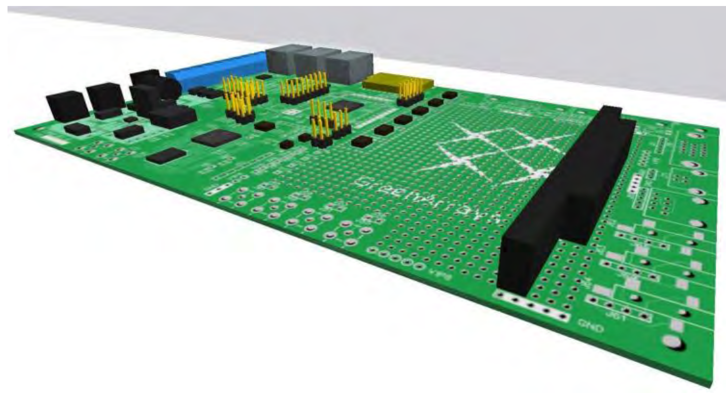
7.5 Optional use of SD socket



Although software being prepared for the evaluation board will be capable of taking advantage of a dual voltage MMC card for various purposes, the board layout is versatile enough to allow for development of code to access 3.3v SD cards as well. To take advantage of this capability, you must arrange to supply the SD socket with 3.3v power and construct the circuitry needed to communicate with it using 3.3v logic signals. All nine pins are available at the socket on J33 and J38, including two handhake lines, V_{DD} , all four data lines, card-present and write-protect signals.

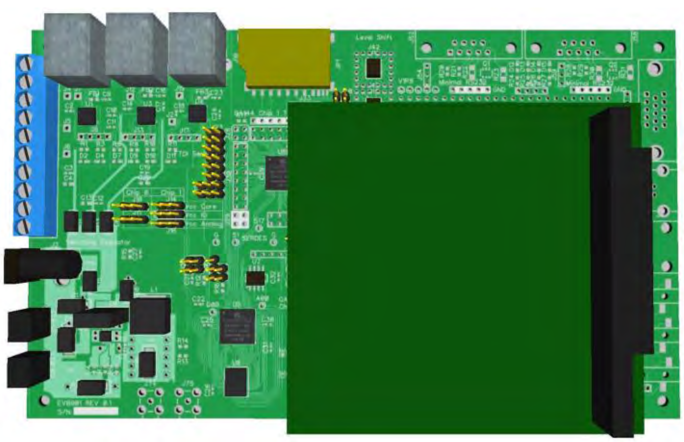
7.6 Expanding the Prototyping Area

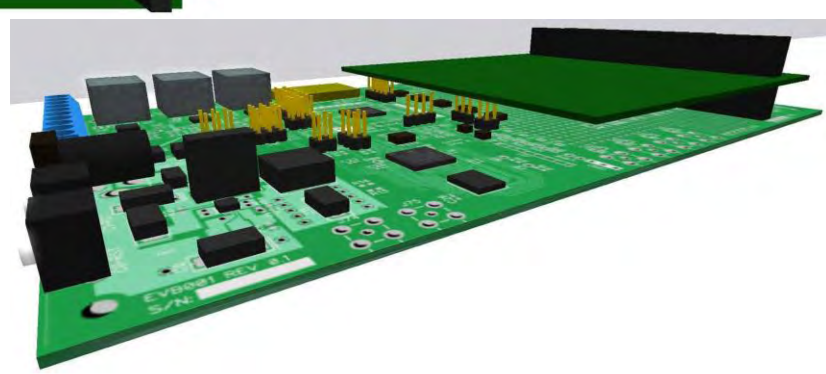
As suggested above, the grid of holes on 0.1" centers facilitates the installation of female headers into which various expansion devices may be plugged.



Schmartboard™ Products include small boards which can connect various surface mount parts to our prototyping area using 0.1" headers. This is considerably simpler and more likely to succeed than is "dead bugging" SMT components.

As another example, by soldering double row female headers appropriately in the prototyping area, PC-104 boards may be connected to the evaluation board. For example, see WinSystems® Products which include prototyping boards that could simply enlarge the prototyping area, or peripheral boards that could be used with level shifters.
Here is one possible placement of a 16-bit PC-104 connector and two views of a PC-104 board mounted on it:





Prototyping Area

8. Physical Documentation

This section includes signal tables, schematics and PCB layout artwork.

8.1 GA144 Signal map

These tables identify header pins or holes at which each chip's signals may be found.

8.1.1 Host Chip

<table>
<tr><th>Type</th><th>Name</th><th>Pin</th><th>Access</th><th>Description</th></tr>
<tr><td rowspan="18">SRAM Data Bus</td><td>d00</td><td>1</td><td>D00</td><td rowspan="18">Bits 0 through 17 of node 007 UP port.
General purpose bidirectional parallel bus.

Bits 0 through 15 are connected to the SRAM BGA and probe access is not supported except for bit 0 to probe timing. Mapping to SRAM data lines is randomized for best layout.

Bits 16 and 17 are pulled down so that they will read as zero.</td></tr>
<tr><td>d01</td><td>2</td><td rowspan="15">None</td></tr>
<tr><td>d02</td><td>3</td></tr>
<tr><td>d03</td><td>8</td></tr>
<tr><td>d04</td><td>9</td></tr>
<tr><td>d05</td><td>10</td></tr>
<tr><td>d06</td><td>11</td></tr>
<tr><td>d07</td><td>12</td></tr>
<tr><td>d08</td><td>13</td></tr>
<tr><td>d09</td><td>16</td></tr>
<tr><td>d10</td><td>21</td></tr>
<tr><td>d11</td><td>22</td></tr>
<tr><td>d12</td><td>23</td></tr>
<tr><td>d13</td><td>24</td></tr>
<tr><td>d14</td><td>25</td></tr>
<tr><td>d15</td><td>30</td></tr>
<tr><td>d16</td><td>31</td><td>R14</td></tr>
<tr><td>d17</td><td>32</td><td>R13</td></tr>
<tr><td rowspan="4">GPIO</td><td>008.17</td><td>33</td><td rowspan="2">None</td><td rowspan="4">General purpose 4-pin node used for SRAM control (1,3) and high order address lines (5,17). Pins 1 and 3 are pulled up so that the SRAM is made inactive when chip is reset.</td></tr>
<tr><td>008.5</td><td>34</td></tr>
<tr><td>008.3</td><td>35</td><td>WE-</td></tr>
<tr><td>008.1</td><td>36</td><td>CE-</td></tr>
<tr><td rowspan="18">SRAM Address Bus</td><td>a17</td><td>37</td><td rowspan="17">None</td><td rowspan="18">Bits 17 through 0 of node 009 UP port.
General purpose bidirectional parallel bus.

Bits 0 through 17 are connected to the SRAM BGA and probe access is not supported except for bit 0 to probe timing. Mapping to the low order 17 SRAM address lines is randomized for best layout. A17 must be mapped directly so that the layout will accommodate chips with 128k or fewer words.</td></tr>
<tr><td>a16</td><td>38</td></tr>
<tr><td>a15</td><td>39</td></tr>
<tr><td>a14</td><td>42</td></tr>
<tr><td>a13</td><td>43</td></tr>
<tr><td>a12</td><td>44</td></tr>
<tr><td>a11</td><td>45</td></tr>
<tr><td>a10</td><td>46</td></tr>
<tr><td>a09</td><td>53</td></tr>
<tr><td>a08</td><td>54</td></tr>
<tr><td>a07</td><td>55</td></tr>
<tr><td>a06</td><td>56</td></tr>
<tr><td>a05</td><td>57</td></tr>
<tr><td>a04</td><td>58</td></tr>
<tr><td>a03</td><td>65</td></tr>
<tr><td>a02</td><td>66</td></tr>
<tr><td>a01</td><td>67</td></tr>
<tr><td>a00</td><td>68</td><td>A00</td></tr>
</table>

SERDES	001.17	27	J75	Node 001 Clock	Available at dedicated SMA connector hole patterns..
	001.1	26	J74	Node 001 Data	
SERDES	701.17	86	S17	Node 701 Clock	Connected to Target node 001 SERDES. Both chips reset to SDERDES boot.
	701.1	87	S1	Node 701 Data	
GPIO	300.17	14	J35.1	Sync clock	General purpose 2-pin node. ROM supports synchronous boot. May be connected to Target node 300.
	300.1	15	J34.1	Sync data	
GPIO	708.17	78	J23.2	Rx Input	General purpose 2-pin node. ROM supports asynchronous boot. May be connected to USB port A for IDE operations.
	708.1	79	J23.4	Tx Out	
GPIO	705.17	85	DI	Data In	General purpose 4-pin node. Normally used for boot and/or read/write on SPI Flash and/or mass storage such as MMC depending on jumpers. May also be free for application use. When MMC selected, SS- and other signals are on J40.
	705.5	84	DO	Data Out	
	705.3	81	SS-	Chip Enable-	
	705.1	80	SCK	Clock	
GPIO	100.17	20	J23.8		1-pin GPIO nodes. May be connected to USB port B for use with high level Virtual Machines.
	200.17	18	J23.6		
	500.17	7	J22.1		1-pin GPIO node. May be used to reset the Target chip.
	600.17	6	J39.1		1-pin GPIO node. May be used in selecting expanded SPI bus.
	317.17	52	J21.5		1-pin GPIO nodes. Available for application use.
	417.17	59	J21.4		
Analog In	709.ai	76	J27.3		Analog nodes whose I/O is powered by separate $V_{DD}A$ bus. Available for application use.
Analog Out	709.ao	77	J27.2		
Analog In	713.ai	73	J27.4		
Analog Out	713.ao	72	J27.5		
Analog In	717.ai	69	J27.8		
Analog Out	717.ao	70	J27.7		
GPIO	715.17	71	J27.6		General purpose 1-pin node whose pin is shared (read only) by the above analog nodes and may be used by them for timing or other purposes.
Analog In	617.ai	61	J21.2		Analog node whose I/O is powered by $V_{DD}I$ bus.
Analog Out	617.ao	63	J21.1		
GPIO	517.17	60	J21.3		General purpose 1-pin node whose pin is shared (read only) by Analog 617.
Analog In	117.ai	48	J21.8		Analog node whose I/O is powered by $V_{DD}I$ bus.
Analog Out	117.ao	50	J21.7		
GPIO	217.17	51	J21.6		General purpose 1-pin node whose pin is shared (read only) by Analog 117.
Input	RESET-	88	J20.1		Reset signal, active low. Also pin J20.2.
Power	$V_{DD}C$	5	J10.2		Core power bus. Powers F18A computers, and parts of I/O circuitry (such as registers) that are internal to them.
		17			
		29			
		41			
		49			
		62			
		75			
		83			
Power	$V_{DD}I$	4	J11.2		I/O power bus. Powers I/O pads including the parts of the I/O circuitry collocated with the pads. Includes analog pads for nodes 117 and 617.
		19			
		28			
		40			
		47			
		64			
		82			
Power	$V_{DD}A$	74	J11.2		Analog power bus for pads of nodes 709, 713 and 717.
Ground	GND	DAP	any gnd		Common ground and heat sink.

8.1.2 Target Chip

Type	Name	Pin	Access	Description	
Bus I/O	d00	1	J30.1	Bits 0 through 17 of node 007 UP port. General purpose bidirectional parallel bus, such as external memory data.	
	d01	2	J30.2		
	d02	3	J30.3		
	d03	8	J30.6		
	d04	9	J30.7		
	d05	10	J30.8		
	d06	11	J30.9		
	d07	12	J30.10		
	d08	13	J30.11		
	d09	16	J30.12		
	d10	21	J30.15		
	d11	22	J30.16		
	d12	23	J31.1		
	d13	24	J31.2		
	d14	25	J31.3		
	d15	30	J31.4		
	d16	31	J31.5		
	d17	32	J31.6		
GPIO	008.17	33	J31.7	General purpose 4-pin node. Might be used for memory or bus control and handshake lines.	
	008.5	34	J31.8		
	008.3	35	J31.9		
	008.1	36	J31.10		
Bus I/O	a17	37	J31.11	Bits 17 through 0 of node 009 UP port. General purpose bidirectional parallel bus, such as external memory address.	
	a16	38	J31.12		
	a15	39	J31.13		
	a14	42	J31.14		
	a13	43	J31.15		
	a12	44	J31.16		
	a11	45	J36.15		
	a10	46	J36.14		
	a09	53	J36.9		
	a08	54	J36.8		
	a07	55	J36.7		
	a06	56	J36.6		
	a05	57	J36.5		
	a04	58	J36.4		
	a03	65	J32.2		
	a02	66	J32.3		
	a01	67	J32.16		
	a00	68	J32.15		
SERDES	001.17	27	S17	Node 001 Clock	Connected to Host node 701 SERDES. Both chips reset to SDERDES boot.
	001.1	26	S1	Node 001 Data	
SERDES	701.17	86	J28.2	Node 701 Clock	Available for experimentation.
	701.1	87	J28.4	Node 701 Data	
GPIO	300.17	14	J35.2	Sync clock	General purpose 2-pin node. ROM supports synchronous boot. May be connected to Host node 300.
	300.1	15	J34.2	Sync data	

GPIO	708.17	78	J23.10	Rx Input	General purpose 2-pin node. ROM supports asynchronous boot. May be connected to USB port C for IDE operations.
	708.1	79	J23.12	Tx Out	
GPIO	705.17	85	J32.4	Data In	General purpose 4-pin node. If 705.17 is low on reset, ROM will attempt SPI memory boot using signal assignments shown, driving signals on 705.5, 3, 1, and will leave these in output mode unless programmed otherwise.
	705.5	84	J32.5	Data Out	
	705.3	81	J32.6	Chip Enable-	
	705.1	80	J32.7	Clock	
GPIO	100.17	20	J30.14	General purpose 1-pin nodes. No special ROM or interconnections.	
	200.17	18	J30.13		
	500.17	7	J30.5		
	600.17	6	J30.4		
	317.17	52	J36.10		
	417.17	59	J36.3		
Analog In	709.ai	76	J32.9	Analog nodes whose I/O is powered by separate $V_{DD}A$ bus.	
Analog Out	709.ao	77	J32.8		
Analog In	713.ai	73	J32.10		
Analog Out	713.ao	72	J32.11		
Analog In	717.ai	69	J32.14		
Analog Out	717.ao	70	J32.13		
GPIO	715.17	71	J32.12	General purpose 1-pin node whose pin is shared (read only) by the above analog nodes and may be used by them for timing or other purposes.	
Analog In	617.ai	61	J36.1	Analog node whose I/O is powered by $V_{DD}I$ bus.	
Analog Out	617.ao	63	J32.1		
GPIO	517.17	60	J36.2	General purpose 1-pin node whose pin is shared (read only) by Analog 617.	
Analog In	117.ai	48	J36.13	Analog node whose I/O is powered by $V_{DD}I$ bus.	
Analog Out	117.ao	50	J36.12		
GPIO	217.17	51	J36.11	General purpose 1-pin node whose pin is shared (read only) by Analog 117.	
Input	RESET-	88	J22.2	Reset signal, active low. Also pins J22.4 and 6.	
Power	$V_{DD}C$	5	J14.2	Core power bus. Powers F18A computers, and parts of I/O circuitry (such as registers) that are internal to them.	
		17			
		29			
		41			
		49			
		62			
		75			
		83			
Power	$V_{DD}I$	4	J15.2	I/O power bus. Powers I/O pads including the parts of the I/O circuitry collocated with the pads. Includes analog pads for nodes 117 and 617.	
		19			
		28			
		40			
		47			
		64			
		82			
Power	$V_{DD}A$	74	J16.2	Analog power bus for pads of nodes 709, 713 and 717.	
Ground	GND	DAP	any gnd	Common ground and heat sink.	

8.2 Connector Pinouts

8.2.1 Power Control Section

External Connector

Pin 1 of J1 is oriented toward the bottom edge of the board and thus is an exception to the rule.

J1

10	Gnd
9	User supply, J4
8	Gnd
7	User supply, J5
6	Gnd
5	User supply, J6
4	Gnd
3	External Host Pwr
2	Gnd
1	External Target Pwr

Single Pins

J4	User supply, J1.9
J5	User supply, J1.7
J6	User supply, J1.5

Host Power Select

J10

1	External Host Pwr
2	V_{DD}C to Host
3	Main 1.8v Bus

J11

1	External Host Pwr
2	V_{DD}I and A to Host
3	Main 1.8v Bus

Target Power Select

J14

1	External Target Pwr
2	V_{DD}C to Target
3	Main 1.8v Bus

J15

1	External Target Pwr
2	V_{DD}I to Target
3	Main 1.8v Bus

J16

1	External Target Pwr
2	V_{DD}A to Target
3	Main 1.8v Bus

8.2.2 USB Serial Interfaces

Port Data Connections to Host and Target

J23

Port A In	1	2	Host 708.17
Port A Out	3	4	Host 708.1
Port B In	5	6	Host 200.17
Port B Out	7	8	Host 100.17
Port C In	9	10	Target 708.17
Port C Out	11	12	Target 708.1

Port A Access

J7	FTDI 3.3v Pwr

J8

1	DTR signal
2	CBUS2
3	CBUS3
4	CBUS4

Port B Access

J12	FTDI 3.3v Pwr
J24	RTS signal

J13

1	DTR signal
2	CBUS2
3	CBUS3
4	CBUS4

Port C Access

J19	FTDI 3.3v Pwr

J17

1	DTR signal
2	CBUS2
3	CBUS3
4	CBUS4

8.2.3 Host Chip

Probe Points

CE-	SRAM chip enable from 008.1
WE-	SRAM write enable from 008.3
D00	SRAM data bit
A00	SRAM address bit
SS-	Chip select for SPI Flash chip
SCK	Clock line for SPI bus (selectively enabled to the SD socket)
DO	Data out bus from G144 to SPI devices
DI	Data in bus from SPI devices to G144

Reset and Boot

J20

Host RESET pin	1	2	Host RESET pin
USB A RTS signal	3	4	Host reset ckt & J25.3

J25

1	Ground
2	SPI Flash RST- pin
3	Host reset ckt & J20.4

J26

1	Host 705.17
2	1K Pull-up to 1.8v

SPI Bus Expansion

J39

1	Host 600.17
2	FLASHENABLE-
3	Ground

J37

FLASHENABLE- on SPI bus.	1	2	2 inputs to NAND. Output low enables MMC on SPI bus.
	3	4	

Uncommitted Host Pins

J21

1	617.ao
2	617.ai
3	517.17
4	417.17
5	317.17
6	217.17
7	117.ao
8	117.ai

J27

1	Ground
2	709.ao
3	709.ai
4	713.ai
5	713.ao
6	715.17
7	717.ao
8	717.ai

8.2.4 Target Chip

Probe Points

S17	SERDES Clock between Host and Target
S1	SERDES Data

Reset and Host Communication

J22

Host 500.17	1	2	Target RESET- pin
USB C RTS signal	3	4	
Target reset circuit	5	6	

J35

1	Host 300.17
2	Target 300.17

J34

1	Host 300.1
2	Target 300.1

Uncommitted Target Pins

J30

d00	1	2	d01
d02	3	4	600.17
500.17	5	6	d03
d04	7	8	d05
d06	9	10	d07
d08	11	12	d09
200.17	13	14	100.17
d10	15	16	d11

J31

d12	1	2	d13
d14	3	4	d15
d16	5	6	d17
008.17	7	8	008.5
008.3	9	10	008.1
a17	11	12	a16
a15	13	14	a14
a13	15	16	a12

J32

617.ao	1	2	a03
a02	3	4	705.17
705.5	5	6	705.3
705.1	7	8	709.ao
709.ai	9	10	713.ai
713.ao	11	12	715.17
717.ao	13	14	717.ai
a00	15	16	a01

J36

617.ai	1	2	517.17
417.17	3	4	a04
a05	5	6	a06
a07	7	8	a08
a09	9	10	317.17
217.17	11	12	117.ao
117.ai	13	14	a10
a11	15	16	Ground

J28

Ground	1	2	701.17 SERDES clock
	3	4	701.1 SERDES data

8.2.5 Prototyping Area

SD/MMC Socket Signals

SD Socket signals	J38	J40	*SPI Bus signals*
CLK/SCLK	1	1	SPI CLK MMC
DAT3/CS-	2	2	SPI CS- MMC
CMD/SI	3	3	SPI DO
DAT0/SO	4	4	SPI DI
V_{DD}	5	5	1.8v

J33	*SD Socket Signals*
1	DAT1
2	DAT2
3	Card Present
4	Write Protect

TI TXB0108 Level Shifterss

Each level shifter is surrounded by this hole pattern:

A2	$V_{CC}A$	A1	B1	$V_{CC}B$	B2
A3					B3
A4					B4
A5					B5
A6					B6
A7	A8	OE	V_{SS}	B8	B7

Convenience Logic

TP4	NAND 1 Input
TP5	NAND 1 Input
TP11	NAND 1 Output
TP6	NAND 2 Input
TP7	NAND 2 Input
TP12	NAND 2 Output
TP8	NAND 3 Input
TP9	NAND 3 Input
TP13	NAND 3 Output
TP2	OR Input
TP3	OR Input
TP10	OR Output

DB9 RS232 site Left (J52)

J54

1	RX Incoming
2	TX Outgoing
3	RTS Incoming

Note these signals are on chip side of minimal quasi-RS232 transceiver.

General Purpose LEDs

J57

1	V_{DD} for D12
2	V_{DD} for D13
3	V_{DD} for D14
4	V_{DD} for D15

DB9 RS232 site Right (J58)

J59

1	RX Incoming
2	TX Outgoing
3	RTS Incoming

Note these signals are on chip side of minimal quasi-RS232 transceiver.

VGA site (J70)

J67

1	RED
2	GREEN
3	BLUE
4	HSYNC
5	VSYNC
6	gnd

USB site (J71)

J68

1	V_{CC}
2	D+
3	D-

RJ48 site (J69)

J66

1	TX+
2	TX-
3	RX+
4	RX-
5	n/c

Audio site (J62, 63, 64)

J65

1	RING
2	NC TIP SWITCH
3	TIP
4	SLEEVE

J60

1	RING
2	NC TIP SWITCH
3	TIP
4	SLEEVE

J61

1	RING
2	NC TIP SWITCH
3	TIP
4	SLEEVE

SMA RF site (J41, 49, 51, 55)

J48

1	J41 Signal
2	Gnd

J50

1	J49 Signal
2	Gnd

J53

1	J51 Signal
2	Gnd

J56

1	J55 Signal
	Gnd

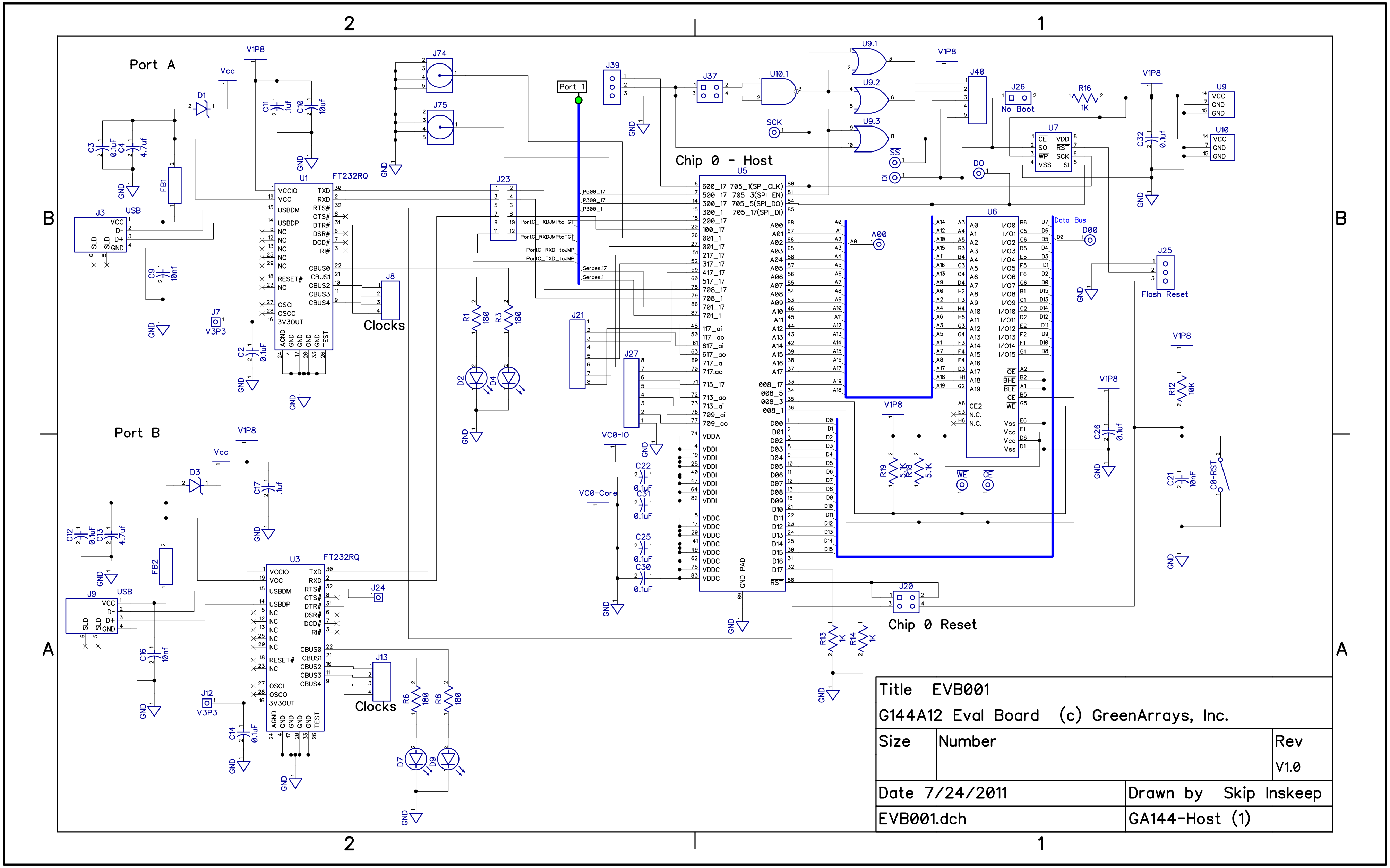
8.3 Problems and Solutions

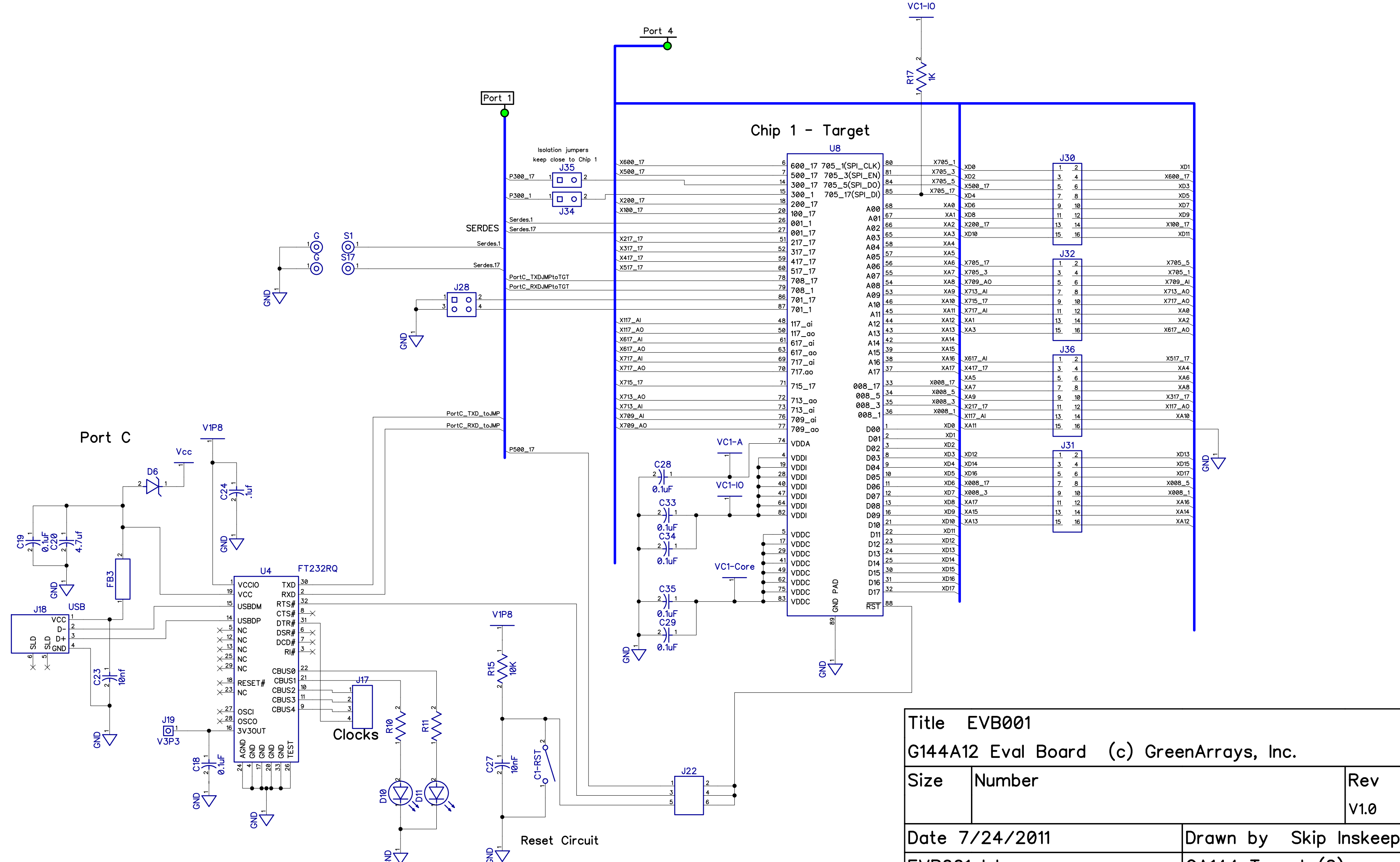
There are no known problems with this board, hence no rework or workarounds are listed here.

8.4 Schematics and Layout

The following nine pages may be used to print or view high resolution renderings of these graphics.

Status of artwork: These are preproduction draft drawings. The schematics are complete for all practical purposes, and the layouts are complete with only minor exceptions.


Port A
Port B
Chip 0 - Host
Chip 0 Reset
Clocks
Clocks
Flash Reset
No Boot
Data_Bus
FT232RQ
FT232RQ
Title EVB001
G144A12 Eval Board (c) GreenArrays, Inc.
Size
Number
Rev
V1.0
Date 7/24/2011
Drawn by Skip Inskeep
EVB001.dch
GA144-Host (1)

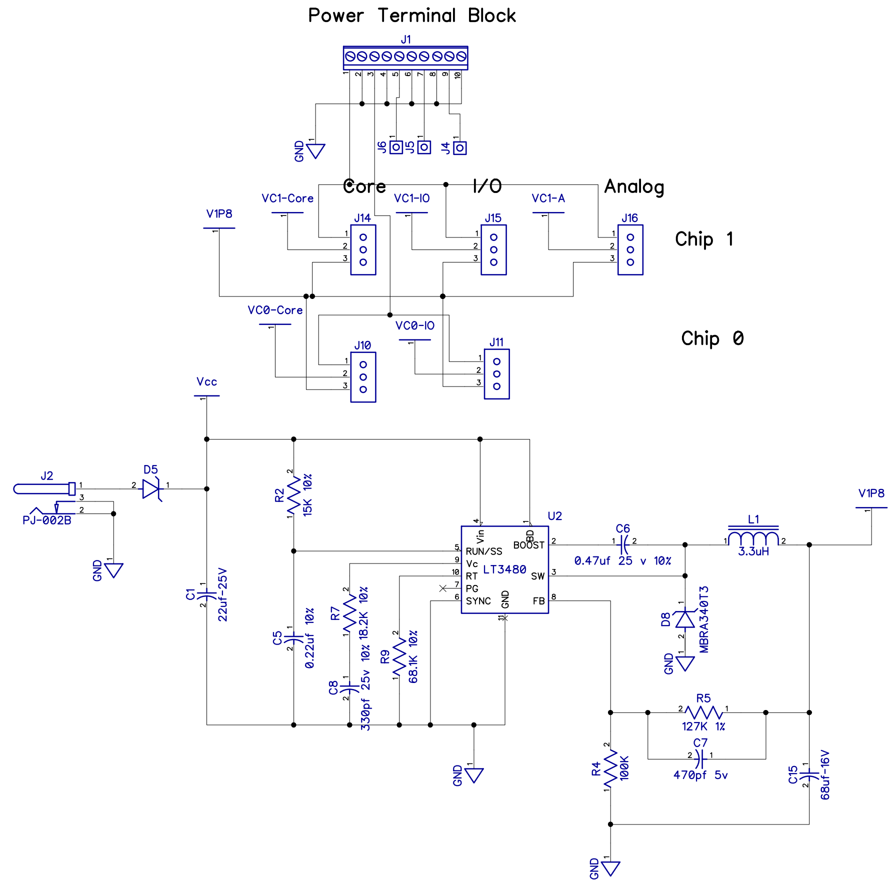


Title EVB001

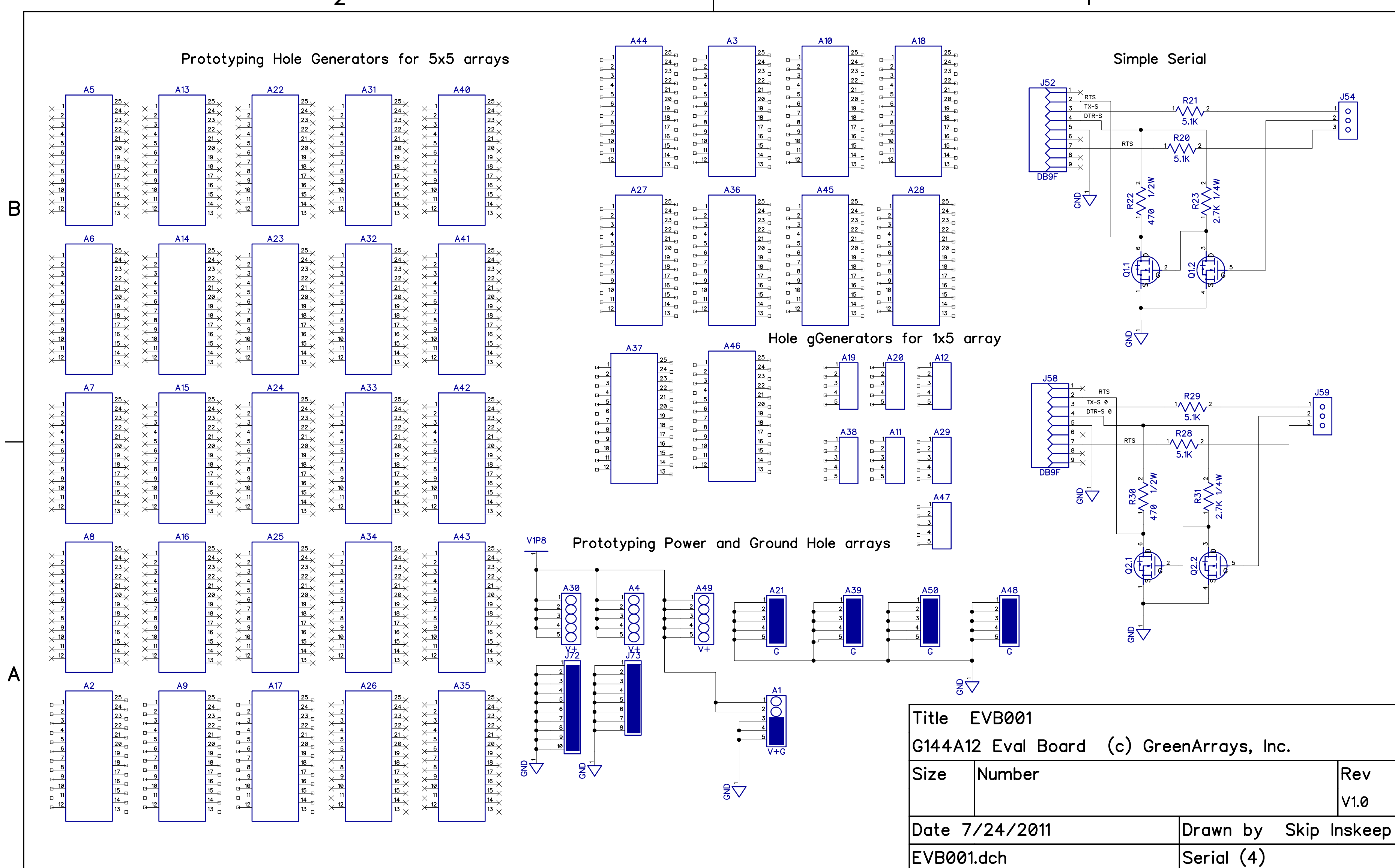
G144A12 Eval Board (c) GreenArrays, Inc.

Size	Number	Rev
		V1.0

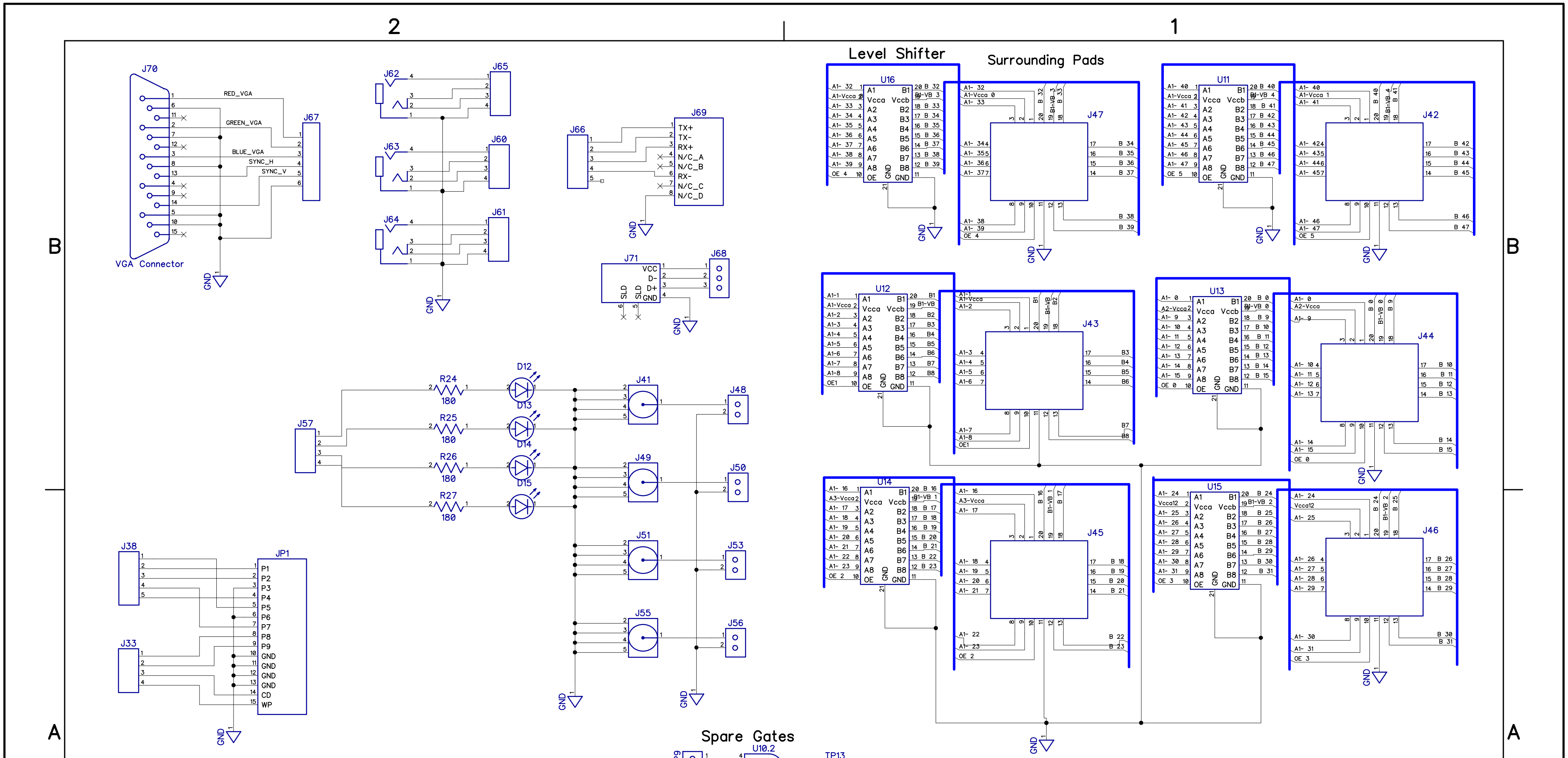
Date 7/24/2011	Drawn by Skip Inskeep
EVB001.dch	GA144-Target (2)



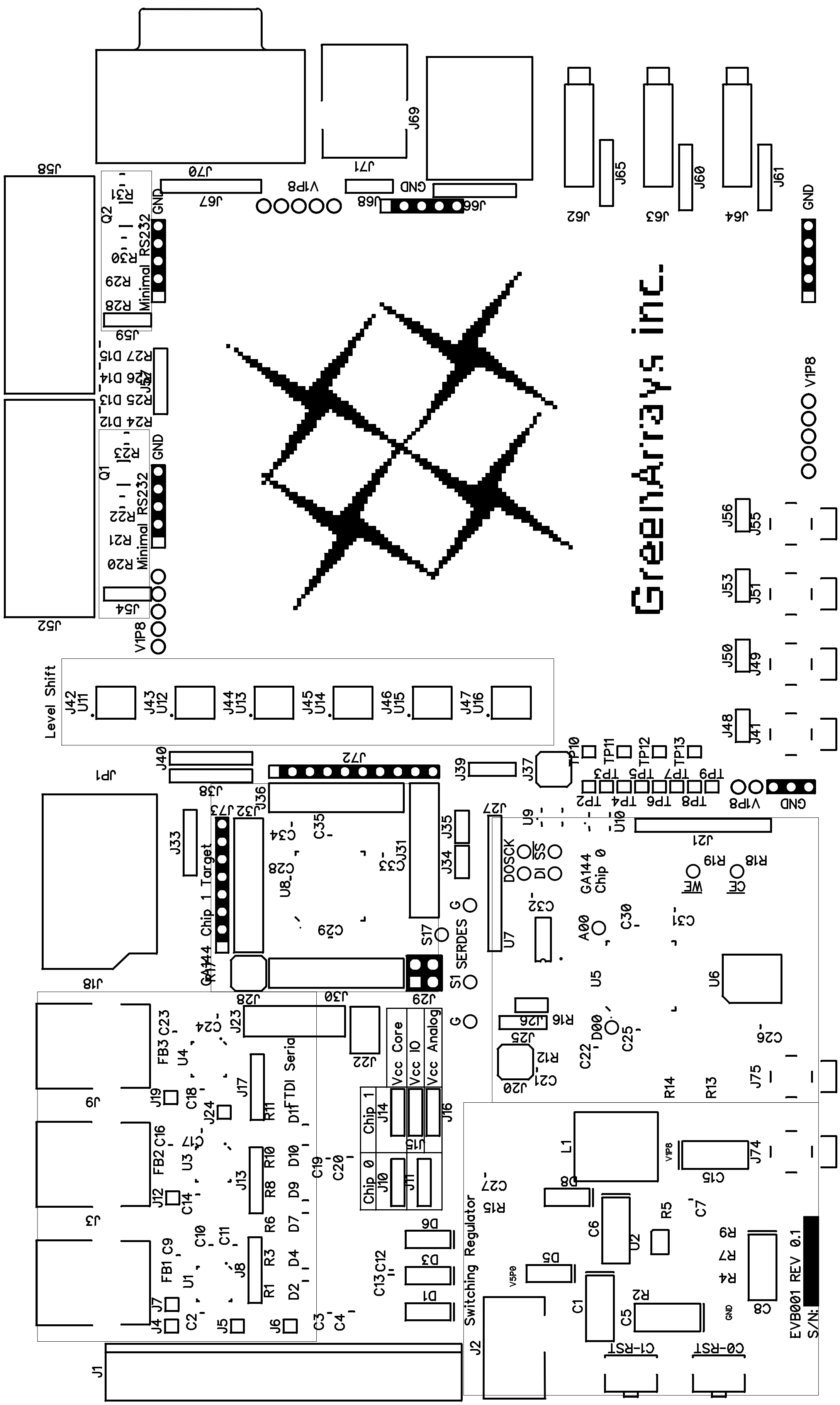
Title EVB001		
G144A12 Eval Board (c) GreenArrays, Inc.		
Size	Number	Rev V1.0
Date 7/24/2011	Drawn by Skip Inskeep	
EVB001.dch	Supply (3)	



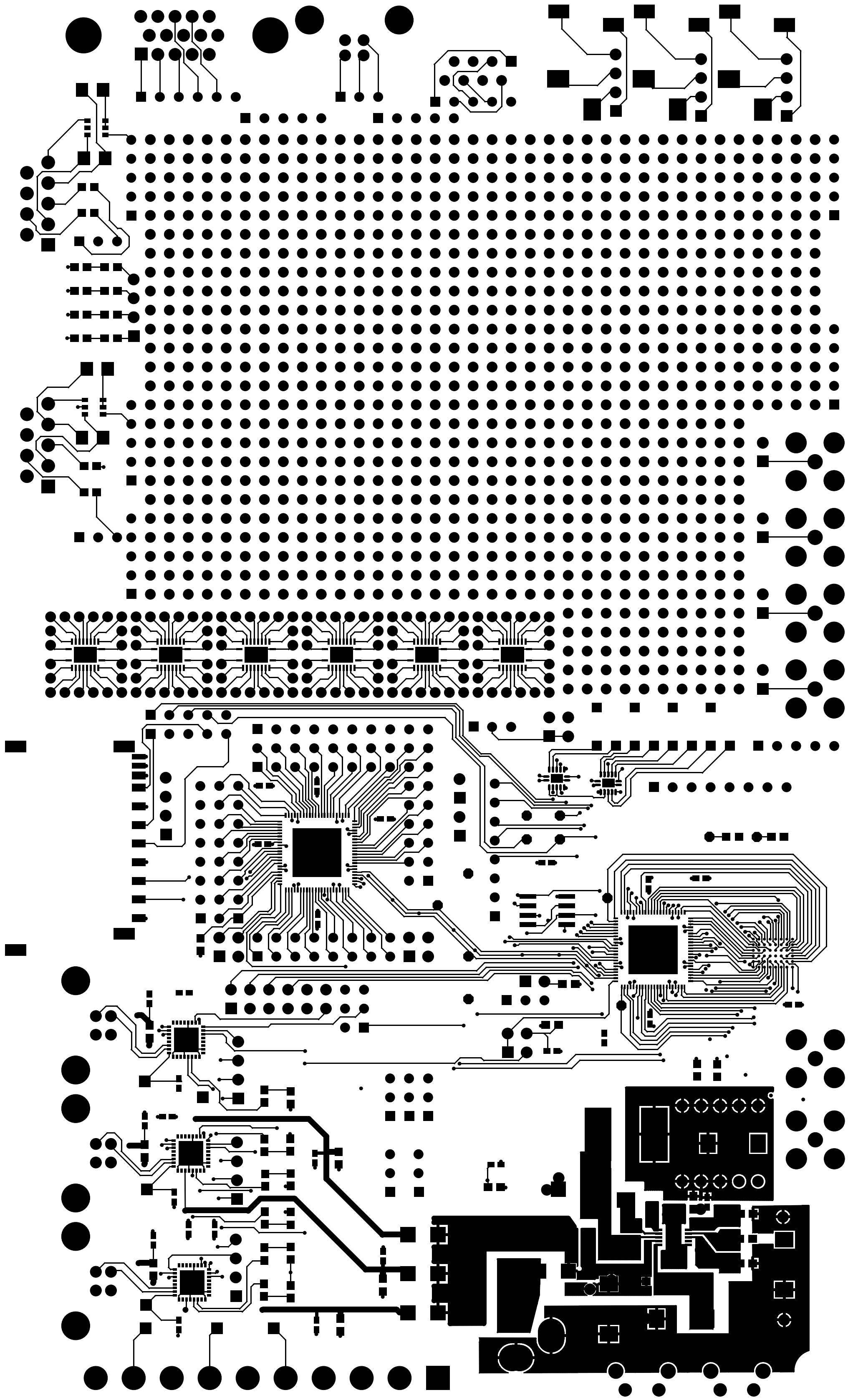
Title EVB001		
G144A12 Eval Board (c) GreenArrays, Inc.		
Size	Number	Rev V1.0
Date 7/24/2011	Drawn by Skip Inskeep	
EVB001.dch	Serial (4)	

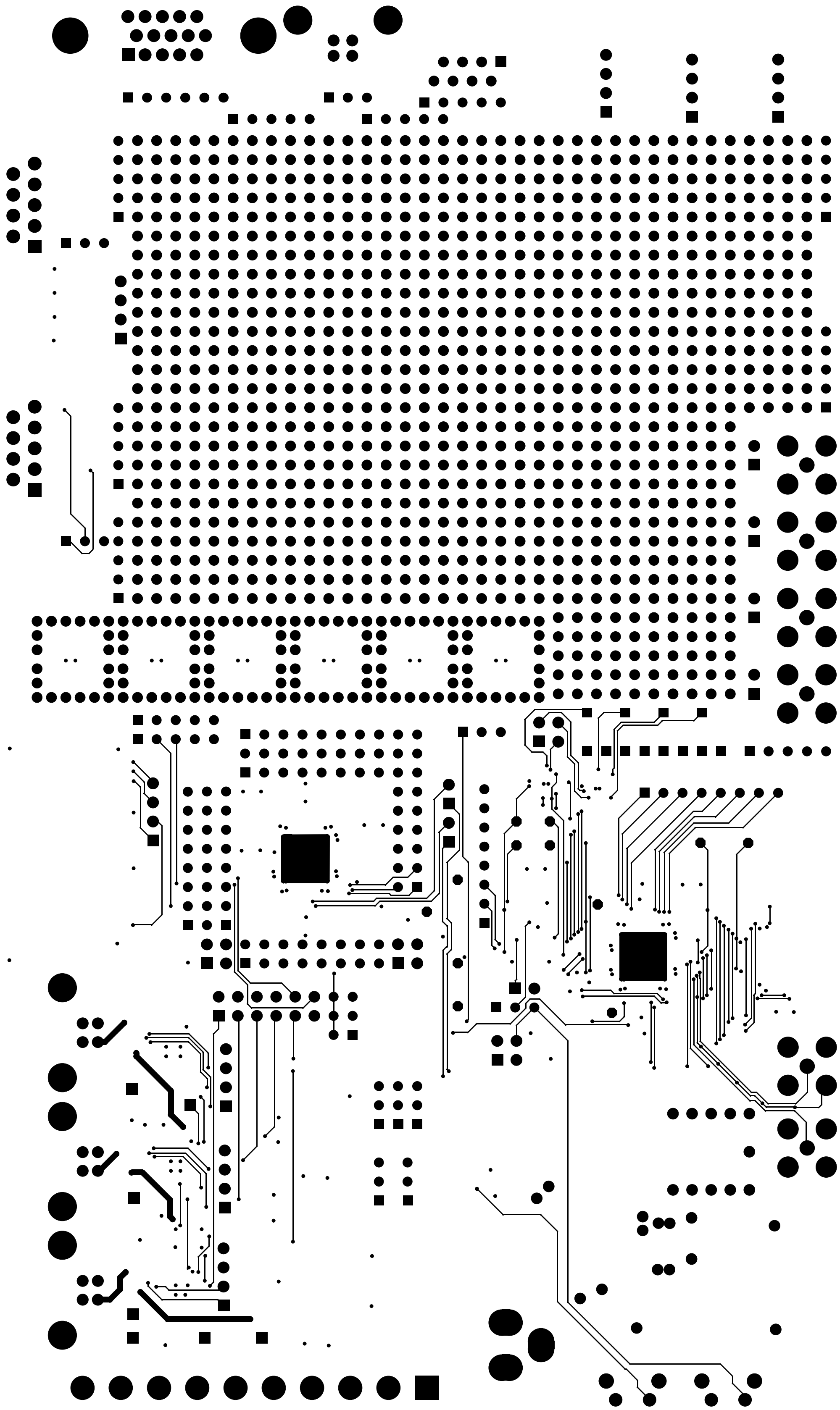


Title EVB001		
G144A12 Eval Board (c) GreenArrays, Inc.		
Size	Number	Rev V1.0
Date 7/24/2011	Drawn by Skip Inskeep	
EVB001.dch	Sheet 5	



GreenArrays inc.
EVB001 REV 0.1
S/N:
Level Shift
Switching Regulator
GA144 Chip 1 Target
GA144 Chip 0
Minimal RS232
Minimal RS232
FTDI Serial
Vcc Core
Vcc IO
Vcc Analog
Chip 1
Chip 0
SERDES
C0-RST
C1-RST
DOSCK
DI
SS
A00
D00
WE
CE
V1P8
V5P0
GND
J1
J2
J3
J9
J18
J52
J58
J69
J70
J71
JP1





9. Data Book Revision History

REVISION	DESCRIPTION
110726	Preliminary release with pre-production drawings.

Green Arrays™

Product Data Book

For more information, visit www.GreenArrayChips.com

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