1.

a. Define half adder.

- The circuit that generates to carry and sum with two given inputs is known as half adder.

b. Draw a truth table for the sum and carry of half adder.

A	B	Sum(S)	Carry(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

c. Write the sop expression from the truth table.

- The SOP for sum is $A \oplus B$ and for Carry is A.B

d. Draw the circuit using logsim.

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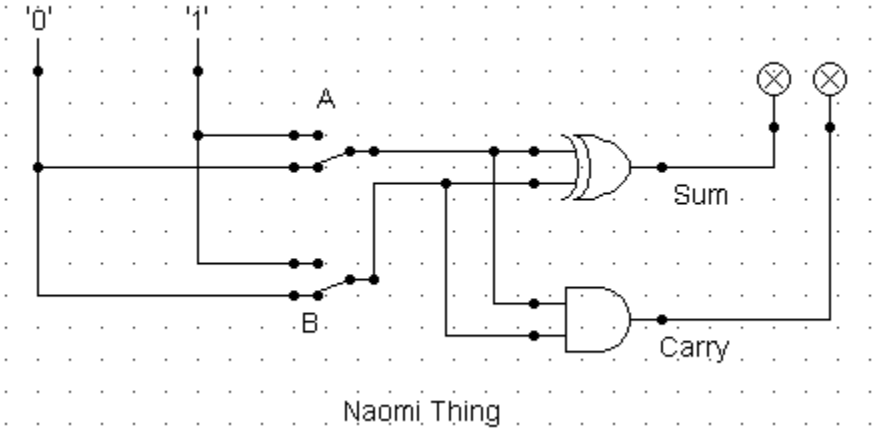

2.

a. Draw the truth table for the outputs of the full adder.

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A	B	C(in)	Sum(S)	Carry[C(out)]
0	0	0	0	0

1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

b. Write the corresponding sop expression for sum and carry of full adder and simplify the expression

-SOP expression of Sum = A'B'C+AB'C'+A'BC'+ABC
= A'(B'C+BC')+A(B'C'+BC)
=A'(B⊕C)+A(B⊕C)'
let B⊕C=X
so;
=A'X+AX'
=A⊕X
=A⊕B⊕C

- SOP expression of Carry = A'BC+AB'C'+ABC
= A'BC+ABC+AB'C+ABC+ABC'+ABC
=BC(A'+A)+AC(B'+B)+AB(C'+C)
=AB+BC+AC

c. Draw full adder using two half adder and an OR gate.
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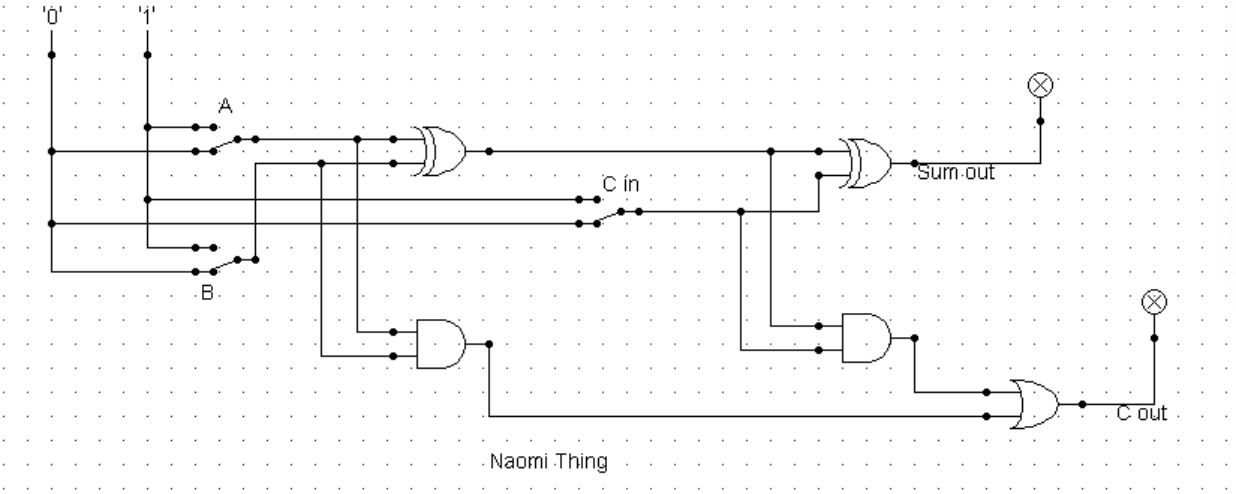

3. Using the three stages of design, construct the circuits for the following input /output values. Here A, B and C are the inputs whereas D, E, F, G, H and I are outputs. *Note: Draw circuit diagram using logsim corresponding to the simplified expression of outputs D, E, F, G, H and I.*

A	B	C	D	E	F	G	H	I
0	0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	0	1
0	1	0	1	0	1	1	1	1
1	0	0	1	0	0	1	0	1
1	1	1	1	1	1	1	1	1
1	1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	1	0
0	1	1	0	0	0	1	1	1

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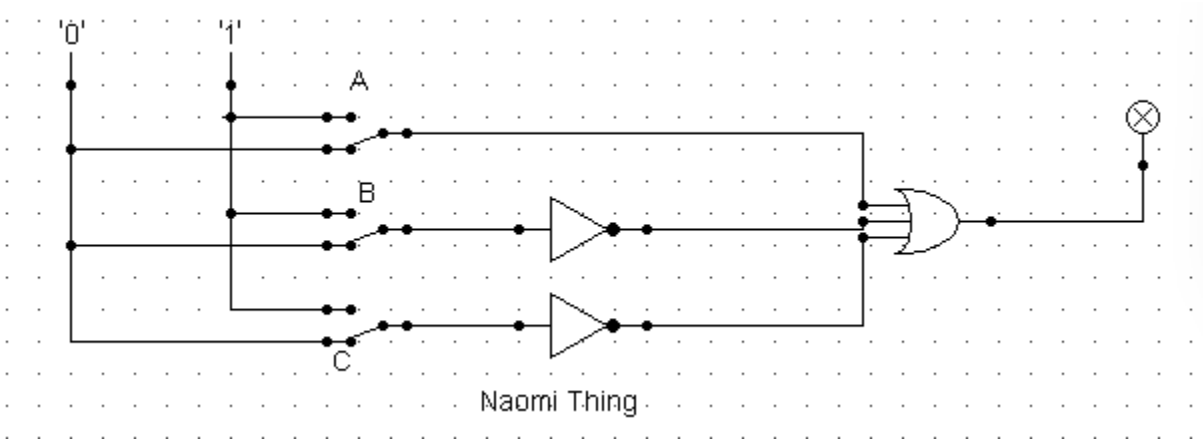
ans:

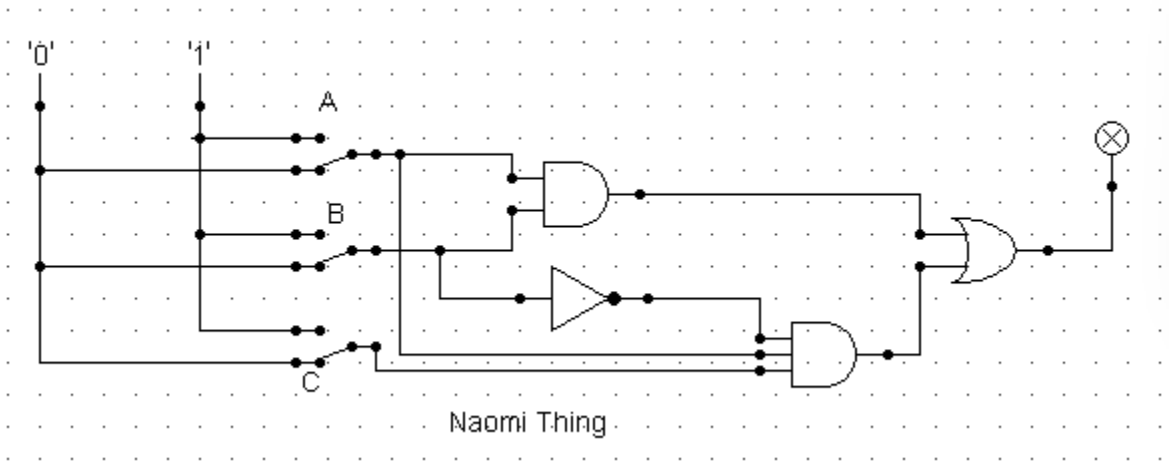
POS of D=A+B'+C'



SOP of E=ABC+ABC'+AB'C

=AB(C+C')+AB'C

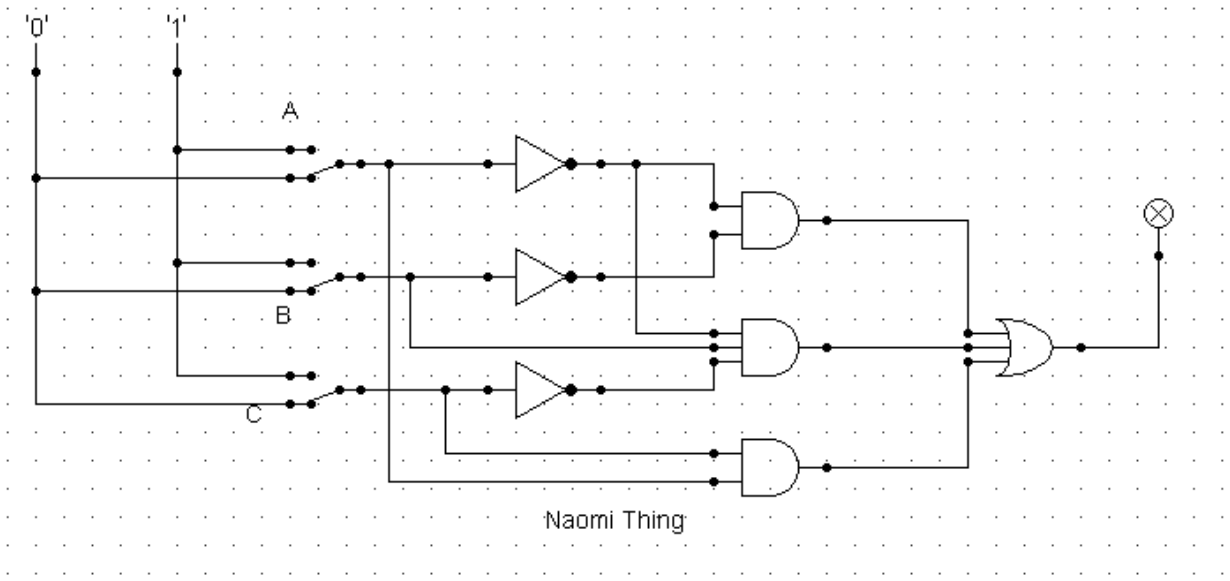
=AB+AB'C



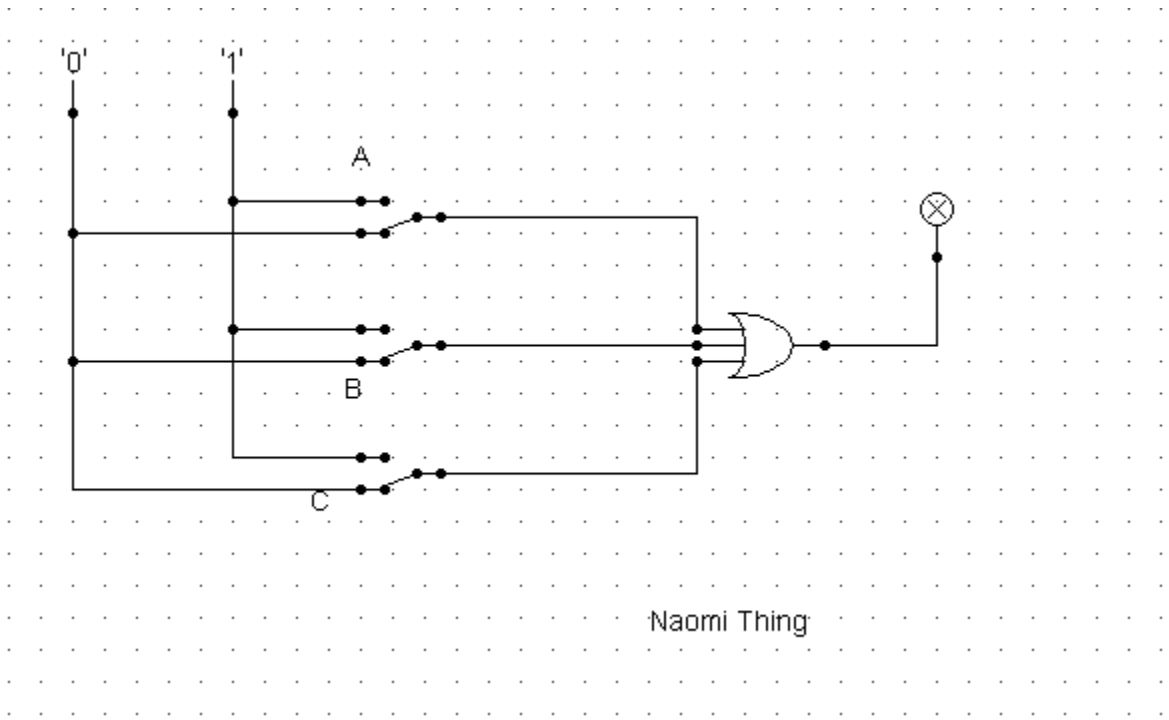
SOP of F = A'B'C'+A'B'C+A'BC'+ABC+AB'C

=A'B'(C'+C)+A'BC'+AC(B+B')

=A'B'+A'BC'+AC



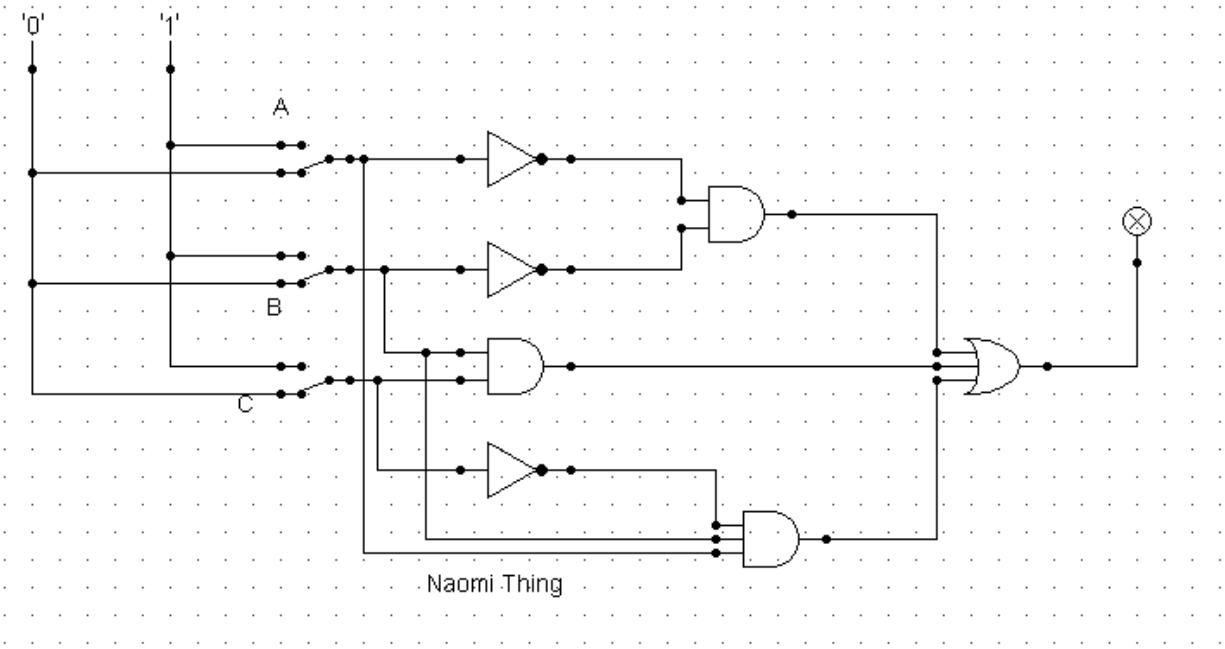
POS of G =A+B+C



SOP of H = A’B’C’+A’BC’+ABC+AB’C+A’BC

= A’C’(B’+B)+BC(A+A’)+AB’C

=A’C’+BC+AB’C



POS of I = A'+B+C'