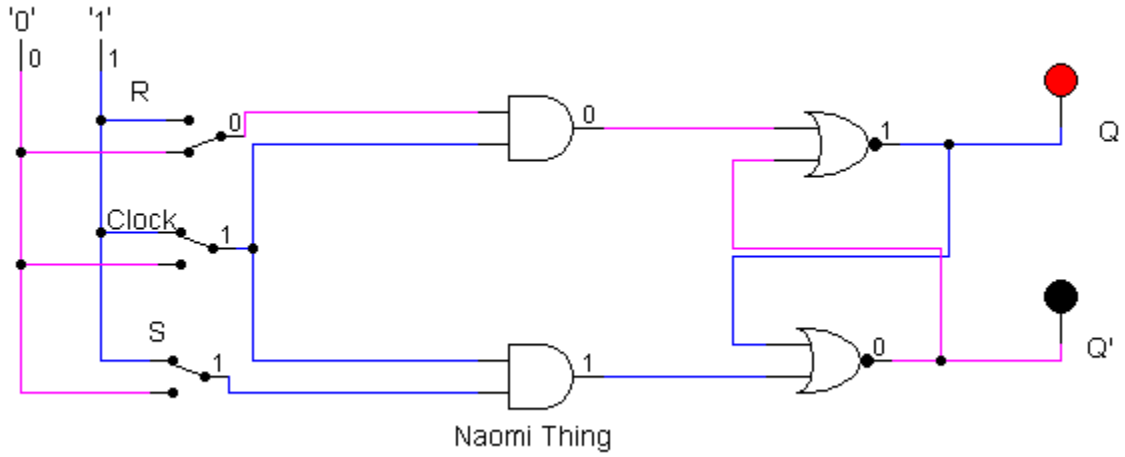
Naomi Thing

Instruction:

Complete all questions in **1 hour.**

1. What is flip flop? Describe the working mechanism RS flip flop.

= A device which stores the single bit of binary digit of data is known as flip flop.



= When the R and S have 0 (low), it shows the previous memory but when there is no previous operation it toggles.

Case 1:

When S=0 and R=1, we get the values Q=0 and Q'=1. This output is derived from the concept of NOR gate.

Case 2:

When S=0 and R=1, we get the values Q=1 and Q'=0. This output is also derived from the truth table of NOR gate.

Case Forbidden State:

When we provide both S and R as 1, we get both Q and Q' 0. This case is not possible as the Q and Q' cannot be same in any moment. Thus this is known as Forbidden State.

S	R	Q	Q'	Cases
0	0	X	X	Previous Output
0	1	0	1	Case 1
0	0	0	1	Memory
1	0	1	0	Case 2
0	0	1	0	Memory
1	1	X	X	Forbidden State

2. Construct the timing diagram for half adder and half subtractor, full adder.

= **Half Adder:**

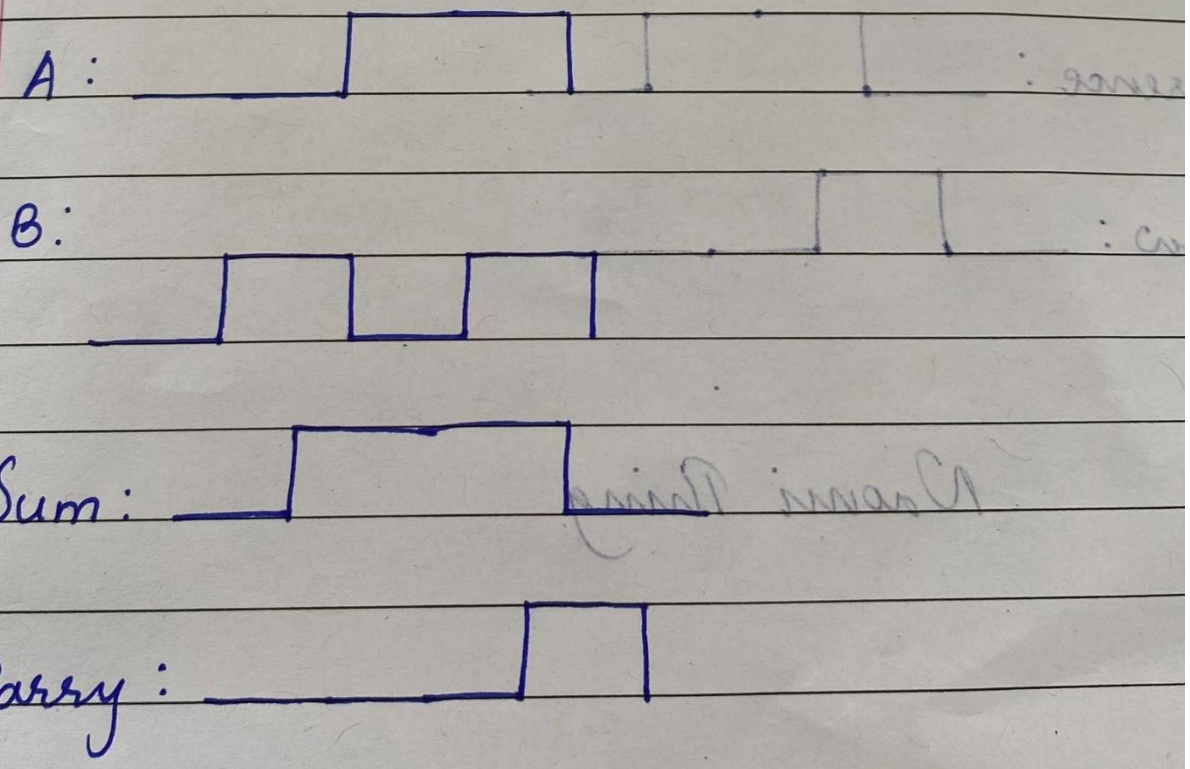
Naomi Thing

*. Half-adder:

→ Truth-Table:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

→ Timing-diagram:



Naomi Thing

Naomi Thing

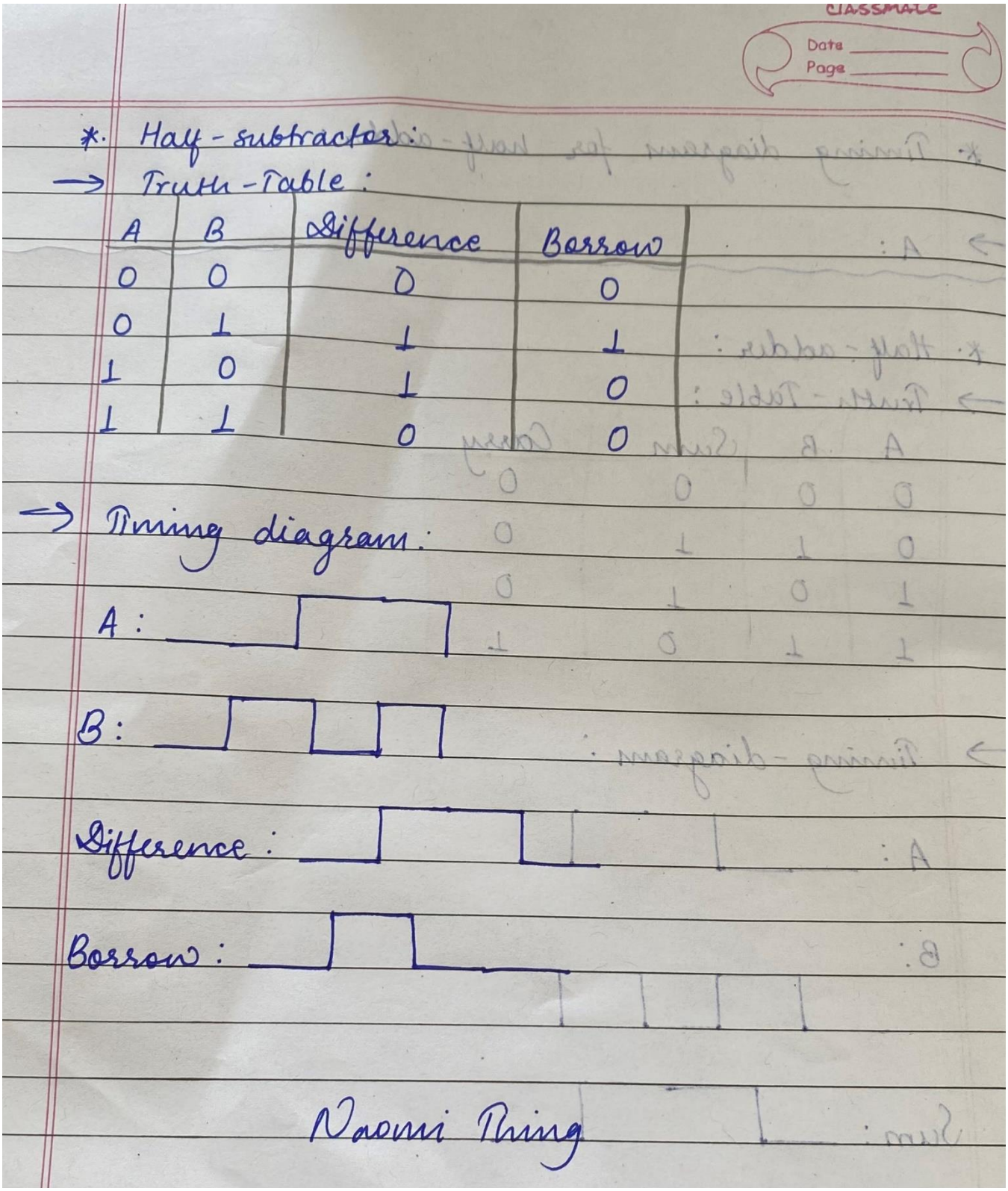
Half Subtractor:

*. Half-subtractor:

→ Truth-Table:

A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

→ Timing diagram:



Full Adder:

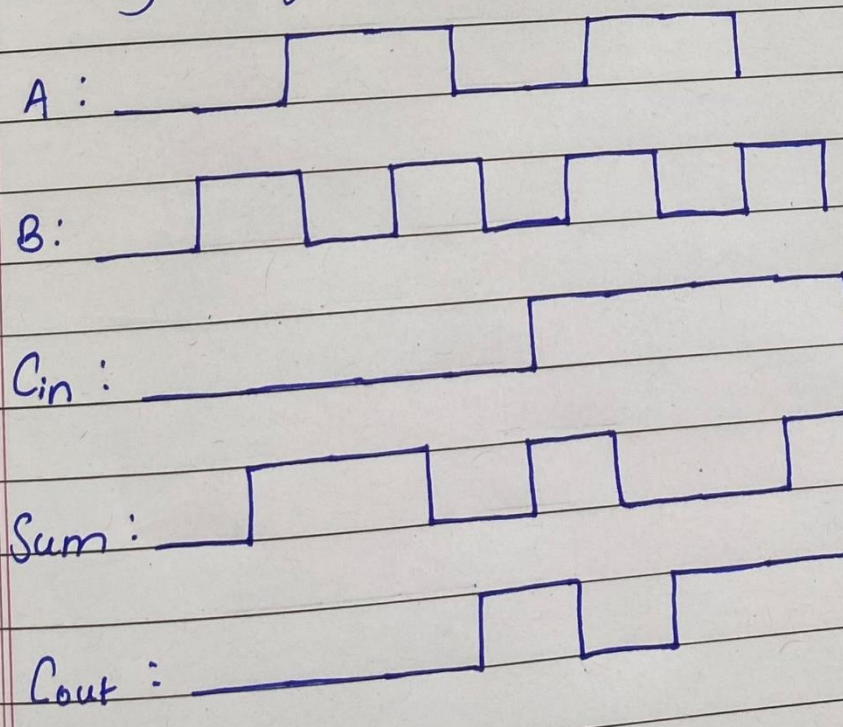
Naomi Thing

* Full-Adder :

→ Truth Table :

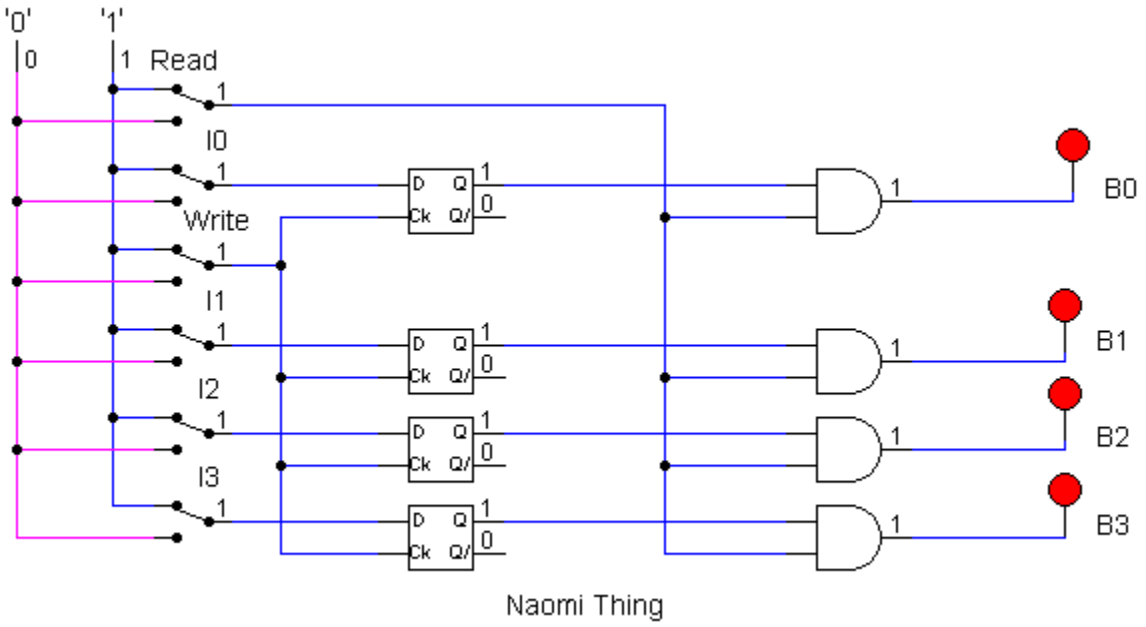
A	B	Carry in (Cin)	Sum	Carry out (Cout)
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

→ Timing diagram :



Naomi Thing

3. Describe the working mechanism of 4-bit register by constructing the circuit using D flip flop.



= Working Mechanism of 4-Bit register: a 4-bit register is a machine that can process and store 4 bits of data. Here, a D flip flop is used to build it. The device that can store one bit of data is a D flip flop. The write-stored D flip flop featured D inputs (I0, I1, I2 AND I3). To load data into the register, the clock signal is reduced in level. The clock signal is then raised to the high level to transfer data outputs (B0, B2, B3, B4). Until new data is added, it retains the previous data.

4. Differentiate between:
   a) Flip flop and Latch

Flip Flop	Latch
- A flip flop is triggered by a clock signal. - Flip flops are used for synchronous data storage and transfer. - Flip flops typically have two inputs. - Flip flops are less prone to race conditions because they are triggered by a clock signal.	- Latch is triggered by an enable signal. - Latches are used for asynchronous data storage and transfer. - Latches have two or more inputs. - Latches can experience race conditions if the enable signal changes while the data is being transferred.

   b) Combinational circuit and Sequential circuit

Combinational Circuit	Sequential Circuit
- It performs logical operations on input signals to produce output signals. - They are made up of logic gates, which are connected in a specific way to perform a specific function. - Combinational circuits do not have a state transition. - This circuits are used in a variety of applications, including logic gates, adders, and decoders.	- They store and process data over time. - They are made up of memory elements, such as flip-flops or latches, which store and process data. - Sequential circuit can have state transitions based on the input signals and the current state of circuit. - This circuits are used in applications that require data storage and processing, such as counters, registers, and state machines.

c) SIPO and PISO shift register

SIPO shift register	PISO shift register
- SIPO (Serial In, Parallel Out) shift register has a data shifted in serially and shifted out in parallel. - This register has a single input for serial data. - SIPO shift register has multiple outputs for parallel data. - In this shift register, data is transferred from one flip-flop to the next by the clock signal.	- PISO (Parallel In, Serial Out) shift register, data is shifted in in parallel and shifted out serially. - This register has multiple inputs for parallel data. - PISO shift register has a single output for serial data. - In this shift register, data is transferred from the flip-flop to the output by the clock signal.