Instruction:

Complete all questions in 1 hour.

1. Which one is the characteristic of Harvard Architecture?
   A. Program and Data stored in Separate Memory
   B. Program and Data stored in the same Memory
   C. Program and data stored in Cache Memory
   D. All of the Above
2. Which of the following is the working cycle of the CPU?
   A. Decode, Execute, Fetch
   B. Fetch, Decode, Execute
   C. Fetch, Execute, Decode
   D. All of the Above
3. Any condition that causes a processor to stall is called _____
   A. Hazard
   B. Page fault
   C. System error
   D. None of the mentioned
4. What does the control unit generate to control other units?
   A. Transfer signals
   B. Command Signal
   C. Control signals
   D. Timing signals
5. What must the processors of all computers have?
   A. Control unit
   B. ALU
   C. Register
   D. All of these
6. Which is the fastest memory in the computer?
   A. Cache
   B. RAM
   C. Register
   D. Hard disk

7. With the help of _____, we reduce the memory access time:
   A. SDRAM
   B. Cache
   C. Heaps
   D. Higher capacity RAMs

8. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
   A. ISA
   B. ANSA
   C. Super-scalar
   D. All of the mentioned
9. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____
   A. Super-scaling
   B. Pipe-lining
   C. Parallel Computation
   D. None of the mentioned
10. A 24 bit address generates an address space of _____ locations.
   A. 1024
   B. 4096
   C. 2^{48}
   D. 16,777,216
11. The USA contains about 3100 counties. Suppose you have a table that stores, for each county, its name (up to 40 characters in 8-bit ASCII), its state (a two-letter code), its population, and its median income (both as 32-bit numbers). How much space would the whole database take in memory?

Name	State	Population	Median
4 characters in 8 bits 40*8=320	2 letters in 8 bit 2*8=16	32 bit	32 bit

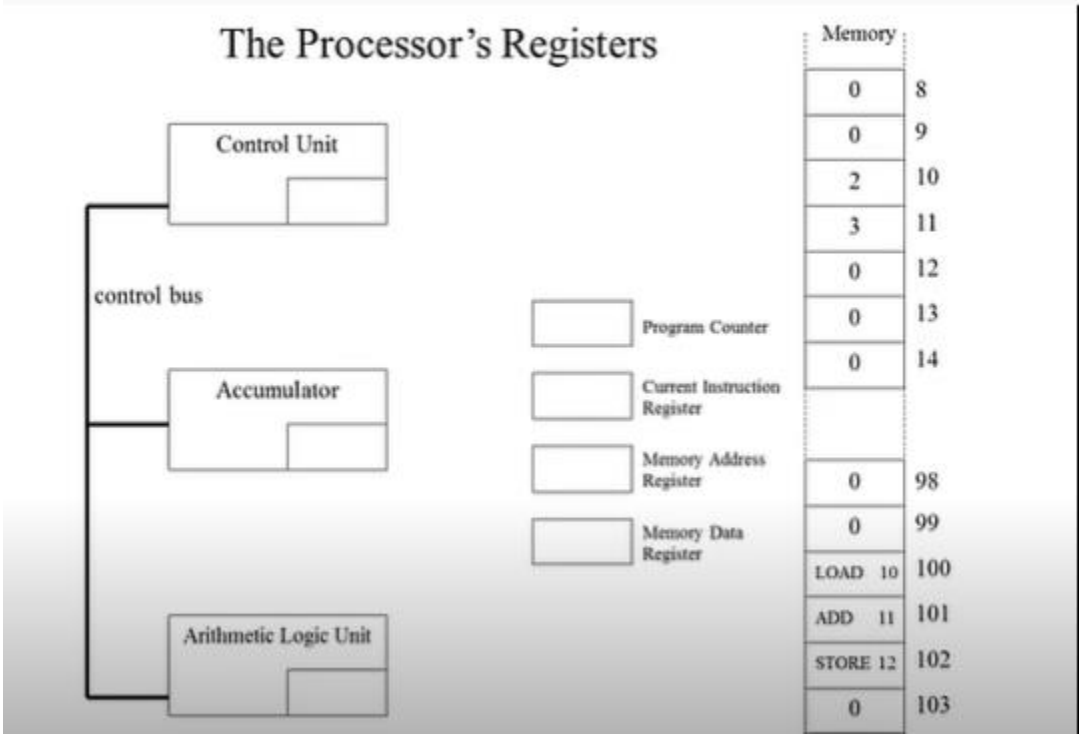
For 1 country = 320+16+32+32
= 400 bits
Total memory by 3100 countries = 400*3100

=1240000bit
= 1240000/8*1024

12. The computer has a maximum addressable memory of 16 Gigabytes. Its address bus width is 32.
    a) Calculate the width of the data bus.
    total memory = 16Gb
    width of address bus=32 byte
    width of data bus=x(let)
    total memory=2^width of address bus*x
    $16Gb=2^{32}x$
    Or, $16*2^{30}=2^{32}*x$
    Or, $2^4*2^{30}=2^{32}*x$
    Or, $2^{34}/2^{30}=x$
    Or, $x=2^2$
    Or, x=4

    b) State the effect that adding one new line to the address bus would have on the maximum addressable memory.
    Width of the address bus=32+1=33
    Width of data bus=4
    Total memory=$2^{33}*4$
    $=2^{33}*2^2$
    $= 2^{35}$
    $= 2^5*2^{30}$
    = 32GB

13. Explain the *Instruction cycle* of the processor by taking an example of the program
    Load: [10]
    Add : [11]
    Store: [12]



= Processor instructions are followed by the instruction cycle, sometimes referred to as fetch-decode-execute in this software. It begins by using its location to fetch data from load 2 through load 10. Additionally, after obtaining, it decodes Add 11's value, which is 3, and transmits for execution. Finally, it performs the actions by using the load 10 and 11 locations to store the instructions for the given operations into a register. So, until the program is finished running, this process is repeated for each instruction in the program.

14. Write short notes on the following topic:

a) Von Neumann and Harvard Architecture

= The Von Neumann architecture, sometimes referred to as the Von Neumann model or the Princeton architecture, is a type of computer architecture distinguished using shared memory area where the CPU can store and access both data and instructions (CPU). John Von Neumann and others put forth this architecture in the middle of the 1940s, and it formed the framework for most contemporary computers. On the other hand, the Harvard design is a computer architecture that physically

separates the signal and storage routes for data and instructions. In this architecture, the instruction and data caches on the CPU are kept apart, as are the buses used to access each type of memory. In embedded systems and microcontrollers, where the distinction between instruction and data memory might offer a performance benefit, the Harvard design is frequently utilized.

b) RISC vs CISC architecture

= RISC stands for Reduced Instruction Set Computer whereas, CISC stands for Complex Instruction Set Computer. A compact, highly optimized set of fast-executing instructions characterizes RISC architectures. As a result, the CPU becomes less complex and can process more instructions per clock cycle. Contrarily, CISC designs feature a bigger set of instructions that can handle a wider variety of jobs. These processors can be more expensive to produce because they are often more complicated and require more transistors. Overall, RISC architectures outperform CISC architectures in terms of speed and efficiency, although CISC architectures are more robust and versatile. The system being designer's particular requirements will determine which option is best.