Weekly report(3.13-3.20)

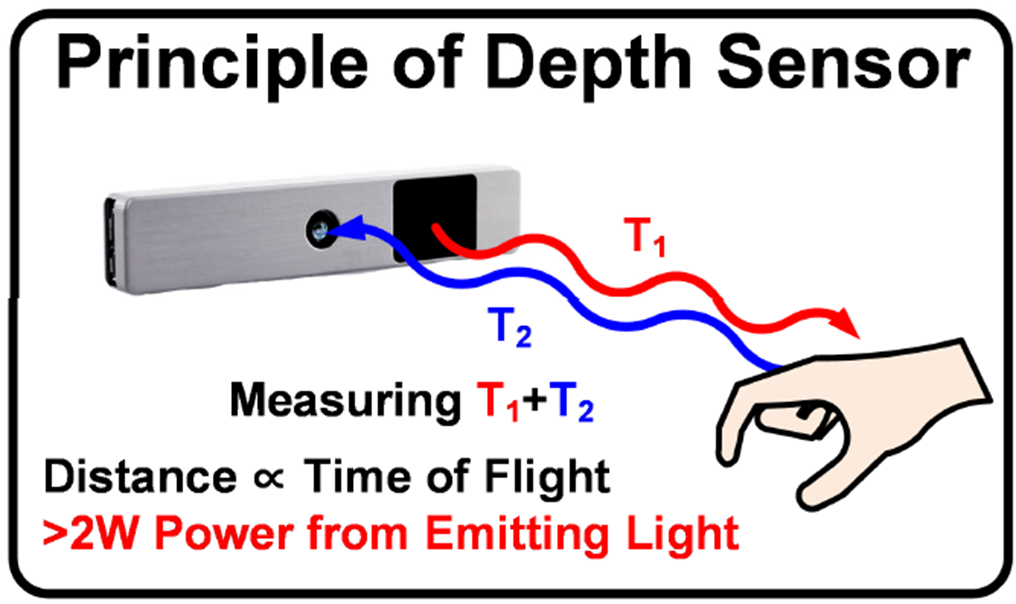
## Accomplished last week

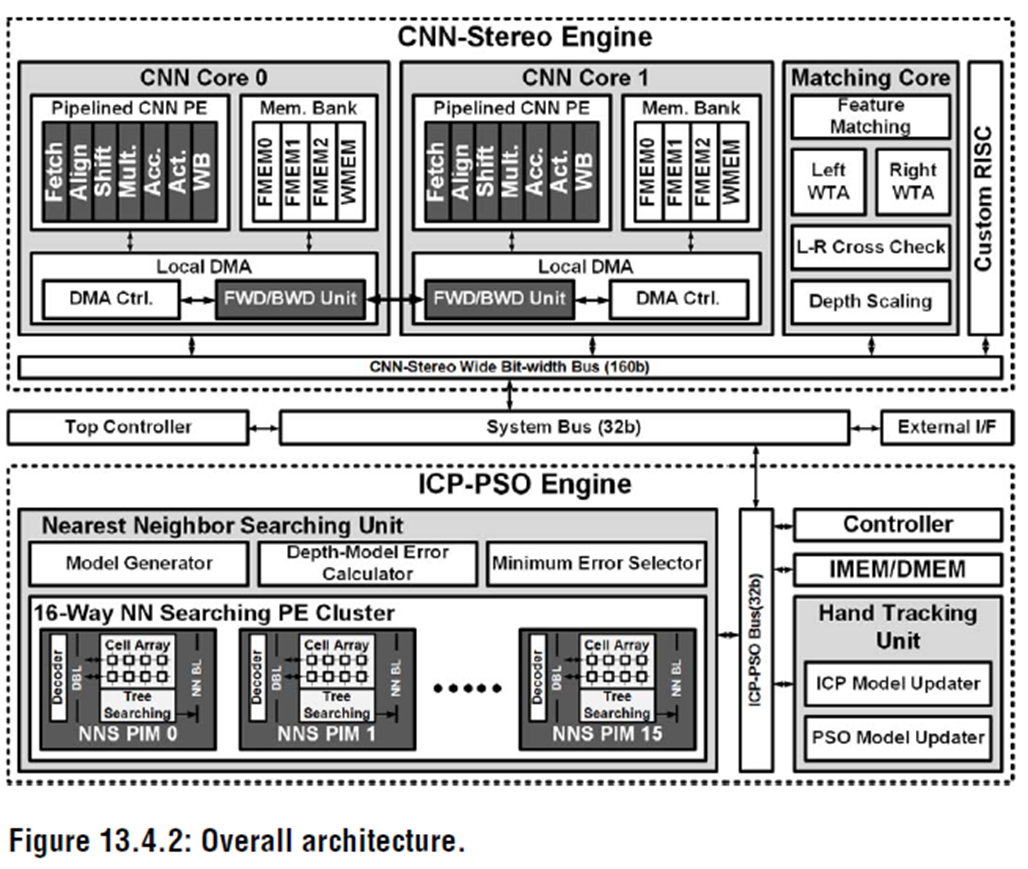
**Item 1 : Embedding Linux in FPGA research and FPGA learning**

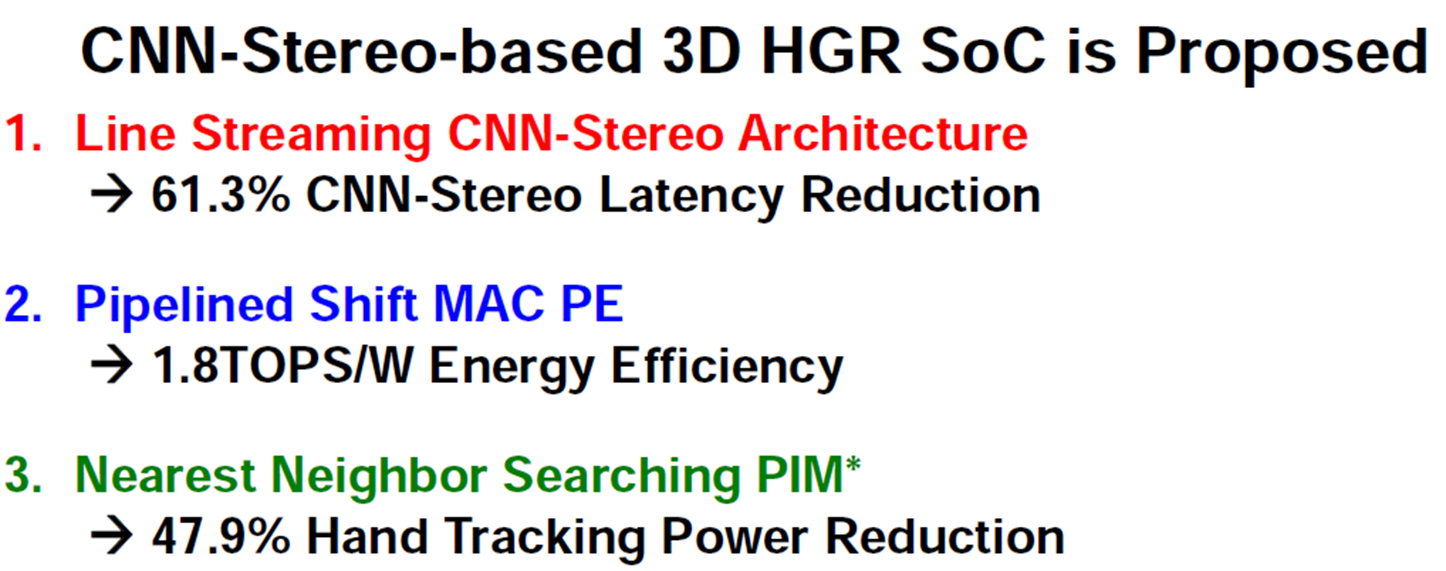
Learned some basic knowledge about FPGA and building embedded system on it , such as booting system , managing devices , address arrangement and so on .

**Item 2 : Paper Reading : A 9.02mW CNN-Stereo-Based Real-Time 3D Hand-Gesture Recognition Processor for Smart Mobile Devices**

3D hand-gesture recognition (HGR) has become an important feature in smart mobile devices. Time-of-flight (ToF) depth sensor is very power-consuming(>2W) , limiting 3D HGR operation to less than 3 hours.

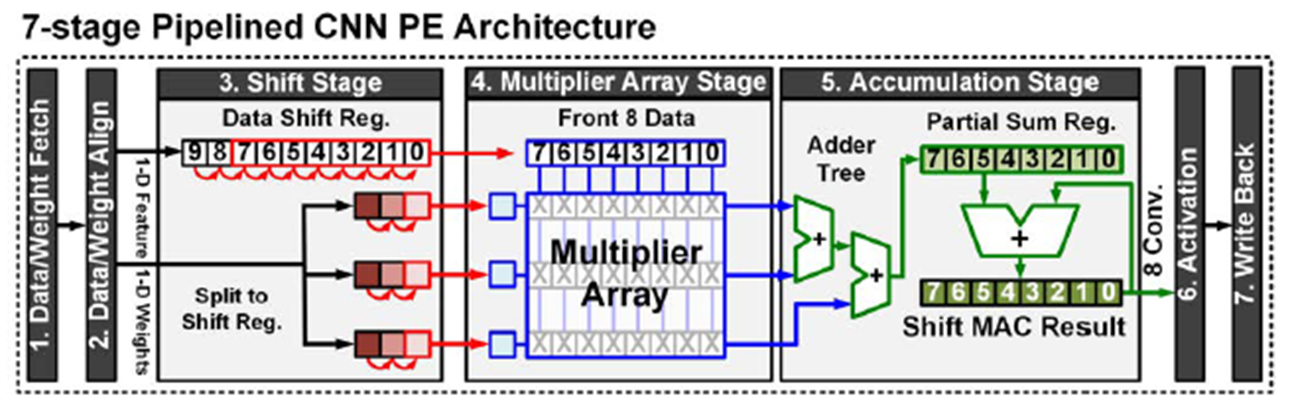


The CNN-based HGR system comprises two 6-layer CNNs (stereo) without any pooling layers to preserve geometrical information and an iterative-closest-point/particle-swarm optimization-based (ICP-PSO) hand tracking to acquire 3D coordinates of a user’s fingertips and palm from the hand depth.



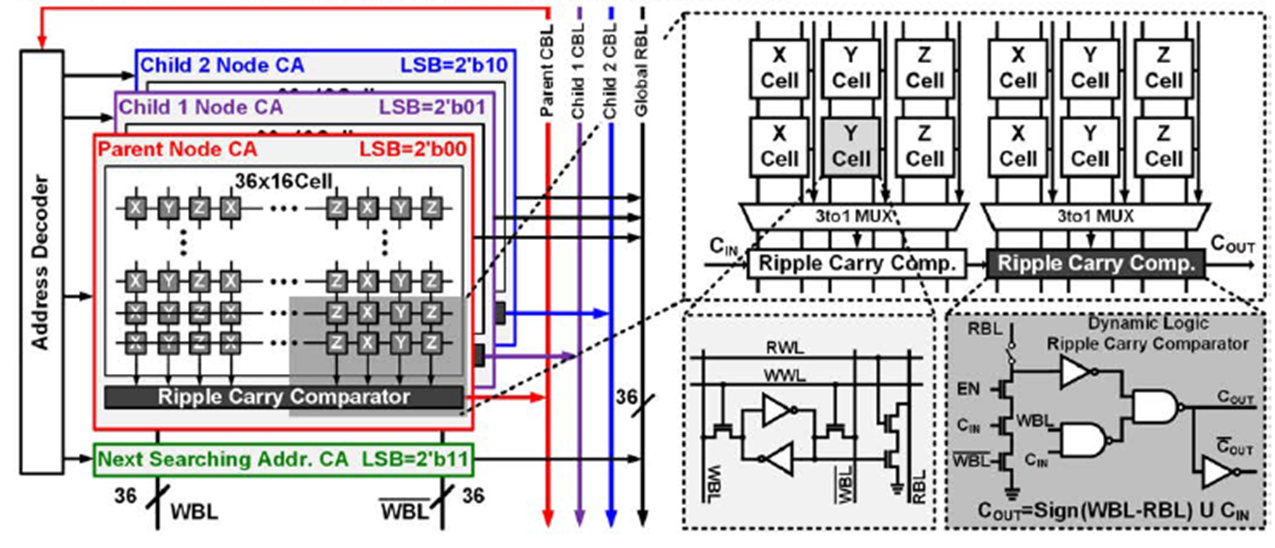
The HGR processor consists of a CNN-stereo engine (CSE) and an ICP-PSO engine (IPE).

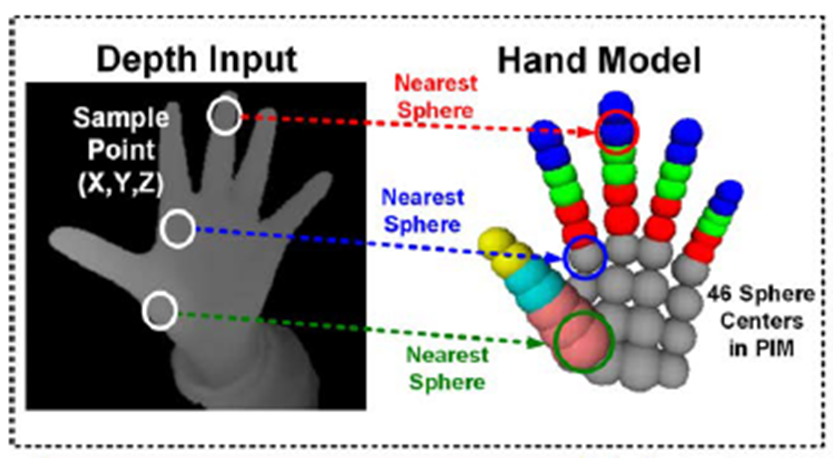
The CSE contains two line-streaming CNN cores with 4 locally distributed memories and one matching core. The CNN core has one pipelined CNN PE and a local DMA with a forwarding/backwarding (FWD/BWD) unit to balance workloads between the CNN cores.

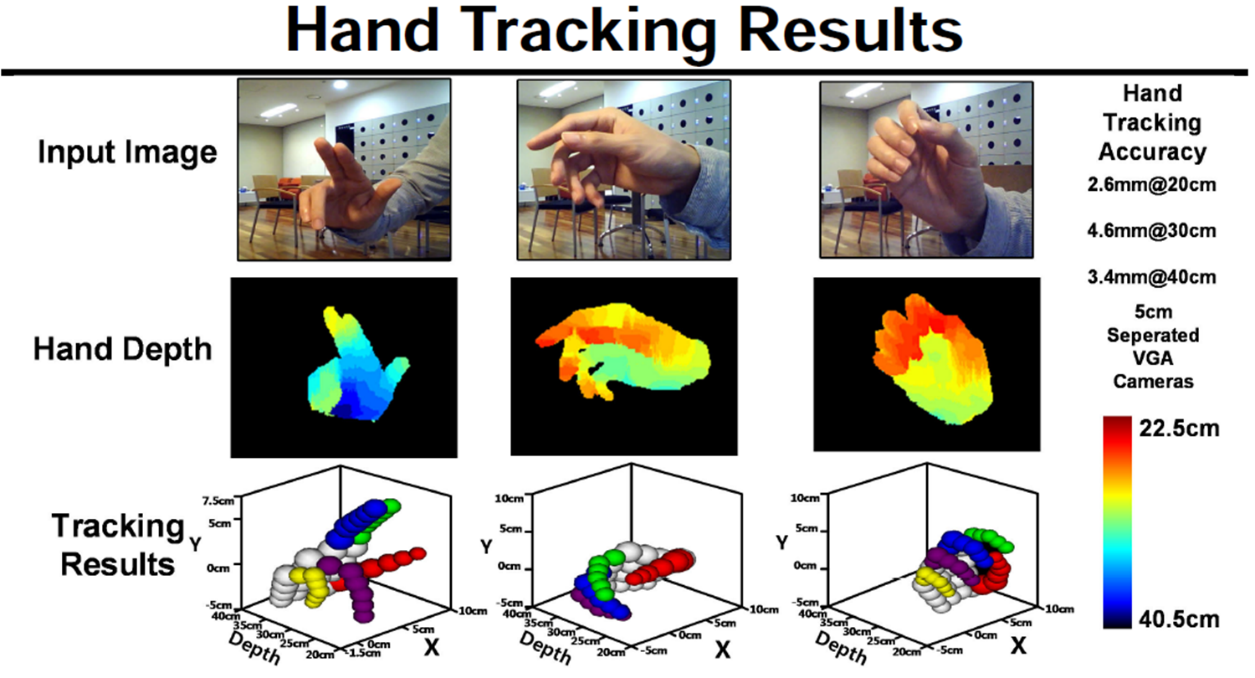
 The IPE consists of a NNS unit with 16-way parallel NNS PIMs and a hand tracking unit.

The line-streaming CNN operation is accelerated by the 7-stage pipelined CNN PE that processes 48 MACs per cycle with 96% core utilization.

Moreover, the pipelined architecture enables line-streaming processing, as well as memory access latency hiding to achieve 1.80TOPS/W, 60MHz at 0.9V.



The PIM architecture specialized for NNS to track a user’s hands in the IPE. Hand tracking requires >360K-node k-d tree NNS between the 46-sphere model in the memory and the depth input from the CSE.



# Plan for next week :

Item 1 : Continue FPGA practicing ;

Item 2 : Paper reading ;