Verification of Digital Designs: Week 3

Martin Schoeberl

Technical University of Denmark
Embedded Systems Engineering

September 8, 2021

Overview

- Kasper on UVM
- Discuss your tester solution
- Lab: design and test in pairs

Lab Time + Home Work

- Work in pairs
- One design engineer, the other verification engineer
- Switch role and team
- Specify together the design and make a test plan
- Do not aim for a too complicated design
- A configurable counter might be fine
- Document this in `lab3/README.md`

Design Examples

- Accu
- programmable counter
- FIFO
- FSM
- FSMD
- UART tx or rx
- Feel free to chose your own ideas