Verification of Digital Designs: Week 6

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November 30, 2021

Overview

- Constraint random
- Processor testing
- Projet topics
- Code review of your designs and tests
- There is a 2006 version of the book available
- In two weeks we have a guest lecture from a verification company

(Constraint) Random

- Usually, we cannot exhaustive test a design
- Pick corner cases
- Use random values
- Constraints build limits on the random values
- We do not yet have a constraint random solver in Chisel

Co-simulation

- Have a reference model in software
- C/C++ is common
- Some of you did it as part of the AluAccu tester
- Then run the hardware and the model on corner cases, random data

Testing a Processor

- Write self testing programs
- With a known outcome
- E.g., return 0
- With a C compiler there are many test available
- We run nightly tests on Patmos with gcc torture, show email
- Show in Lipsi

Reference Model

- Implement an instruction set simulator
- Not timing correct
- No pipeline
- Just a big case statement
- Some of you have/had it as project in CAE

Processor Co-simulation

- Run the ISA simulator and the hardware in parallel
- Execute test programs
- Compare the results
- What would you compare in a RISC-V ISA?
- How can you handle timing difference?
- Talk on Patmos and show in Lipsi

Code Review

- A static verification tool
- Identify functional and code errors
- Performed by peers
- Not to criticize the developer
- To share knowledge
- To have a consistent coding style
- For better readable code
- Code reviews have been commonly used in SW development

Code Review

- Can be part of pull requests
- Each pull request has to have a review before accepting it
- Motivates committers to tie up loose ends
- Common practice in open-source projects
- E.g., it is public in the Chisel development and very friendly
- Maybe watch the Chisel project for some time

Project Work

- Read up on a topic
- Anything related to testing and verification
- Implement the project
- Write a paper style report
- Give a 15’ presentation in the last week
- Add your project title to the README.md
- Start a folder in our repo for your project
- Put a README.md into your folder

Project Topics

- Constraint random generator
- Processor co-simulation (use your RISC-V simulator)
- Cover points in Chisel
- Assertions, including time (see book, p 64)
- Test coverage at FIRRTL level
- Create test infrastructure (e.g., AXI transactions)
- Your idea/interest

Code Review Time

- Andreas labs ready?
- Three more designs on lab3
- Solutions for lab4