Naqash Naveed

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Education

October 2023 – December 2025

MS Communication and Electronics Engineering, Technical University of Munich(TUM), Germany

- System on Chip Technologies
- Chip Multi-core processor
- Embedded Systems for Machine learning
- Analog and Mixed-Signal Circuit Design
- Synthesis of Digital Systems
- Testing of Digital Circuits
- VHDL System Design Laboratory
- System-C Laboratory

September 2016 – July 2020

BS Electrical Engineering, National University of Sciences and Technology(NUST), Pakistan

- Microprocessor Systems
- Digital Logic Design
- Data structures and Algorithms
- Power Electronics
- Embedded Systems
- Digital Signal Processing
- Object Orientated Programming
- Control Systems

Professional Experience

June 2025 – December 2025

Master Thesis Student, Infineon Technologies AG, Munich, Germany

- Gained in-depth knowledge of control strategies, power converters and PSoC control MCU.
- Implemented firmware (C) for peak current mode control (PCMC) strategy for dual active bridge (DAB) topology on PSoC control MCU.
- Validated PCMC using PLECS and RT Box Hardware-in-the-Loop (HIL), and currently working on validation with DAB hardware.
- Hand's on experience with ModusToolbox and device configurator.

PCMC | DAB | C | MCU | HIL | PLECS | RT-BOX | ARM | ModusToolbox

June 2024 – May 2025

Working Student : Software Engineer, Infineon Technologies AG, Munich, Germany

- Developed chaiTea Based Tests for PSoC Control MCU.
- Developed C-based unit tests for power conversion libraries using Unity, Ceedling, and CMock.
- Implemented C-based fuzz tests with AFL++ fuzzers to enhance software robustness.
- Integrated Docker-based test environments, optimizing execution and debugging workflows for C-based tests.
- Designed Simulink-based tests for power conversion libraries using Simulink Test Manager.
- Managed CI\CD pipeline and improved test documentation in Confluence, TM4J, and Jira, ensuring traceability of test specifications.

C | Simulink | MATLAB | Git | Jira | CI\CD | ARM | Docker | Unity | Ceedling | CMock | AFL++

October 2024 – April 2025

Internship : CVA6 Memory Encryption, Technical University of Munich (TUM), Munich, Germany

- Developed RTL (System Verilog) for memory encryption modules for Culsans-CVA6 (RISC-V-based architecture), integrating ASCON encryption between the LLC and DRAM.
- Worked on cache and memory hierarchy analysis, including eviction policies and cache line.
- Worked on simulation environments for CVA6 multicore, enabling OpenOCD-based JTAG simulation.
- Created and improved Makefiles and Python scripts.
- CoreMark benchmarks to validate the design.

System Verilog | RISC-V | make | python | Modelsim | OpenOCD

February 2021 – October 2023

System Design Engineer, Signatics pvt ltd, Pakistan

- **Signal Monitoring :** Design and implementation (Verilog, VHDL, C) of high-performance signal processing applications on a custom hardware platform (Software Defined Radio (SDR)) featuring high-speed ADCs and Xilinx Zynq Ultrascale+ (FPGA, ARM) with a two-stage superheterodyne RF front-end. Developed a real-time spectrum analyzer (30 MHz–6 GHz sweep, 500 MHz bandwidth, 1 µs time resolution) with features including persistence, peak hold, waterfall, and multi-channel channelizers. Enabled real-time data streaming to LabVIEW Host via PCIe DLLs (C/C++, Windows DLLs).
- **Direction Finding (DF) :** Developed RTL (Verilog, VHDL) and firmware (C) for a five-channel, high-speed ADC system (500 MHz IQ sample rate) on Zynq Ultrascale+ for direction finding. Implemented phase alignment, DDC-based downsampling, and real-time data streaming to host PC via PS-Ethernet. Utilized MUSIC and Correlative Interferometry algorithms (LabVIEW, C) for direction estimation.
- **Digital Down Converter (DDC) :** Designed and implemented a fixed DDC on LabVIEW FPGA for NI USRP TwinRX, achieving 400x downsampling and 80 dB out-of-band attenuation using three-stage polyphase filters and DDS-based frequency shifting. Enabled phase synchronization for multi-channel TwinRX setups.
- **Additional Contributions :** Board bring-up and peripheral driver development (Verilog, VHDL, C) ; Applications for Xilinx interfaces (DMA, AXI, MIG, DDR, SERDES, PCIe, 10G Ethernet, Aurora, JESD204B) ; Application for Xilinx Ultrascale+ RFSoC with phase synchronize ADC and DAC ; Real-time data synchronization between PL and Multicore PS ; performed system-level optimization for SFDR and sensitivity ; supported lab testing with oscilloscopes, spectrum analyzers, and signal generators.

C | C++ | Xilinx Vivado | Verilog HDL | VHDL | RTL | RFSoC | Zynq Ultrascale+ | SERDES | PCIe | Aurora | JESD204B | DSP | Ethernet Subsystem | Embedded C | RF | SDR | LabVIEW FPGA | Python | ARM

July 2020 – February 2021

Hardware Design Engineer (Embedded), AKSA-SDS pvt ltd, Pakistan

- **Radio Frequency Front-End (RFFE) :** Parsed Ethernet-based communication from SDR to BeagleBone MCU (Python) relayed to Xilinx Spartan 6 using SPI and UART. Designed and implemented a control unit (Verilog/VHDL, Xilinx Spartan 6) for the RF front-end of a SDR to control RF chain (local oscillators, direct digital synthesizers, ADCs, DACs, digital alternators, and amplifiers).
- **Standby Flight Information Display Unit (SFIDU) :** Optimized memory resources and user experience for a standby altitude meter for aircraft emergency use. The system consisted of a Zynq 7000 SoC FPGA coupled with STM32, providing reliable backup flight information.
- **Additional Contributions :** Developed a custom PetaLinux build for Xilinx SoC ; implemented BPSK and MSK modulation/demodulation models in MATLAB ; performed hands-on lab testing with oscilloscopes, spectrum analyzers, and signal generators.

C | C++ | Xilinx ISE | Xilinx Vivado | Verilog HDL | VHDL | RTL | Python | Petalinux | SDR | ARM | STM32

September 2019 – February 2020

Research And Development Intern, Real-time Intelligent Secure Computing (RISC) Research Lab, Pakistan

- Theory of RISC-V ISA
- Key concepts of Verilog HDL
- Hands on experience on Intel Quartus II , QSYS and ModelSim
- Implementation of five stage pipelined RV32I on logisim
- Implementation of five stage pipelined RV32I in Verilog HDL and tested it on altera DE-1 board
- Floating point extension in RV32I
- GNU cross compiler support for RV32IF
- JTAG UART support for RV32IF

RISC V | Verilog HDL | Quartus | Modelsim | Logisim | Assembly | C | C++ | Python

Skills

Programming Languages	Verilog HDL, VHDL, System Verilog, make, System-C, LabVIEW, Assembly Languages(RISC-V, MIPS, ARM , x86, x64), Embedded C, C++, Python, JAVA, MATLAB/Simulink
IDE's / Tools	Xilinx ISE, Xilinx Vivado, Altera Quartus II, Modelsim, Lattice Diamond, GHDL, Icarus Verilog, GTKWave, ModusToolbox, PLECS, PetaLinux , Arduino, Advance Design System (ADS), PSpice
Platforms	Zynq Ultrascale+, NI USRP, Altera Cyclone, STM32, 8051 micro-controller, Raspberry pi, Arduino, Infineon PSoC MCU, BeagleBone, RT-Box