Silicon (2022) 14:10301–10311
https://doi.org/10.1007/s12633-022-01769-6

ORIGINAL PAPER

Design and Optimization of Dual Material Gate Junctionless FinFET Using Dimensional Effect, Gate Oxide and Workfunction Engineering at 7 nm Technology Node

Rambabu Kusuma [1] · V. K. Hanumantha Rao Talari [1]

Received: 12 November 2021 / Accepted: 15 February 2022 / Published online: 1 March 2022

Abstract
In this paper, we designed and analyzed the performance of Dual Material Gate Junctionless FinFET(DMG JLFinFET) using gate engineering with high-k dielectrics for nanoscale applications. Here first we optimized the doping and later optimized the work function. Thereafter by using these optimized values we carried our work for other simulations. Various high-k materials are used as gate oxide. We found that by replacing gate oxide with high-k materials the device performance is improved in terms of I_{on}/I_{off}, SS, and DIBL. The fine tuning of gate workfunction reduces short channel effects (SCEs). In Fin width (F_W) variation, single gate oxide HfO_2 has 61.29 mV/dec and 16.03 mV/V, dual gate-oxide Si_3N_4 + HfO_2 has 61.22 mV/dec and 18.49 mV/V as SS and DIBL, respectively. In Fin height (F_H) variation single gate oxide HfO_2 has 63.04 mV/V and 27.11 mV/V, dual gate oxide Si_3N_4 + HfO_2 has 62.57 mV/V and 26.05 mV/V as SS and DIBL, respectively. I_{on}/I_{off} is improved to 0.78×10^7 using HfO_2 and 1.25×10^7 using Si_3N_4 + HfO_2 as gate oxides. The ratio of I_{on}/I_{off} with F_H and F_W variation provide evidence that the DMG JLFinFET is best competent for low power nanoscale applications. 3-D simulations are done using Cogenda genius Visual TCAD.

Keywords Dual material gate (DMG) · SCEs · JLFinFET · On-current · Off-current

1 Introduction

The possibility of scaling of MOS (metal oxide semiconductor) devices has made the Complementary CMOS technology commercially successful [1]. As CMOS devices are scaled into deep sub-micrometer regimes, power dissipation increases dramatically due to an increase in leakage current (caused mostly by threshold voltage lowering) and other factors like drain-induced barrier lowering (DIBL), temperature effect, narrow width effect, gate-induced drain leakage (GIDL) [2]. Furthermore, due to direct scaling, conventional MOSFETs have issues such as excessive parasitic capacitance, and surface mobility deterioration. Two solutions were proposed: the first was to operate the device at low temperatures, and the second was Fully Depleted Silicon on Insulator (FDSOI) [3–6]. Thin-film SOI MOSFETs have enhanced short channel effects (SCEs), have excellent latch-up immunity, and have a lower DIBL impact [7]. But SOI devices has lower carrier transport with high electric field near drain, causes hot-carrier effect [8]. To overcome these issues double-gate devices were proposed [9, 10]. The overlap capacitances are the major problem in double-gate devices due to miss alignment of gates [11].

To alleviate above problems self-aligned FinFETs were proposed where gate is self-aligned to reduce parasitic resistance and it is effectively controlling SCEs [12–14]. Bulk and SOI technologies are the two ways for designing FinFETs. The advantage of bulk technology was low self-heating and wafers at a reasonable cost are available [15, 16], on other hand SOI FinFETs have more saturation current and low leakage current and low parasitic capacitances [17–19]. The gate material engineering was proposed [20–23] with two different workfunction materials are used for gate structures to increase the efficiency of carrier transportation which suppresses the SCEs [24–28]. FinFETs are suitable devices to control the leakage current. FinFETs are front runners of current nanometer technology. Dual material bottom spacer ground plane

✉ Rambabu Kusuma
rambabu@student.nitw.ac.in

V. K. Hanumantha Rao Talari
tvkhrao75@nitw.ac.in

[1] Department of Electronics and Communication Engineering, National Institute of Technology Warangal, Warangal 506004, India

FinFET performance was analyzed and shows that dual material improves I_{on}/I_{off} ratio and ground plane reduces the DIBL [29]. Different structures are proposed in literature like Teeth Junctionless Gate All Around Field Effect Transistor [30] and Ion Sensitive Field Effect Transistors (ISFET) [31]. To the best of authors knowledge in the literature very few dual material gate FETs were designed but, not dual material gate junctionless FinFET.

In this paper, we proposed Dual Material Gate JLFinFET to reduce SCEs. The organization of the paper as follows. Section II describes the device structure, section III results and discussion with I_{on}/I_{off} current ratio, SS, and DIBL included and section IV concludes the paper.

2 Device Structure and Simulation Setup

The DMG JLFinFET 3D schematic is shown in Fig. 1a and 2D X-Y cut of DMG JLFinFET shown in Fig. 1b. The gate length (L_G) is 14 nm, fin height (F_H) is varied from 10 nm to 30 nm, fin width (F_W) is varied from 4 nm to 6 nm. To avoid junction formation at nanoscale, uniform doping is used. Si_3N_4 and HfO_2 are used as high-k materials. All simulations using Visual TCAD [32–34] are carried out at T = 300 K.

The mid-gap metals are used as gate materials. The metal gate workfunction for M1 is 4.9 eV and M2 is 4.3 eV to 4.7 eV which are placed at source side and drain side, respectively. The gate stack is made of SiO_2, Si_3N_4 and HfO_2. All contacts are made with aluminum.

The physical models: band gap narrowing and dopant dependent models are used as the doping concentration is uniform from source to drain. Fermi Dirac distribution model is used to get good accuracy and SRH model is used to estimate generation and recombination effects. Lombardi mobility model is invoked to find mobility degradation. Gummel and Newton numerical methods are invoked to attain good results. Quantum drift-diffusion model invoked for the quantum confinement effect. To validate the simulation results we

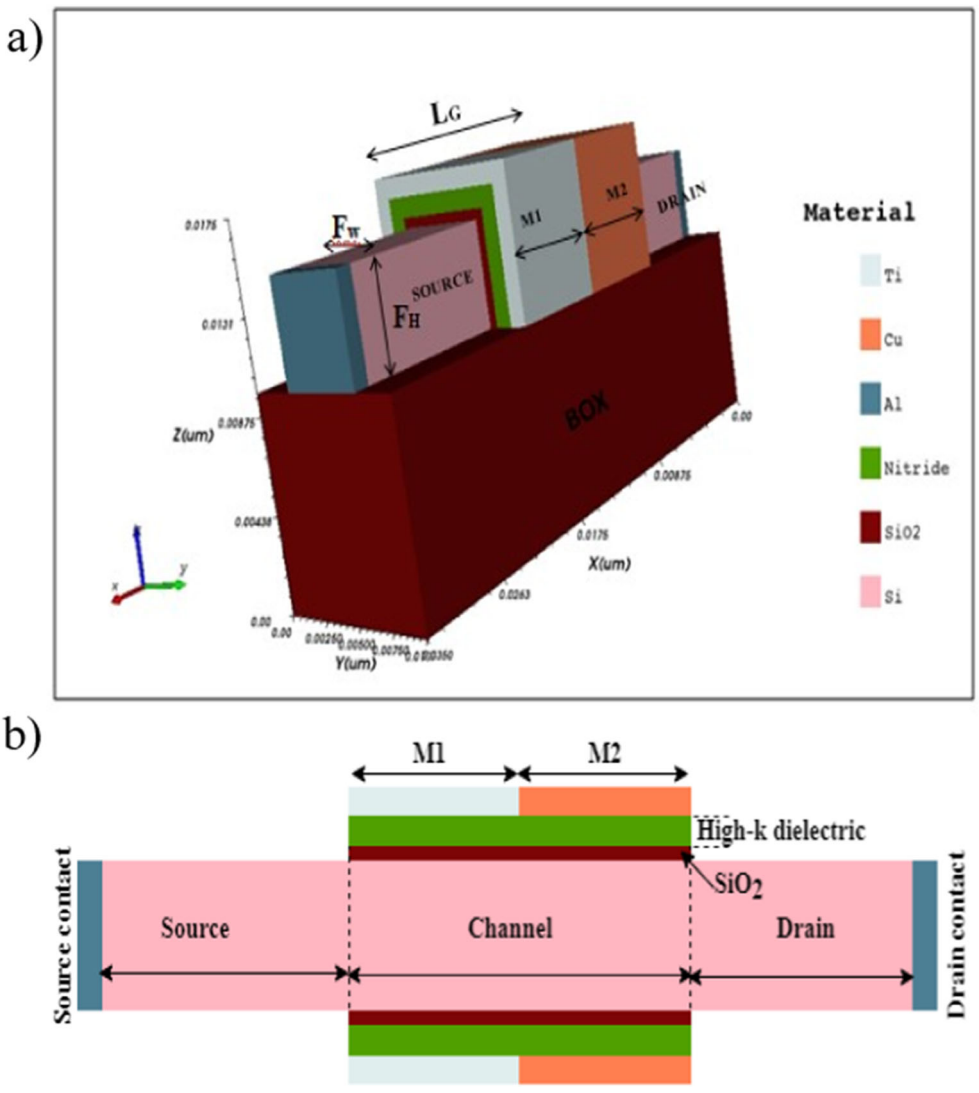

Fig. 1 **a** Three-dimensional view of DMG JLFinFET, **b** 2D X-Y cut view of DMG JLFinFET

calibrated the experimental data [35] shown in Fig. 2. The device dimensions and parameters used in this work are given in Table 1.

3 Results and Discussions

The drain characteristics of the DMG JLFinFET simulated in two groups. First one used different single dielectric material as gate oxide and second one by various Gate Stack(GS) configurations to investigate the effect of GS on 14 nm gate length. We used single dielectric materials SiO_2, Si_3N_4 and HfO_2. For GS configuration SiO_2 + Si_3N_4, SiO_2 + HfO_2, Si_3N_4 + HfO_2 are used. Figure 3 shows I_{on}/I_{off} ratio while varying workfunction of M2 with single gate oxide i.e. SiO_2 for different doping concentration levels (5E17 cm^{-3} to 5E19 cm^{-3}). Figure 4 shows the effect of doping variation on drain current with single gate oxide i.e. SiO_2, Si_3N_4, and HfO_2. In single gate oxide the DMG JLFinFET with HfO_2 as gate oxide has less leakage current due to high dielectric constant of HfO_2.

3.1 Gate Oxide Engineering

SiO_2, Si_3N_4 and HfO_2 are taken as gate oxides individuvally with dielectric constant 3.9,9 and 24, respectively. SiO_2 with 0.5 nm considered as interfacial layer, Si_3N_4 and HfO_2 is 0.96 nm and 3.07 nm, respectively to get EOT = 1 nm considered as per IRDS [36]. In each case I_{off} was extracted. Workfunction of M1 is fixed. i.e. Φ_{M1} = 4.9 eV and vary the workfunction of M2 i.e. Φ_{M2} from 4.3 eV to 4.7 eV. The doping concentration of source, drain and channel are taken as uniform because simultaions are performed for JLFinFET. The I_{on}/I_{off} variation is observed by taking different doping levels. The doping concentration is varying from $5x10^{17}cm^{-3}$ to $5x10^{19}cm^{-3}$. From below Fig. 3 it is evident that I_{on}/I_{off} ratio is good for doping concentration of $1x10^{18}cm^{-3}$ compared to other doping concentration levels. However, with increasing the workfunction of M2, the off state current gradually increases and it is more for doping concentration $5x10^{19}cm^{-3}$ hence the I_{on}/I_{off} ratio is very low for doping $5x10^{19}cm^{-3}$. It is observed from Fig. 3 the variarion of Φ_{M2} is less effect on I_{on}/I_{off} but the variation of I_{on}/I_{off} is more in doping concentration. The slight variation of I_{on}/I_{off} has observed at Φ_{M2} = 4.5 eV. Figure 4 shows the I_{on}/I_{off} ratio with doping variation with fixed Φ_{M1} = 4.9 eV and Φ_{M2} = 4.5 eV. it is evident from Fig. 4 that Compared to SiO_2 and Si_3N_4 gate oxides, HfO_2 has less leakage current because the dielectric constant of HfO_2 is higher than SiO_2 and Si_3N_4. Hence the I_{on}/I_{off} ratio is also high for HfO_2.

SiO_2 + Si_3N_4, SiO_2 + HfO_2 and Si_3N_4 + HfO2 are considered as dual gate oxides individually.The work function of M1 is fixed. i.e. Φ_{M1} = 4.9 eV and vary the workfunction of M2 i.e. Φ_{M2} from 4.3 eV to 4.7 eV. In Fig. 5a the I_{on}/I_{off} variation is observed for all doping concentration levels ($5x10^{17}cm^{-3}$ to $5x10^{19}cm^{-3}$) at different workfunction values of Φ_{M2}. The doping $1x10^{18}cm^{-3}$ at workfunction 4.5 eV giving high I_{on}/I_{off} ratio in all combinations. From Fig. 5b it is evident that the gate stack combination Si_3N_4+ HfO_2 has superior I_{on}/I_{off} compared to SiO_2 + Si_3N_4 and SiO_2 + HfO_2.

From above Figs. 4 and 5b it is observed that doping concentration $1x10^{18}cm^{-3}$ at workfunction Φ_{M1} = 4.9 eV and Φ_{M2} = 4.5 eV, The I_{on}/I_{off} is good compared to all other doping concentrations. The rest of simulations for fin width and fin height variation, doping concentration $1x10^{18}cm^{-3}$ and workfunction Φ_{M1} = 4.9 eV and Φ_{M2} = 4.5 eV are considered.

Table 1 Device dimensions and parameters used

Parameter	Value
Gate length	14 nm
Fin width	(4–6) nm
Fin height	(10–30) nm
Interfacial Layer SiO_2	0.5 nm
High-k dielectric thickness	Variable (Si_3N_4–0.96 nm, HfO_2–3.07 nm)
EOT(Equivalent Oxide Thickness)	1 nm
Supply Voltage	0.8 V
Workfunction of M1	4.9 eV
Workfunction of M2	4.3 eV- 4.7 eV

3.2 FinWidth Variation

The drain current versus gate voltage for different fin widths with single gate oxides are shown in Fig. 6. The gate length (L_G) and fin height (F_H) are fixed at 14 nm and 30 nm with fin width (F_W) varying from 4 nm to 6 nm. The drain current variation was observed for single gate oxides SiO_2, Si_3N_4 and HfO_2. By increasing the F_W off current also increased slightly because it loses the gate control over the channel [37]. Among the F_W variation lowest F_W 4 nm has less I_{off} and I_{on}/I_{off} ratio is $>10^6$ for the same.

The drain current dependence on fin widths with dual gate oxides are shown in Fig. 7. The gate length (L_G) and fin height (F_H) are fixed at 14 nm and 30 nm, fin width (F_W) varying from 4 nm to 6 nm. SiO_2 + Si_3N_4, SiO_2 + HfO_2 and Si_3N_4 + HfO_2 are used as dual gate oxides. While F_W is increasing I_{off} also increased where the control action of gate is less. Si_3N_4 + HfO_2 gate stack configuration with F_W 4 nm has less I_{off}. The I_{on}/I_{off} ratio is far better for dual gate oxide than single gate oxide configuration.

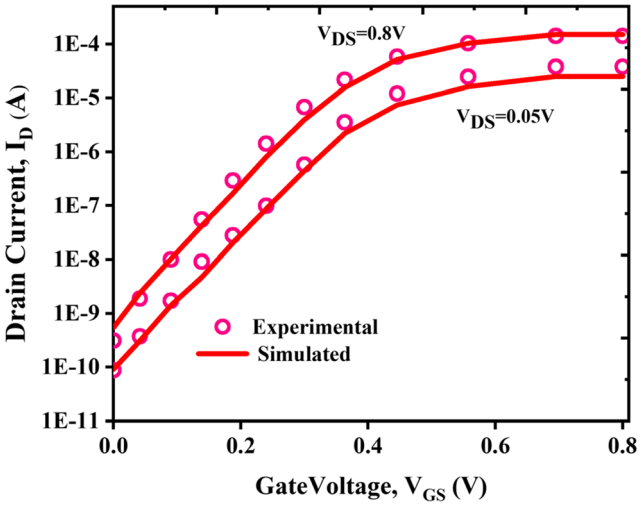

Fig. 2 Calibrated Drain Characteristics of DMG JLFinFET [35]

3.3 Fin Height Variation

The effect of Fin height variation using single gate oxides on drain current is shown in Fig. 8. L_G and F_W are fixed to 14 nm and 5 nm. Fin height (F_H) is varied from 10 nm to 30 nm. By increasing the F_H, the I_{off} also increasing. For higher F_H 30 nm the I_{off} is more due to side wall fringing fields at high fin height.

The effect F_H variation using dual gate oxides on drain current is shown in Fig. 9. L_G and F_W are fixed to 14 nm and 5 nm F_H is varied from 10 m to 30 nm. An increase in F_H alters device design, resulting in a decrease in aspect ratio (F_W/F_H). The I_{on}/I_{off} ratio should increase with F_H, however it falls with decreased sensitivity owing to quantum confinement phenomenon [38]. The I_{on}/I_{off} ratio exceeding 10^6 at the lowest F_H of 10 nm and I_{off} staying < pA assures continued down scaling. An increasing the F_H, I_{off} also increasing. For higher F_H 30 nm the I_{off} is more due to less electrostatic integrity at high F_H.

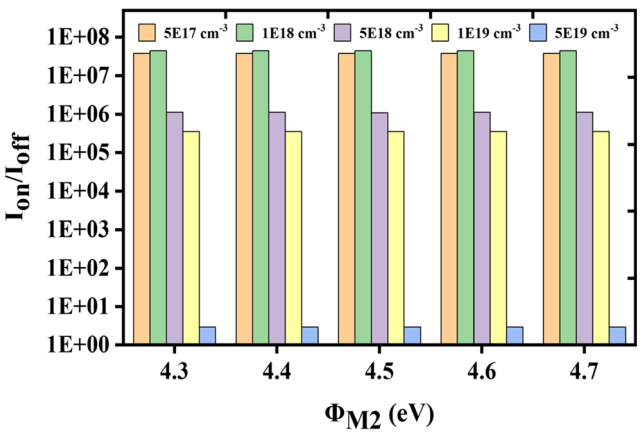

Fig. 3 Φ_{M2} Vs I_{on}/I_{off} with SiO_2 as gate oxide at constant Φ_{M1} = 4.9 eV

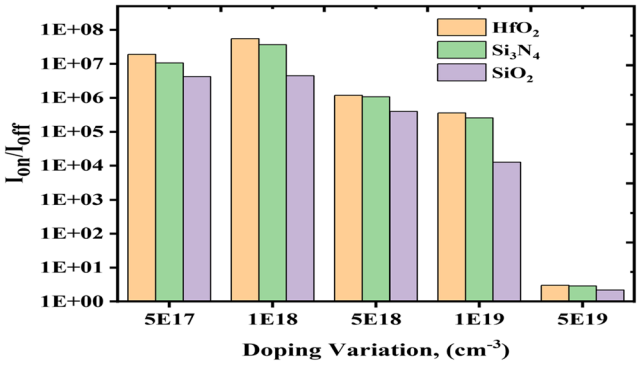

Fig. 4 I_{on}/I_{off} Vs Doping Variation with fixed Φ_{M1} = 4.9 eV and Φ_{M2} = 4.5 eV for different single gate oxides

Figure 10a shows how the distribution of potential occurred in DMG JLFinFET. At the drain side the potential distribution is high and it is less in source and channel thus reducing SCEs. Figure 10b and c shows the contour plots of conduction band energy and valence band energy. In both the energy level is more at source side and low at drain side because of band bending.

The I_{on}/I_{off} ratio is a significant electrical performance characteristic of the device, and it is intended to be high. The on-state (I_{on}) current is obtained as the drain current at gate voltage (V_{GS}) = 0.8 V and V_{DS} = 0.8 V. High-k gate dielectrics can improve the I_{on}/I_{off} ratio but mobility deterioration is a serious issue with high-k gate dielectrics owing to the scattering effect. The GS high-k metal gate technology has been utilized to control the mobility degradation problem.

The performance parameters I_{on}/I_{off}, SS and DIBL are calculated with F_W variations and tabulated in Tables 2, 3 and 4. As depicted in the tables single gate oxide configuration with HfO_2 is giving good I_{on}/I_{off} ratio for all F_W variations. In dual gate configuration Si_3N_4 + HfO_2 has better I_{on}/I_{off} ratio and it is maximum at F_W = 5 nm, approximately 1.93 × 10^7.

SS and DIBL are two important characteristics to study in nanoscale devices. The SS and DIBL are computed separately using below equations [19].

$$\mathrm{DIBL(mV/V)} = \frac{V_{T1} - V_{T2}}{V_{D1} - V_{D2}}$$

$$\mathrm{SS(mV/decade)} = \frac{\partial V_{GS}}{\partial \log_{10}(I_D)}$$

Where V_{T1} andbV_{T2} are threshold voltages calculated at V_{D1} = 0.05 V and V_{D2} = 0.8 V respectively. From Table 2. SS and DIBL are decreased from 72.48 mV/dec to 62.90 mV/dec and 50.56 mV/V to 22.33 mV/V respectively. From Table 3 it is evident that SS and DIBL are reduced from 69.83 mV/dec to 61.22 mV/dec and 42.79 mV/V to 19.01 mV/V. We observe that from Table 4 SS and DIBL are minimized from 67.35 mV/dec to 61.29 mV/dec and 35.99 mV/V to 16.03 mV/V. The overall comparison from

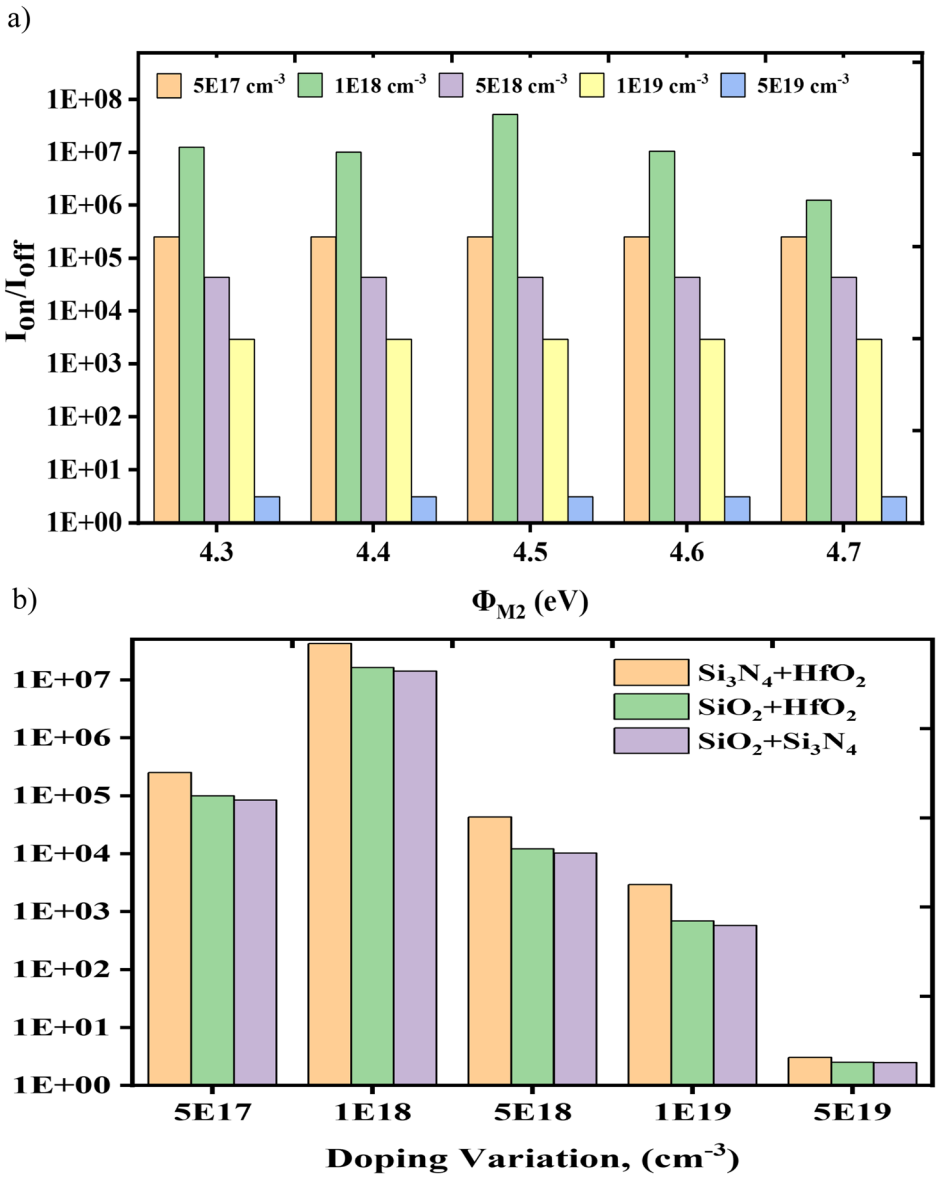

Fig. 5 Φ_{M2} Vs I_{on}/I_{off} with SiO_2 + Si_3N_4 as gate oxide at constant Φ_{M1} = 4.9 eV. b) I_{on}/I_{off} Vs doping variation with fixed Φ_{M1} = 4.9 eV and Φ_{M2} = 4.5 eV for different dual gate oxides

Tables 2, 3 and 4 is that by using high-k materials as GS the performance parameters such as I_{on}/I_{off}, SS, and DIBL are improved. Among the different configurations, single gate oxide HfO_2 giving good I_{on}/I_{off} ratio, in dual gate oxide Si_3N_4 + HfO_2 has superior I_{on}/I_{off}.

The I_{on}/I_{off} ratio with F_H variation is shown in Tables 5 and 6. It is observed that in single gate oxide combination HfO_2 is giving good I_{on}/I_{off} ratio. An ameliorated I_{on}/I_{off} ratio observed in dual gate oxide combination Si_3N_4 + HfO_2 because increasing the gate dielectric reduces the leakage current thereby increasing I_{on}/I_{off} ratio. The high-k dielectrics increases capacitance between gate and channel so less leakage current thereby improved I_{on}/I_{off}, SS, and DIBL. The electrical performance parameters with L_G = 14 nm, F_W = 5 nm, F_H = 20 nm are shown in Table 5. As moving on from single gate oxide to double gate oxide I_{on}/I_{off} ratio was improved to 1.25 × 10^7, SS, and DIBL are reduced to 63.18 mV/dec, 26.05 mV/V respectively. It is obvious from Table 6 that, as we are decreasing F_H to 10 nm, I_{on}/I_{off} ratio fall down to 1.71 × 10^6, SS, and DIBL 62.57 mV/dec, 29.90 mV/V respectively. Further reduction of fin height creates process complexity. Reducing the F_H is improving the SS but with cost of DIBL. The overall comparison from Tables 5 and 6 is that, among all gate oxide combinations Si_3N_4 + HfO_2 have better I_{on}/I_{off} ratio and the optimized F_H is 20 nm. As Si_3N_4 + HfO_2 have better results, comparison is made for this combination. From Table 7 it is evident that compare to Single Metal Gate JLFinFET, Dual Metal Gate JLFinFET is giving good performance.

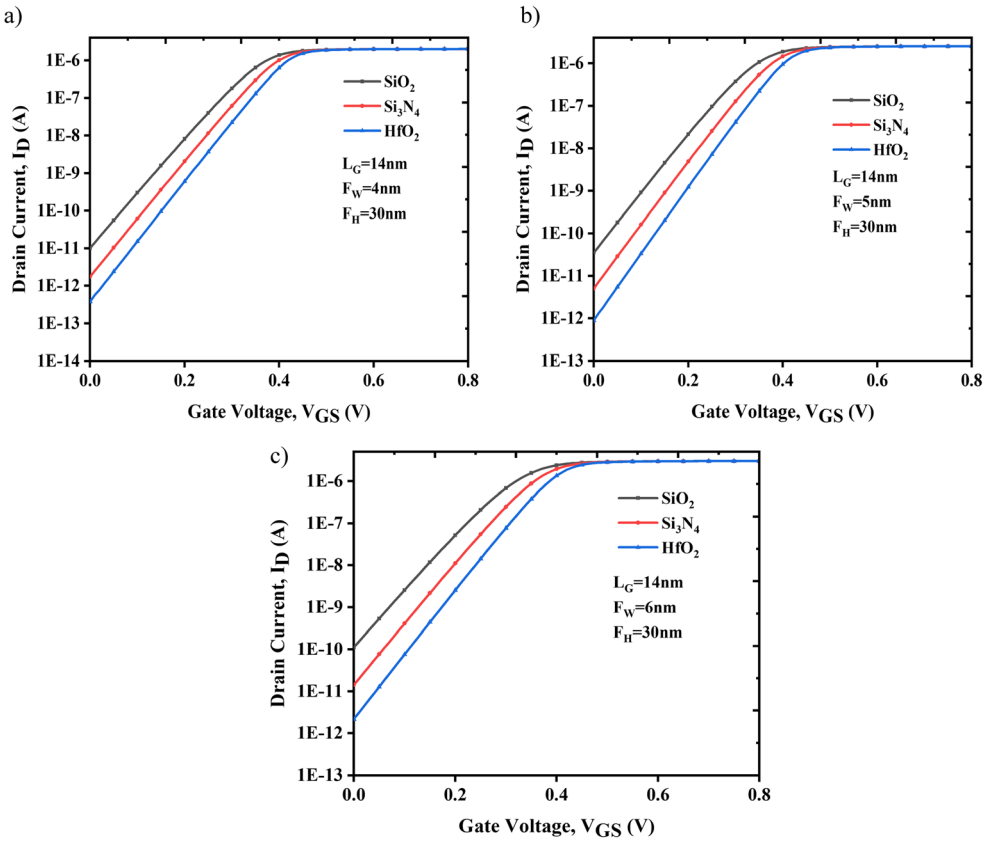

Fig. 6 Fin width variation of DMG JLFinFET with single gate oxides **a** F_W = 4 nm, **b** F_W = 5 nm, **c** F_W = 6 nm

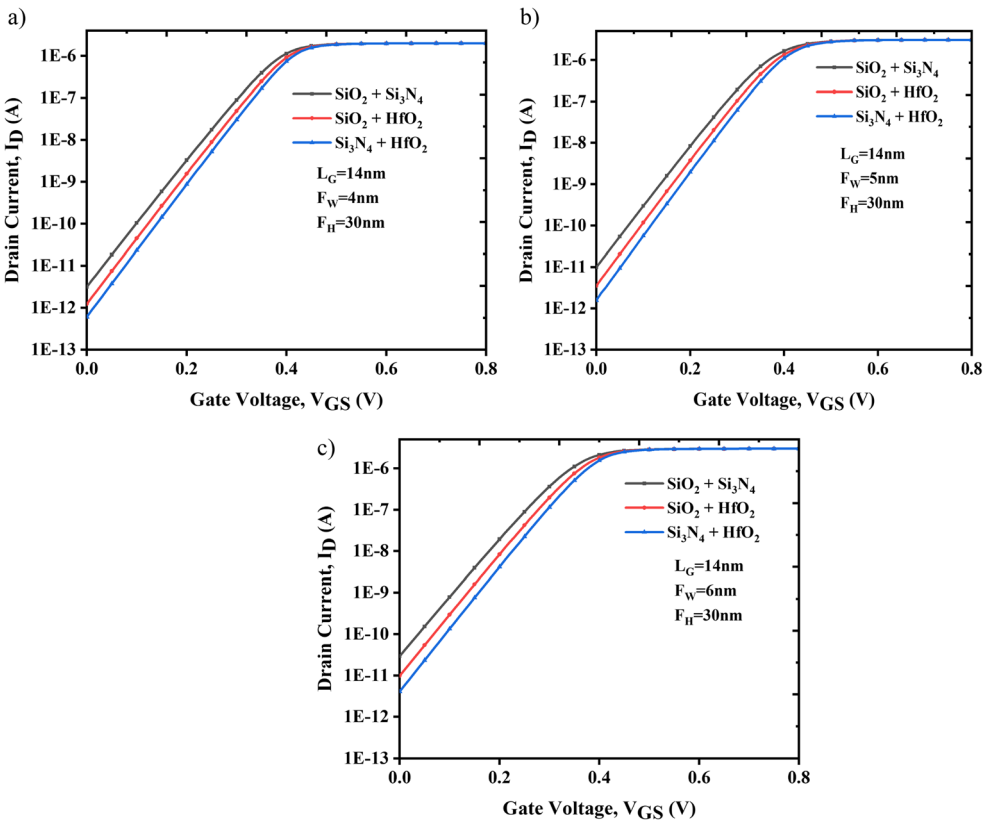

Fig. 7 Fin width variation of DMG JLFinFET with dual gate oxides **a** F_W = 4 nm, **b** F_W = 5 nm, **c** F_W = 6 nm

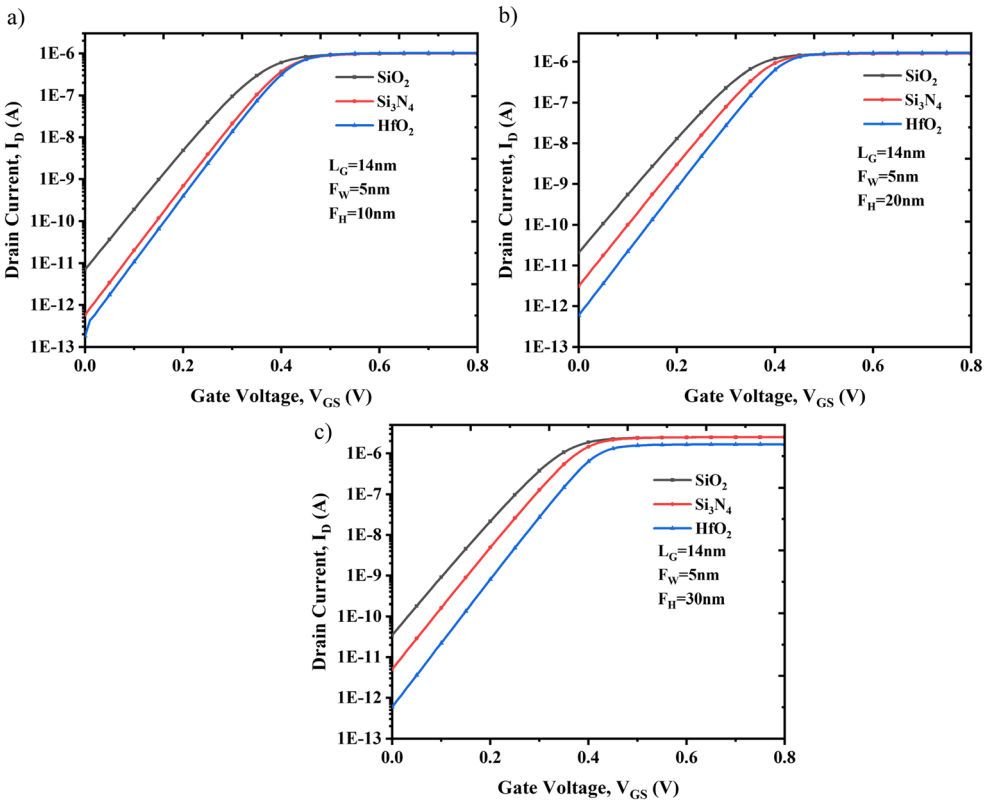

Fig. 8 Fin height variation of DMG JLFinFET with single gate oxides **a** F_H = 10 nm, **b** F_H = 20 nm, **c** F_H = 30 nm

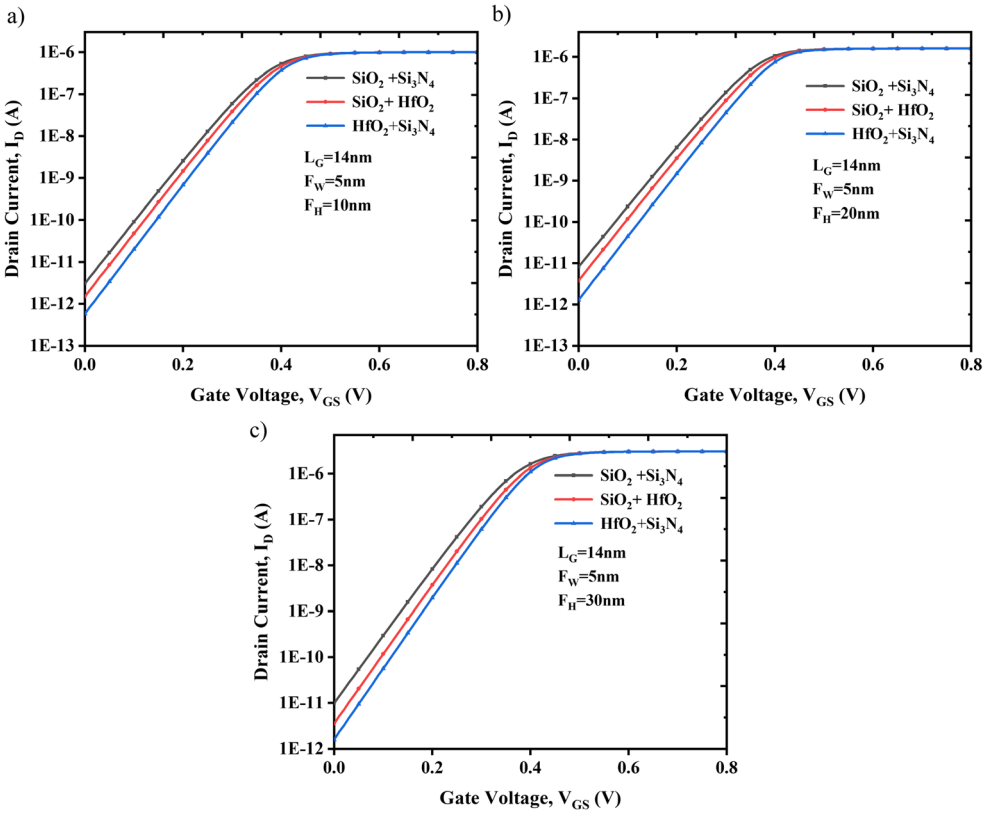

Fig. 9 Fin height variation of DMG JLFinFET with dual gate oxides, **a** F_H = 10 nm, **b** F_H = 20 nm, **c** F_H = 30 nm

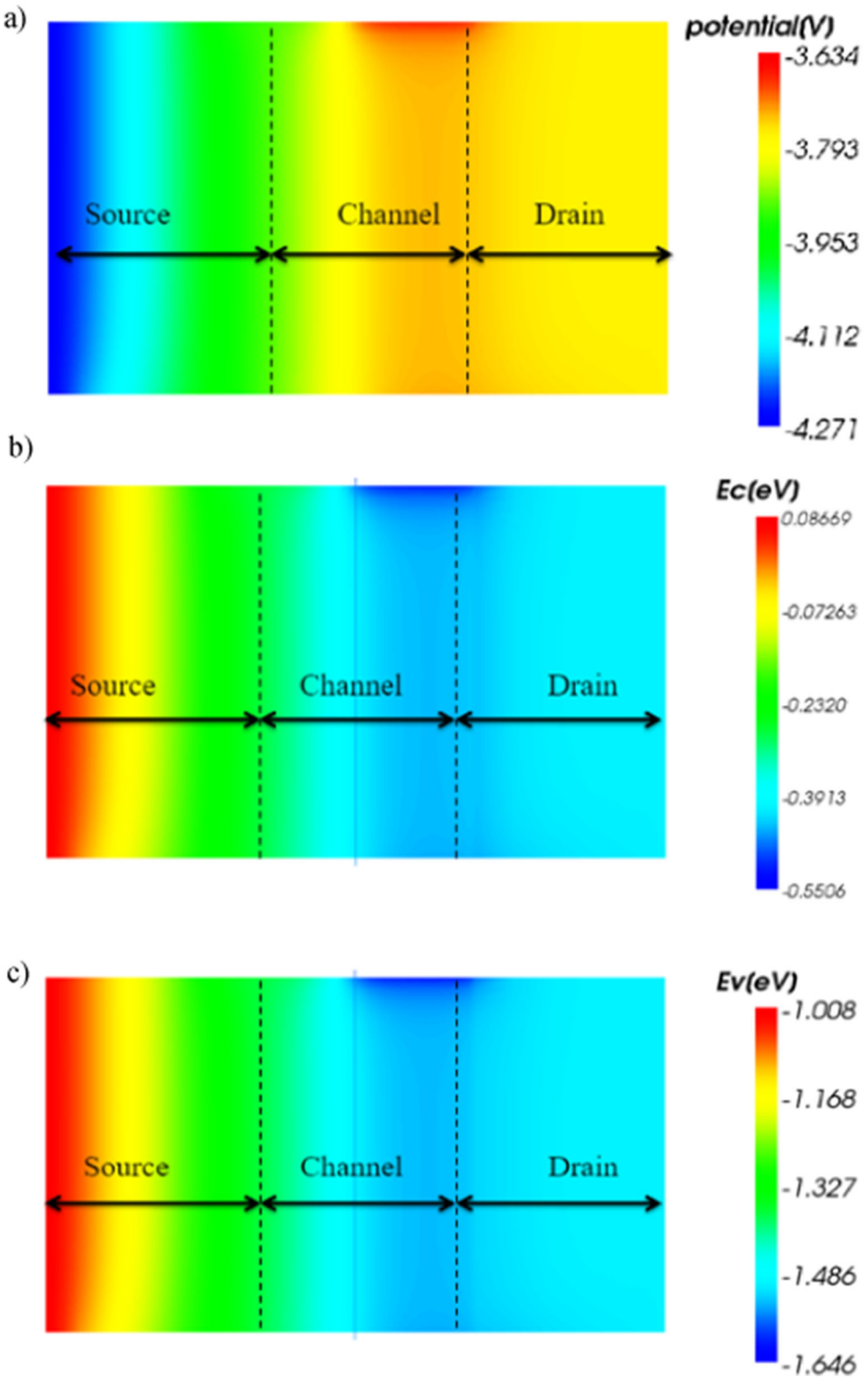

Fig. 10 Horizontal X-Ycut contour plots of potential distribution **b** conduction band energy **c** valence band energy of DMG JLFinFET with V_{GS} = 0.8 V and V_{DS} = 0.8 V at 300 K

4 Conclusion

Comparative analysis of DMG JLFinFET has been done using oxide and workfunction engineering. The device performance parameters I_{on}/I_{off} ratio, SS, and DIBL are extracted. In single gate oxide HfO_2 gives improved electrical characteristics. In dual gate oxide Si_3N_4 + HfO_2 has controlled SCEs due to reduced parasitic capacitances. Further, the same investigations

Table 2 Performance parameters of DMG JLFinFET with L_G = 14 nm, F_H = 30 nm, F_W = 6 nm

Configuration	Gate oxide	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	SS(mV/dec)	DIBL(mV/V)
Single Gate oxide	SiO_2	2.99×10^{-5}	1.11×10^{-11}	2.69×10^{6}	72.48	50.56
	Si_3N_4	2.99×10^{-5}	1.42×10^{-11}	2.11×10^{6}	67.53	33.60
	HfO_2	2.99×10^{-5}	2.17×10^{-11}	1.38×10^{6}	62.90	22.33
Dual Gate oxide	SiO_2+ Si_3N_4	2.99×10^{-5}	2.92×10^{-11}	1.02×10^{6}	69.23	38.80
	SiO_2+ HfO_2	2.99×10^{-5}	9.81×10^{-11}	3.05×10^{6}	66.79	31.07
	Si_3N_4+HfO_2	2.99×10^{-5}	4.07×10^{-12}	7.34×10^{6}	64.14	25.98

Table 3 Performance parameters of DMG JLFinFET with L_G = 14 nm, F_H = 30 nm, F_W = 5 nm

Configuration	Gate oxide	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	SS(mV/dec)	DIBL(mV/V)
Single Gate oxide	SiO_2	2.52×10^{-5}	3.52×10^{-11}	7.16×10^{5}	69.83	42.79
	Si_3N_4	2.52×10^{-5}	8.94×10^{-13}	2.82×10^{6}	65.29	28.95
	HfO_2	2.52×10^{-5}	5.08×10^{-12}	4.96×10^{6}	62.41	19.01
Dual Gate oxide	SiO_2+ Si_3N_4	3.06×10^{-5}	9.89×10^{-12}	3.09×10^{6}	66.10	33.15
	SiO_2+ HfO_2	3.06×10^{-5}	3.54×10^{-12}	8.64×10^{6}	62.14	26.55
	Si_3N_4+HfO_2	3.06×10^{-5}	1.58×10^{-12}	1.93×10^{7}	61.22	22.18

Table 4 Performance parameters of DMG JLFinFET with L_G = 14 nm, F_H = 30 nm, F_W = 4 nm

Configuration	Gate oxide	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	SS(mV/dec)	DIBL(mV/V)
Single Gate oxide	SiO_2	2.01×10^{-6}	1.02×10^{-11}	1.97×10^{5}	67.35	35.99
	Si_3N_4	2.01×10^{-6}	1.76×10^{-12}	1.14×10^{6}	62.99	24.59
	HfO_2	2.01×10^{-6}	3.78×10^{-13}	5.31×10^{6}	61.29	16.03
Dual Gate oxide	SiO_2+ Si_3N_4	2.01×10^{-6}	1.18×10^{-12}	1.70×10^{6}	64.65	28.07
	SiO_2+ HfO_2	2.01×10^{-6}	1.24×10^{-12}	1.62×10^{6}	62.92	22.23
	Si_3N_4+HfO_2	2.01×10^{-6}	1.07×10^{-13}	1.88×10^{7}	62.74	18.49

Table 5 Performance parameters of DMG JLFinFET with L_G = 14 nm, F_W = 5 nm, F_H = 20 nm

Configuration	Gate oxide	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	SS(mV/dec)	DIBL(mV/V)
Single Gate oxide	SiO_2	1.60×10^{-6}	2.09×10^{-11}	0.54×10^{6}	69.83	46.60
	Si_3N_4	1.60×10^{-6}	3.12×10^{-12}	1.96×10^{6}	65.48	31.91
	HfO_2	1.60×10^{-6}	5.90×10^{-13}	0.78×10^{7}	63.41	27.11
Dual Gate oxide	SiO_2+ Si_3N_4	1.60×10^{-6}	8.26×10^{-12}	1.25×10^{6}	67.75	39.13
	SiO_2+ HfO_2	1.60×10^{-6}	3.83×10^{-12}	2.66×10^{6}	65.97	33.53
	Si_3N_4+HfO_2	1.60×10^{-6}	1.29×10^{-12}	1.25×10^{7}	63.18	26.05

Table 6 Performance parameters of DMG JLFinFET with L_G = 14 nm, F_W = 5 nm, F_H = 10 nm

Configuration	Gate oxide	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	SS(mV/dec)	DIBL(mV/V)
Single Gate oxide	SiO_2	9.90×10^{-7}	7.04×10^{-12}	1.41×10^{5}	68.70	50.84
	Si_3N_4	9.90×10^{-7}	5.79×10^{-13}	1.71×10^{6}	63.58	36.45
	HfO_2	1.02×10^{-6}	1.81×10^{-13}	5.64×10^{6}	63.04	36.45
Dual Gate oxide	SiO_2+ Si_3N_4	9.90×10^{-7}	3.07×10^{-12}	3.23×10^{5}	66.49	43.55
	SiO_2+ HfO_2	9.90×10^{-7}	1.50×10^{-12}	6.58×10^{5}	64.17	37.51
	Si_3N_4+HfO_2	9.90×10^{-7}	5.79×10^{-13}	1.71×10^{6}	62.57	29.90

Table 7 Performance comparison of single metal and dual metal gate JLFinFET

Parameter	Single Metal Gate JLFinFET	Dual Metal Gate JLFinFET
I_{on} (A)	3.73×10^{-7}	9.90×10^{-7}
I_{off} (A)	1.01×10^{-12}	5.79×10^{-13}
SS (mV/dec)	71.92	62.57
DIBL (mV/V)	35.72	29.90

are carried out for F_W variations. At fin width(F_W) of 5 nm better I_{on}/I_{off} ratio and SS are obtained with values 1.93 × 10^7 and 62.41 mV/dec respectively. At 4 nm F_W an excellent DIBL value of 16.03 mV/V was found. Similarly for fin height (F_H) variations we calculated electrical performance parameters. At lowest F_H 10 nm we got good performance in terms of SS but at the cost of DIBL and I_{on}/I_{off}. From workfunction and gate oxide engineering with all different combinations, the comparative analysis with Si_3N_4 + HfO_2 has an excellent electrical performance. Result analysis shows that proper choosing of device dimensions gives good electrical performance for nanoscale applications.

Acknowledgements The authors thank to the Department of Electronics and Communications Engineering, NIT Warangal for providing the TCAD Tools.

Author Contributions Rambabu Kusuma: Writing- Original draft preparation, Formal Analysis, Investigation,Simulation, Data Curation. VK Hanumantha Rao Talari: Conceptualization, Methodology, Supervision.

Funding No Funding Received.

Data Availability Not applicable.

Declarations

Ethics Approval The contents of this manuscript are not now under consideration for publication elsewhere, The contents of this manuscript have not been copyrighted or published previously, The contents of this manuscript will not be copyrighted, submitted, or published elsewhere, while acceptance by the Journal is under consideration.

Consent to Participate Yes.

Consent for Publication Yes.

Research Involving Human Participants and/or Animals Not applicable

Informed Consent Not applicable

Financial Interests The authors declare they have no Financial interests.

Conflict of Interest The author has no conflicts of interest to declare that are relevant to the content of this article.

References

1. Moore GE (1998) Cramming more components onto integrated circuits. Proc IEEE 86:82–85. https://doi.org/10.1109/JPROC.1998.658762
2. Roy K, Mukhopadhyay S, Mahmoodi-Meimand H (2003) Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits. Proc IEEE 91:305–327. https://doi.org/10.1109/JPROC.2002.808156
3. Yan RH, Ourmazd A, Lee KF (1992) Scaling the Si MOSFET: from bulk to SOI to bulk. IEEE Trans Electron Devices 39:1704–1710. https://doi.org/10.1109/16.141237
4. Srivastava NA, Mishra K, Chauhan RK (n.d.) Analytical Modelling of Surface Potential of Modified Source FD-SOI MOSFET
5. Srivastava NA, Priya A, Mishra RA (2021) Interface trap charge-based reliability assessment of high-k dielectric-modulated nanoscaled FD SOI MOSFET for low power digital ICs: Modeling and simulation. Superlattice Microst 154:106871. https://doi.org/10.1016/j.spmi.2021.106871
6. Srivastava NA, Priya A, Mishra RA (2020) Analog and radio-frequency performance of nanoscale SOI MOSFET for RFIC based communication systems. Microelectron J 98:104731. https://doi.org/10.1016/j.mejo.2020.104731

7. Veeraraghavan S, Fossum JG (1989) Short-Channel effects in Soi Mosfet's. IEEE Trans lectron Devices 36:522–528. https://doi.org/10.1109/16.19963
8. Colinge JP (1992) Problems and issues in SOI CMOS technology. In: 1991 IEEE international SOI conference proceedings. Publ by IEEE, pp 126–127
9. Balestra F, Cristoloveanu S, Benachir M, Brini J, Elewa T (1987) Double-gate silicon-on-insulator transistor with volume inversion: a new device with greatly enhanced performance. IEEE Electron Device Lett 8:410–412. https://doi.org/10.1109/EDL.1987.26677
10. Kranti A, Chung TM, Flandre D, Raskin JP (2004) Laterally asymmetric channel engineering in fully depleted double gate SOI MOSFETs for high performance analog applications. Solid State Electron 48:947–959. https://doi.org/10.1016/j.sse.2003.12.014
11. Wong HS, Frank DJ, Taur Y, Stork JMC (1994) Design and performance considerations for sub-0.1 μm double-gate SOI MOSFETs. In: technical digest - international Electron devices meeting. IEEE, pp 747–750
12. Wong H-SP, Chan KK, Taw Y (n.d.) Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel
13. Lee JH, Taraschi G, Wei A, et al (1999) Super self-aligned double-gate (SSDG) MOSFETs utilizing oxidation rate difference and selective epitaxy. In: Technical Digest - International Electron Devices Meeting. IEEE, pp. 71–74
14. Hisamoto D, Lee WC, Kedzierski J et al (2000) FinFET—A self-aligned double-gate MOSFET scalable to 20 nm. IEEE Trans Electron Devices 47:2320–2325. https://doi.org/10.1109/16.887014
15. Park TS, Cho HJ, Choe JD et al (2006) Characteristics of the full CMOS SRAM cell using body-tied TG MOSFETs (bulk FinFETS). IEEE Trans Electron Devices 53:481–487. https://doi.org/10.1109/TED.2005.864392
16. Lee H, Lee CH, Park D, Choi YK (2005) A study of negative-bias temperature instability of SOI and body-tied FinFETs. IEEE Electron Device Lett 26:326–328. https://doi.org/10.1109/LED.2005.846587
17. Bansal A, Mukhopadhyay S, Roy K (2007) Device-optimization technique for robust and low-power FinFET SRAM design in NanoScale era. IEEE Trans Electron Devices 54:1409–1419. https://doi.org/10.1109/TED.2007.895879
18. Tripathi S, Narendar V (2015) A three-dimensional (3D) analytical model for subthreshold characteristics of uniformly doped FinFET. Superlattice Microst 83:476–487. https://doi.org/10.1016/j.spmi.2015.03.048
19. Narendar V, Mishra RA (2015) Analytical modeling and simulation of multigate FinFET devices and the impact of high-k dielectrics on short channel effects (SCEs). Superlattice Microst 85:357–369. https://doi.org/10.1016/j.spmi.2015.06.004
20. Long W (1999) Dual-material gate (DMG) field effect transistor. IEEE Trans Electron Devices 46:865–870. https://doi.org/10.1109/16.760391
21. Reddy NN, Panda DK (2020) Simulation study of dielectric modulated dual material gate TFET based biosensor by considering Ambipolar conduction. Silicon. https://doi.org/10.1007/s12633-020-00784-9
22. Reddy NN, Panda DK (2021) Performance analysis of Z-shaped gate dielectric modulated (DM) tunnel field-effect transistor-(TFET) based biosensor with extended horizontal N+ pocket. Int J Numer Model Electron Netw Devices Fields 34: e2908. https://doi.org/10.1002/jnm.2908
23. Reddy NN, Panda DK (2021) Nanowire gate all around-TFET-based biosensor by considering ambipolar transport. Appl Phys A Mater Sci Process:127, 1–129. https://doi.org/10.1007/s00339-021-04840-y
24. Chaudhry A, Kumar MJ (2004) Controlling Short-Channel effects in deep-submicron SOI MOSFETs for improved reliability: a review. In: IEEE Transactions on Device and Materials Reliability. pp. 99–109
25. Narendar V, Girdhardas KA (2018) Surface potential modeling of Graded-Channel gate-stack (GCGS) high-K dielectric dual-material double-gate (DMDG) MOSFET and analog/RF performance study. Silicon 10:2865–2875. https://doi.org/10.1007/s12633-018-9826-z
26. Vadthiya N, Tripathi S, Naik RBS (2018) A two-dimensional (2D) analytical modeling and improved Short Channel performance of Graded-Channel gate-stack (GCGS) dual-material double-gate (DMDG) MOSFET. Silicon 10:2399–2407. https://doi.org/10.1007/s12633-017-9683-1
27. Narendar V, Rai S, Tiwari S (2016) A two-dimensional (2D) analytical surface potential and subthreshold current model for the underlap dual-material double-gate (DMDG) FinFET. J Comput Electron 15:1316–1325. https://doi.org/10.1007/s10825-016-0899-x
28. Narendar V, Rai S, Tiwari S, Mishra RA (2016) A two-dimensional (2D) analytical subthreshold swing and transconductance model of underlap dual-material double-gate (DMDG) MOSFET for analog/RF applications. Superlattice Microst 100:274–289. https://doi.org/10.1016/j.spmi.2016.09.028
29. Narendar V, Narware P, Bheemudu V, Sunitha B (2020) Investigation of Short Channel effects (SCEs) and analog/RF figure of merits (FOMs) of dual-material bottom-spacer ground-plane (DMBSGP) FinFET. Silicon 12:2283–2291. https://doi.org/10.1007/s12633-019-00322-2
30. Meriga C, Ponnuri RT, Satyanarayana BVV, Gudivada AAK, Panigrahy AK, Prakash MD (2021) A novel teeth junction less gate all around FET for improving electrical characteristics. Silicon:1–6. https://doi.org/10.1007/s12633-021-00983-y
31. Prakash MD, Nelam BG, Ahmadsaidulu S, Navaneetha A, Panigrahy AK (2021) Performance analysis of ion-sensitive field effect transistor with various oxide materials for biomedical applications. Silicon. https://doi.org/10.1007/s12633-021-01413-9
32. Vadthiya N (2021) Design and deep insights into Sub-10 nm spacer engineered Junctionless FinFET for nanoscale applications. ECS J Solid State Sci Technol 10:013008. https://doi.org/10.1149/2162-8777/abddd4
33. Vakkalakula BS, Vadthiya N (2021) P-type Trigate Junctionless Nanosheet MOSFET: analog/RF, linearity, and circuit analysis. ECS journal of solid state. Sci Technol 10:123001. https://doi.org/10.1149/2162-8777/ac3bdf
34. Sreenivasulu VB, Narendar V (2021) Characterization and optimization of junctionless gate-all-around vertically stacked nanowire FETs for sub-5 nm technology nodes. Microelectron J 116:105214. https://doi.org/10.1016/j.mejo.2021.105214
35. Yu B, Chang L, Ahmed S, et al (2002) "FinFET scaling to lOnm gate length" digest. Int Electron Devices Meeting, IEEE
36. Semiconductor Industry Association (2016) International Technology Roadmap for Semiconductors, 2015 Results. Itrpv 1–37
37. Sreenivasulu VB, Narendar V (2022) Junctionless SOI FinFET with advanced spacer techniques for sub-3 nm technology nodes. AEU Int J Electron Commun 145:154069. https://doi.org/10.1016/j.aeue.2021.154069
38. Sreenivasulu VB, Narendar V (2021) Performance improvement of spacer engineered n-type SOI FinFET at 3-nm gate length. AEU Int J Electron Commun 137:153803. https://doi.org/10.1016/j.aeue.2021.153803