A NOVEL BULK-FINFET WITH DUAL-MATERIAL GATE

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ABSTRACT

A bulk-FinFET with dual material gate called DMG-Bulk-FinFET is proposed in this paper. Its characteristics are compared to the normal bulk-FinFET using 3-D simulations. It is demonstrated that the new structure has the features in suppressing the short channel effects, improving transconductance and enhancing the carrier transport efficiency. Moreover, these features can be optimized by engineering the gate length ratio and workfunction difference. This work illustrates the better performance of the DMG-Bulk-FinFET than its counterpart with single material gate and presents an optimization design of the DMG structure.

INTRODUCTION

With the scaling of CMOS devices, traditional MOSFET presents more and more severe short channel effects (SCEs). A lot of new structures have been proposed to replace traditional MOSFET at the deep submicron node. FinFET, proposed by professor Hu Chenming in 1999, is widely recognized as the most promising candidate compared to other new structures[1]. The vertical double gates in FinFET enhance the controllability upon the channel region, so that it suppresses the SCEs effectively. Furthermore, FinFET is a quasi-planar structure compatible with the conventional CMOS process[2].

However， the conventional FinFET is a typical multi-gate structure and could not increase the carrier transport efficiency[3]. A useful technology to improve the carrier transport efficiency is Dual Material Gate (DMG) technology, which combines two gates of different materials with different workfunctions[3]. The deceasing workfunction from source to drain in DMG structure can improve both SCEs and carrier transport efficiency. The DMG technology has been incorporated into bulk/SOI MOSFETs, double-gate MOSFETs, surrounding-gate MOSFETs, SOI FinFETs, tunnel FETs and junctionless nanowire transistors[4-9].

In this paper, we investigate the feasibility and advantages of DMG in a bulk-FinFET using the 3-D simulator Davinci.

DEVICE STRUCTURE

A 3-D schematic view of the device called DMG-Bulk-FinFET is shown in Fig.1. The fin Length, width and height are 100nm, 50nm and 20nm, respectively. Top oxide thickness and side oxide thickness are 10nm and 3nm respectively in order to produce a vertical double-gate FinFET. The doping in the p-type fin, n+ type source/drain regions and p-type substrate are kept at 3.5×10^{16}, 5×10^{19} and 1×10^{15} cm^{-3}, respectively. As shown in Fig.1, *GATE1* near the source and *GATE2* near the drain have lengths L_1 and L_2 and workfunctions W_1 and W_2, respectively.

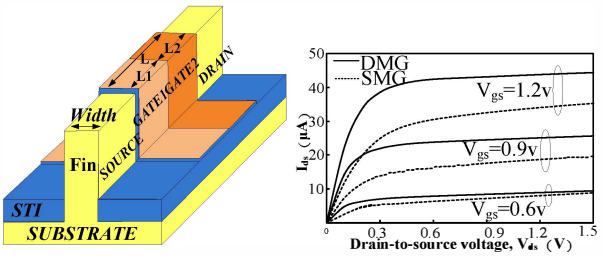

Fig.1: 3-D DMG-Bulk-FinFET schematic view.
Fig.2: Output characteristics of a DMG-Bulk-FinFET compared to SMG counterpart with the same size and V_{th}.

RESULTS AND DISCUSSION

In this section, we have compared the performances of DMG-Bulk-FinFET and Single-Material gate (SMG) bulk-FinFET with the same size. Then, the effects of two main parameters of DMG structure L_1/L ratio and workfunction difference are analyzed and optimized

Performance Comparison with SMG-Bulk-FinFET

Output characteristics of a DMG-Bulk-FinFET and a SMG-Bulk-FinFET with the same size are compared in Fig.2. The workfunction of the SMG-Bulk-FinFET gate is 4.4eV, while workfunctions of the DMG-Bulk-FinFET are W_1 of 4.8eV and W_2 of 4.4eV, respectively. The lengths of the DMG gates are L_1=L_2=50nm. For the comparability, the fin doping concentrations in the DMG device and SMG device are designed as 3.5×10^{16} cm^{-3} and $1.546\times10^{18}cm^{-3}$, to obtain the same threshold voltage (V_{th}) of 0.46V[9].

As shown in Fig.2, the DMG-Bulk-FinFET has better output performance than the SMG-Bulk-FinFET at different drain-to-source voltages (V_{ds}). This is due to the enhancement of electron transport efficiency in the channel region by applying DMG structure to bulk-FinFET.

In order to understand the physical mechanisms for the performance improvements of the new structure, the distributions of its potential, electric field and mean electron velocity in the fin region are shown in Fig.3-5.

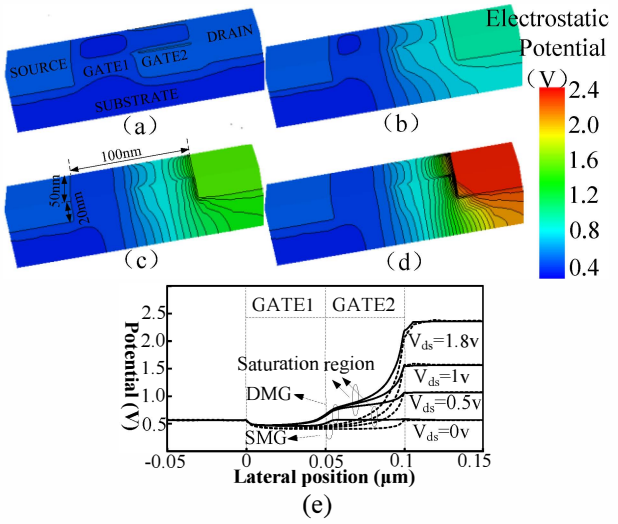

Fig.3: 3-D distributions of potential of a DMG-Bulk-FinFET at V_{ds}=(a) 0V, (b) 0.5V, (c) 1V, (d) 1.8V. (e)potential at the sidewall of the fin (channel region), solid line for DMG, dashed line for SMG with W of 4.4eV.

The 3-D potential distributions are shown in Fig.3(a)-(d) at various drain biases of 0V, 0.5V, 1V and 1.8V. It is observed that the potential under *GATE1* is insensitive to the drain biases, while the potential under GATE2 increases as the drain bias increases. Fig.3(e) compares the lateral surface potential distributions for the DMG-Bulk-FinFET and SMG-Bulk-FinFET. For the SMG device, surface potential increases linearly with the increase of drain bias as the dashed curves represent. However, for the DMG device, when the device operates at the saturation region(V_{ds} is above 0.3V shown in Fig.2), potential under *GATE1* is almost immune to the drain voltage. Such a screen to the drain voltage variations leads to a strong suppression to the drain induced barrier lowering (*DIBL*) effects.

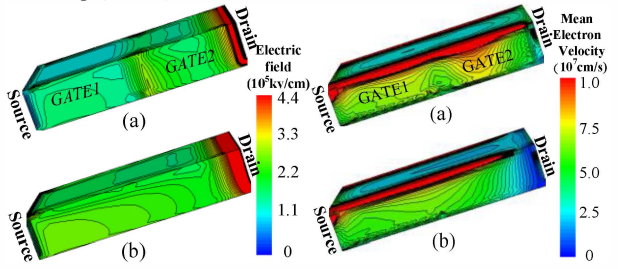

Fig.4: 3-D distributions of electric field of a (a) DMG-Bulk-FinFET, and (b) SMG-Bulk-FinFET.
Fig.5: 3-D distributions of mean electron velocity of a (a) DMG-Bulk-FinFET, (b) SMG-Bulk-FinFET.

Fig.4 shows the comparison of the electric field distributions in the silicon fin of the DMG-Bulk-FinFET and the conventional SMG-Bulk-FinFET. There is a new electric field peak at the joint of *GATE1* and *GATE2* of the fin in the DMG device. Fig.5 shows that such a peak increases the mean electron velocity near the source in the channel and thus improves the carrier transport efficiency compared to the SMG device.

Effects of L_1/L ratio at a fixed channel length L

Characteristics variations are studied for different values of L_1/L ratio at a fixed L in terms of V_{th}, *DIBL*, Subthreshold swing (*SS*), on-state current (I_{on}), off-state current (I_{off}), output conductance (G_d), transconductance (G_m), and voltage gain G_m/G_d. Workfunctions of *GATE1* and *GATE2* are set to 4.8eV and 4.4eV, respectively.

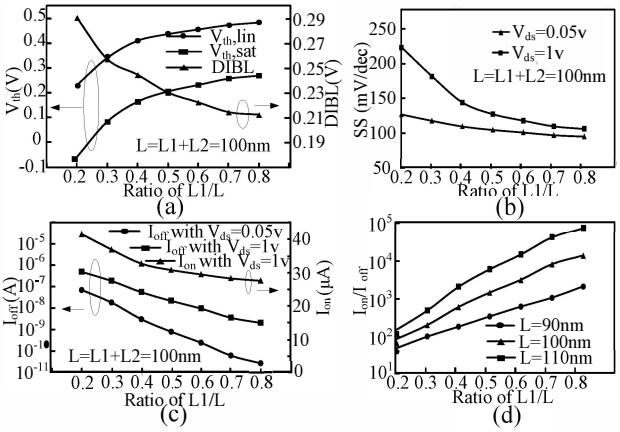

Fig.6: Variation of (a) Vth(extracted from linear region and saturation region, respectively) and DIBL, (b) SS, (c) I_{on} and I_{off}, (d) I_{on}/I_{off} with L_1/L ratio at a fix L.

It is observed from Fig.6 (a) that V_{th} increases as L_1 increases and L_2 decreases at a fixed L no matter when the device operates at linear or saturation region. We can consider it as a gradual transition from a SMG device with lower gate workfunction 4.4eV to a SMG device with higher gate workfunction 4.8eV. Moreover, *DIBL* (defined as the difference between V_{th} extracted at V_{ds}=0.05V and V_{ds}=1V) and *SS* decrease with the increase of L1, as shown in Fig.6(a) and (b). That presents that the higher workfunction of the gate metal helps suppress SCEs.

Fig.6(c) presents I_{on} and I_{off} as the function of the L_1/L ratio for the total gate length of 90nm, 100nm and 110nm. For the increasing L_1/L, I_{on} decreases approximately linearly while I_{off} decreases exponentially. As a result, I_{on}/I_{off} exhibits an increasing trend exponentially when L_1/L ratio increases.

It is observed from Fig.7 that L_1/L ratio also affects G_m, G_d, and voltage gain. G_m reaches its maximum while G_d reaches its minimum when L_1/L ratio is 0.2 at various total gate lengths as shown in Fig.7(a). Hence, the device

of which L_1/L is 0.2 has the largest voltage gain G_m/G_d.

For the DMG device with L of 100nm, maximum of Gm is 71.49μS, 83.1% larger than that of the SMG device with W of 4.4eV, which is only 39.04μS. And it is 24.8% larger than it of a SMG device with W of 4.8eV, which is just 57.29μS.

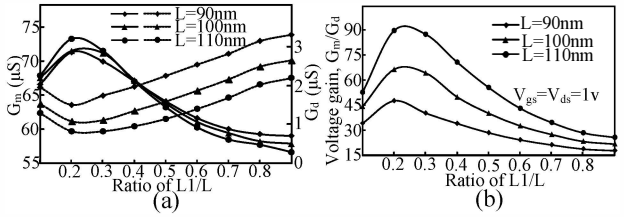

Fig.7: Variation of (a)G_m and G_d, (b) voltage gain with L_1/L ratio at a fix L

Effects of δW at a fixed W_2

Another important factor to design the DMG-Bulk-FinFET is the workfunctions of the gate materials. Fig. 8 illustrates the operating characteristics of the DMG-Bulk-FinFET varied with the workfunction W_1 and W_2 when L_1 and L_2 are fixed at 50nm.

As shown in Fig.8(a), at a fixed W_2 of 4.4eV, V_{th} and *DIBL* increase with the increasing W_1 from 4.5eV to 5.3eV. However, *SS* decreases as δW increases in Fig.8(b). It is also observed from Fig.8(c) that I_{on} and I_{off} exhibit the linear and exponential reduction trends with the increase of δW, respectively. Hence, on-off current ratio I_{on}/I_{off} approximately exponentially increases with increasing δW for the various W_2 , as shown in Fig.8(d).

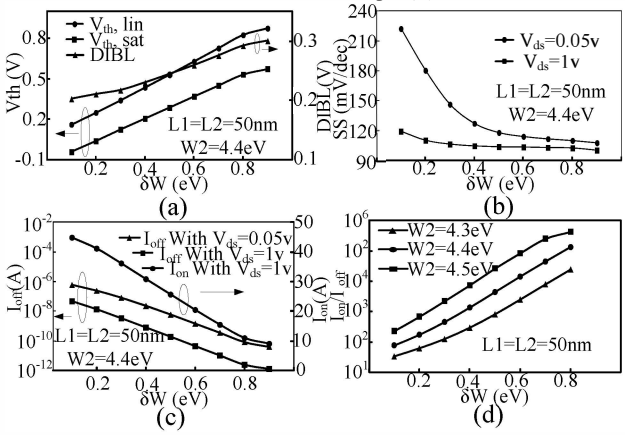

Fig.8: Variation of (a) V_{th} (extracted from linear region and saturation region, respectively) and DIBL, (b)SS, (c)I_{on} and I_{off}, (d) I_{on}/I_{off} with δW at a fixed W_2

Fig.9 shows the G_m and G_d as the function of δW. G_m increases before it reaches its maximum at δW=0.3eV, then it decreases as δW increases, while G_d exhibits oppositely. G_m of the DMG device with W_2 of 4.4eV and W_1 of 4.7eV is 62.6μS, 60.3% higher than that of a SMG device with W of 4.4eV, and 10% higher than that of a SMG device with W of 4.7eV.

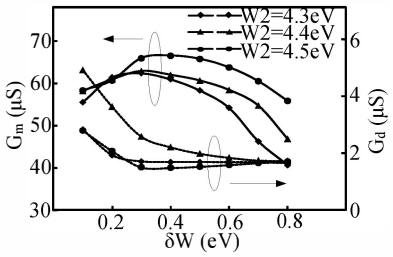

Fig.9: Variation of G_m and G_d with δW at a fixed W_2

CONCLUSION

In this paper, a new structure called DMG-Bulk-FinFET has been proposed and studied using 3-D numerical simulations. The results show that the application of DMG structure exhibits excellent properties, such as SCEs suppression, G_m improvement, and carrier transport efficiency enhancement compared to the conventional Bulk-FinFET. Simulation results indicate the optimum gate length ratio L_1/L=0.2 and workfunction difference δW=0.3eV which are recommended for the DMG-Bulk-FinFET design.

ACKNOWLEDGEMENTS

The present work was supported by the National Natural Science Foundation of China (Grant No. 61076073), and the Specialized Research Fund for the Doctoral Program of Higher Education of China (No. 20133223110003)

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