Silicon (2022) 14:9821–9831
https://doi.org/10.1007/s12633-022-01695-7

ORIGINAL PAPER

Performance Evaluation of GAA Nanosheet FET with Varied Geometrical and Process Parameters

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Received: 7 October 2021 / Accepted: 17 January 2022 / Published online: 8 February 2022

Abstract
Nanosheet Field Effect Transistor (NSFET) is a viable contender for future scaling in sub-7-nm technology. This paper provides insights into the variations of DC FOMs for different geometrical configurations of the NSFET. In this script, the DC performance of 3D GAA NSFET is analyzed by varying the device's width and thickness. Moreover, the gate length is scaled from 20 nm to 5 nm to check for the device suitability for continuous scaling in logic applications. The thickness and width of each nanosheet are varied in the range of 5 to 9 nm and 10 to 50 nm, respectively, to analyze the performance dependency on the geometry of the device. The impact of geometry of NSFET on various DC performance metrics like transfer characteristics, sub-threshold swing (SS), on current (I_{ON}), off current (I_{OFF}), switching ratio (I_{ON}/I_{OFF}), threshold voltage (V_{th}), and drain induced barrier lowering (DIBL) are studied. On top of that, the device's electrical characteristics are analyzed for a wide range of temperatures from -43°C to 127°C to identify the temperature compensation point and is observed at $V_{GS} = 0.55$ V and $I_D = 3.86 \times 10^{-6}$ A. Furthermore, the vital process parameter, work function variations on transfer characteristics of the device is analyzed. Moreover, the analyses reveal that, for sub -7 nm, the NSFET is a potential device for high performance and suitable for logic applications.

Keywords Nanosheet · GAA · SCEs · Process Variations · Scaling · Sub -7 nm

1 Introduction

From the past five decades, the semiconductor industry has taken major steps in designing to improve the performance of semiconductor devices. This possibility is achieved by continuous downscaling of the device dimensions. By decreasing the device dimensions, the number of transistors increased on-chip which in turn increased the performance of the device. According to Moor's Law for every eighteen months, there is a two-fold increase in the number of transistors. This device downscaling has advantages like less power consumption, high speed and reduction in cost [1–7]. The device dimensions are reduced in every successive technological node. For every technological node, the channel length is reduced and is now reached atomic dimensions. The distance between the source and drain will decrease as the channel length decreases and they are in close proximity with each other [8, 9]. As a consequence of this, the lateral electric field from the source and drain starts affecting the channel in addition to the vertical electric field from the gate. This phenomenon introduces the disadvantageous short channel effects (SCEs) in orthodox MOSFETs. As the gate length is decreasing the gate loses its control over the channel which gives scope for Short Channel Effects (SCEs) and leakage currents. Some of the short channel effects are threshold voltage roll-off, drain induced barrier lowering (DIBL), hot electron effects etc [10–13]. To alleviate these SCEs and continue further scaling, researchers came up with various device engineering such as channel engineering, doping variations, device architectural engineering, gate engineering etc., The influence of doping concentration beneath the gate on the scaling feasibility of sub-10-nm junctionless carbon nanotube field-effect transistors is explored in [14]. To improve I_{ON} and to have ease of fabrication, a new structure called VSTB FET discussed in [15–17],

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in which one or more dielectric layers stabilize a thin vertical body, lowering the likelihood of thin fin breaking.

To have good electrostatic integrity, the gate control on the channel should be enhanced and to achieve this, devices with multiple gates are one of the viable options. Double Gate, Trigate, FinFET and Gate All Around (GAA) nanosheet and nanowire structures are the example of multigate devices [18–26].

To get more drive current, FinFETs need tall and thin fins which increase the cost and complexity of fabrication of the device [27]. In GAA structures the gate wraps around the channel in all directions and offers potential control over the channel by the gate. However, it is noticed that the GAA stacked nanowire performance is degraded by the surface roughness factor [28]. Moreover, due to the smaller effective widths, the drive current in nanowire structures is limited [29]. Though the fabrication industries adopted FinFETs for sub 22 nm, due to aggressive scaling it is inefficient for sub 10 nm nodes. For sub 7nm technology node and beyond the GAA NSFET structures emerged as potential contenders for conventional FinFETs because of their excellent control on channel region and are successors of FinFETs due to better leakage control and high current drive capability. Also, NSFETs are immune to short channel effects because of their good electrostatic control over channel [30]. Compared to nanowire and FinFET structures, NSFETs have shown superior electrostatic performance on channel [31]. By introducing minimal changes to the fabrication of FinFET, NSFET can be fabricated; a five-stack nanowire FET is fabricated and presented in the literature [32]. Compared to FinFET or stacked nanowires, single stack NSFET offers greater intrinsic performance for any sheet width. Moreover, NSs also have a greater effective width in a given footprint, making them better at driving capacitive loads [33].

The continuous thinning of gate oxide (SiO_2) with scaling reached to its physical limit and gives scope to leakage through gate. To mitigate this leakage, researchers came up with the solution of using high-k materials in gate stack in addition to gate oxide. The performance of the device with various high-k dielectrics reported in the literature and is shown that the gate leakage can be reduced further by introducing high-k materials in the gate stack [34–36]. For every upcoming generation, in addition to increment in on current, there is a threefold increment in off current which increases power consumption [37]. To circumvent this new device engineering called SOI technology is introduced. Moreover it is reported that SOI FinFETs have better electrostatic integrity than bulk FinFETs, resulting in increased performance and lower variability [38]. Moreover, it is reported that fabrication related issues with that bulk devices such as etching of fin, deposition of isolation oxide can overcome by using SOI structures [39].

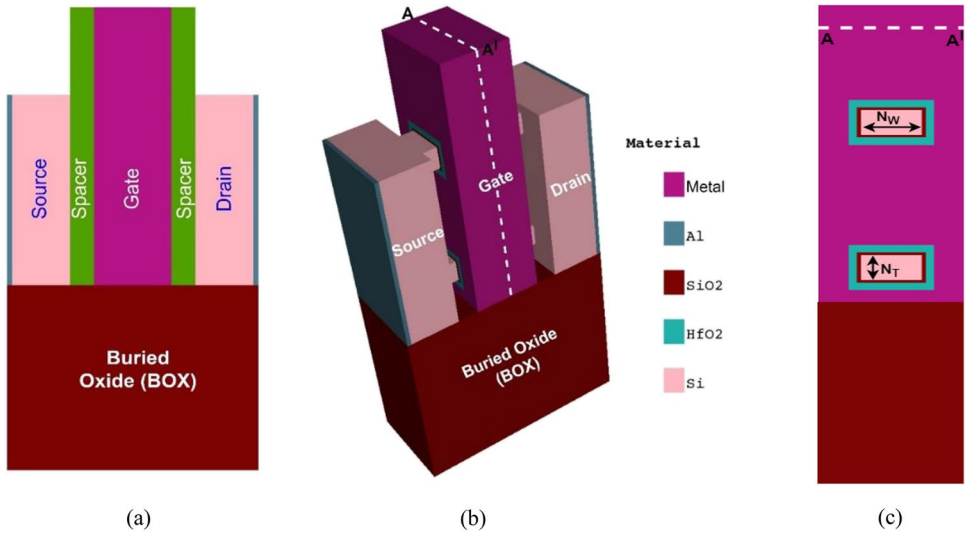
Increasing the number of stacked nanosheet channels to maximize the drive current is a better option, but the larger height of the device exacerbates parasitic capacitances [29]. So, in this paper, vertically stacked GAA NSFET with two nanosheets is designed and simulated for performance evaluation. As the geometry of the device plays crucial role in determining the device's performance, the nanosheet width, thickness is varied in addition to the gate length to observe the performance variations. On top of that, the temperature analyses in done to identify the temperature compensation point, which helps to get optimum performance of the device irrespective of temperature variations of the device.

In this script, the simulation of SOI NSFET is done by using a high-*k* gate stack to maintain superior electrostatic gate control at 300 K. The rest of the document is structured as follows. Section 2 presents the device parameters description and physical models incorporated for simulation. The performance dependence on various parameters is analysed in section 3, Section 4 concludes and gives a summary of this paper.

2 NSFET Structure and Simulation Procedure

The device structure of the NSFET is generated by using the Cogenda Genius 3D TCAD simulator [40]. The 3D NSFET with gate length (L_G) of 16 nm, each sheet thickness (N_T) of 5 nm, and sheet width (N_W) of 10 nm is generated and simulated. The n-type source/drain and p-type channel regions are doped with a doping concentration of 10^{20} cm^{-3} and 10^{15} cm^{-3} respectively. For a high-k gate stack, to get an effective oxide thickness (EOT) of 0.78 nm, thickness values of 0.5 nm and 1.5 nm are considered for SiO_2 and HfO_2 respectively. To ensure better electrostatic integrity, the EOT of 0.78 nm and gate work function of 4.6 eV are taken for all simulations. As the continuous scaling of the device leads to abnormal SCEs, spacers are incorporated to improve the short channel performance of the device. However, the drive current is degraded due to an increase in series resistance in the underlap sections. By using high-k spacers in the underlap area, series resistance can be lowered and drive current can be increased. Various high-k materials like Si_3N_4 and HfO_2 are explored in the literature and is reported that by using Si_3N_4 spacer, the static power consumption reduced compared to other spacer materials [41]. To improve the sub threshold behaviour, a nitride spacer with a length of 5 nm is maintained throughout the simulations [42].

Figure 1(a) depicts the 2-D NSFET with Nitride spacer. The 3-D view of NSFET with stacked nanosheets is shown in Fig. 1(b). 2-D view of NSFET with N_T and N_W is depicted in Fig. 1(c).



(a) (b) (c)

Fig. 1 (a) 2-D view of NSFET with nitride spacer, (b) 3-D schematic view of NSFET and (c) 2-D cross section view of NSFET

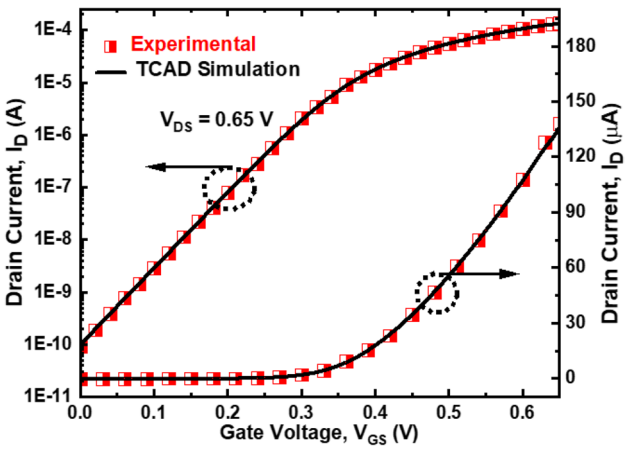


Fig. 2 Calibration of simulation models with that of experimental results [33]

The device is well calibrated using [33, 43]. The models incorporated for simulation are as follows. To account for higher doping concentrations, Fermi Dirac statistics are involved. To consider the effects of generation and recombination of carriers, the Shockley-Read-Hall (SRH) recombination model is involved. To account for the scattering phenomena like acoustic phonons and surface roughness, the Lombardi mobility model is included. The models used for simulations are calibrated with experimental results and the transfer characteristics are presented in Fig. 2. Table 1 gives the information of different parameters considered for simulation.

Table 1 Device parameters used in simulation

Device Parameter	Value
Nanosheet thickness (nm)	5-9
Nanosheet width (nm)	10-50
Gate length (nm)	5 - 20
Source/Drain doping (cm^{-3})	10^{20}
Channel doping (cm^{-3})	10^{15}
EOT (nm)	0.78
Spacer dielectric	Nitride
Source/Drain length (nm)	12
Underlap spacer length (nm)	5
Work function of gate (eV)	4.6
Height of the gate (nm)	60

3 Result Analysis

3.1 Comparison Between SOI NSFET and Bulk NSFET

Figure. 3 illustrates the transfer characteristics of both SOI and bulk NSFET devices. It can be seen from the figure that the I_{OFF} of the bulk NSFET is more than that of SOI NSFET and a marginal increment in I_{ON} is observed in SOI due to higher mobility [44]. Moreover the steep sub threshold slope can be achieved by SOI as shown in Fig. 3. There is an increment of 100x in I_{ON}/I_{OFF} of SOI compared to bulk NSFET which gives good logic performance of the device. Considering all these advantages of SOI substrate, the performancy dependency of SOI NSFET on geometry, temperature and work function variations are presented in the rest of the paper.

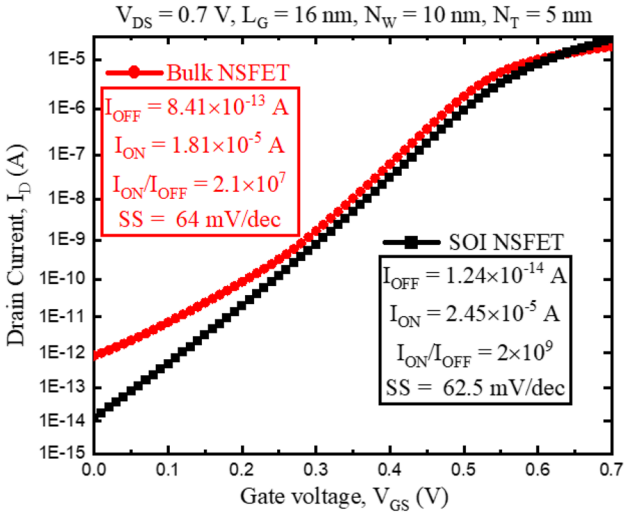


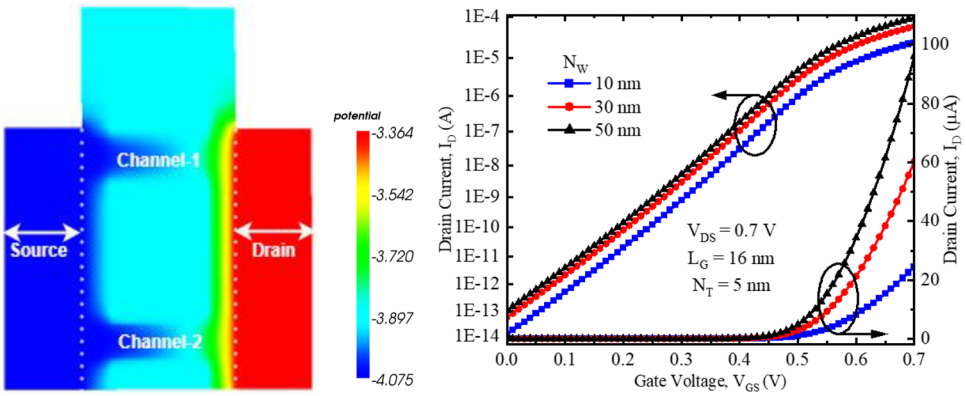
Fig. 3 Comparison between SOI NSFET and bulk NSFET

3.2 Impact on DC Performance of NSFET with Geometric Variations

The DC performance of NSFET is analysed by changing the NS physical dimensions like width and thickness. The N_W varied from 10 nm to 50 nm and N_T is varied from 5 nm to 9 nm. In this section, the key performance parameters like on current, off current, switching ratio, threshold voltage (V_{th}), DIBL, and SS are discussed.

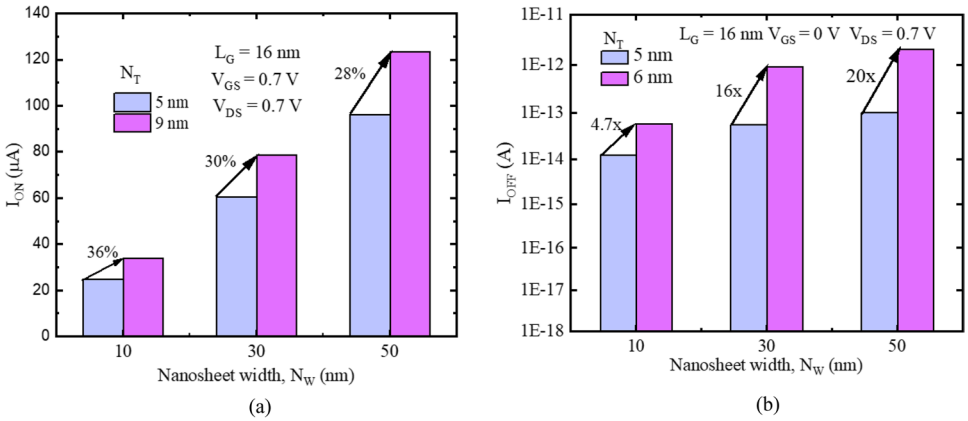
The Contour plot of the potential distribution of NSFET is shown in Fig. 4(a). It can be observed that the potential distribution at the drain side is high compared to the source side. Also, it can be clearly seen that the drain potential impact on the channel is reduced because of the spacer. Fig. 4(b) depicts transfer characteristics in both linear and log scales for various widths of nanosheet at $V_{DS} = 0.7$ V for constant N_T of 5 nm.

Channel width controls the amount of flow of current through the NSFET. The I_{ON} is directly proportional to the effective width of the channel, which leads to an increment in the I_{ON} as the width of the sheet increases. From Fig. 5 (a), it can be seen that the maximum increment of 36% in I_{ON} is observed when the thickness is increased from 5 nm to 9 nm at nanosheet width of 10 nm. It is observed that for larger widths of nanosheet, higher I_{ON} is obtained due to the increment of effective width of nanosheet. On the other hand, in addition to the increment in I_{ON}, the increment in the I_{OFF} also observed. As the width of the channel increases, the gate loses its control on the channel and leads to more



(a) (b)

Fig. 4 (a) Contour plot of the potential distribution of NSFET in ON state (b) Transfer characteristics of NSFET in linear and log scale for $V_{DS} = 0.7$ V



(a) (b)

Fig. 5 (a) I_{ON} and (b) I_{OFF} as a function of N_W for various N_T values

leakages in the device. These leakages will increase the I_{OFF} of the device. Moreover, the increment in I_{OFF} is observed for higher thickness values of nanosheet because of reduction in potential barrier height, conduction band energy in the channel for off state condition [43].

For thinner nanosheets off state current can be reduced, however, the slight reduction in the I_{ON} is observed because of the mobility degradation due to enhancement in the perpendicular electric field [43]. These results are shown in Fig. 5(b). The maximum increment of 20x in off current is observed for thickness from 5 nm to 9 nm at nanosheet width of 50 nm.

Figure 6(a) shows I_{ON}/ I_{OFF} and SS values for different widths of nanosheet. As the N_W increases, the switching ratio followed decreasing manner because of the raise in off current. Moreover, as the width increases, there is a decrement of 71% and 94% in switching ratio is observed for thickness values of 5 nm and 9 nm respectively. It can be observed that the switching performance of the device gets deteriorated with the increment in geometrical values.

Sub-threshold swing (SS) is an important metric for device application in logic circuits. The SS is defined as the change in the gate voltage needed to get a decade change in drain current. The Sub-threshold swing (SS) can be calculated by using the formula (1) [45]

$$SS = \left(\frac{\partial \log_{10} I_D}{\partial V_{GS}}\right)^{-1} \tag{1}$$

From Fig. 6(a), it can be seen that for more width, SS followed an increasing manner since the gate loses its control over the channel. Furthermore, as the width varies from 10 nm to 50 nm, there is an increment of 1.6% and 8.5% in SS is observed for thickness values of 5 nm and 9 nm respectively. Since a lower value of SS is preferred for good sub threshold performance, nanosheet having width and height of 10 nm and 5 nm respectively outperforms with SS of 62.5 mV/dec, which is near to ideal SS.

Fig. 6(b) depicts DIBL and V_{th} for different widths of nanosheet. The threshold voltage is extracted by using the constant current method at 100× W_{eff} /L_G. Where W_{eff} is given by n × (2× (T + W)), where T and W are the thickness and the width of the nanosheet respectively. The term n indicates the number of vertically stacked nanosheets [42, 46]. As the thickness and width of the nanosheet are increasing, from Fig. 6(b), it can be seen that the threshold voltage is reducing because of SCEs. Furthermore, there is a threshold voltage roll-off of 5.3% and 8% is observed for thickness values of 5 nm and 9 nm respectively when the nanosheet width is varied from 10 nm to 50 nm. It can be seen that the V_{th} roll-off is more for higher thickness values of nanosheet.

Drain induced barrier lowering (DIBL) is also one of the crucial sub-threshold performance metrics and it should be as low as possible for good performance of the device. The DIBL is computed by using the equation (2) [47].

$$DIBL = \frac{V_{tlin} - V_{tsat}}{V_{Dsat} - V_{Dlin}} \tag{2}$$

Here, V_{tlin} is the threshold voltage extracted at linear supply voltage, V_{Dlin} = 0.04 V and V_{tsat} is threshold voltage extracted at saturation supply voltage, V_{Dsat} = 0.7 V. It can be observed that, as the nanosheet dimensions are increasing, the DIBL gets increasing. Moreover, as the N_W increased from 10 nm to 50 nm, there is an increment of 24% and 30% in DIBL observed for nanosheet thickness values of 5 nm and 9 nm respectively. The DIBL can be lowered by incorporating the nanosheets which are having smaller widths and thickness values. The results show that DIBL is sensitive towards width and thickness variations.

Fig. 7 shows the output characteristics for various Nanosheet width values with respect to drain voltage at a fixed gate voltage of 0.7 V. It is observed that as the N_W increases, the drain current increases due to the increment in effective width.

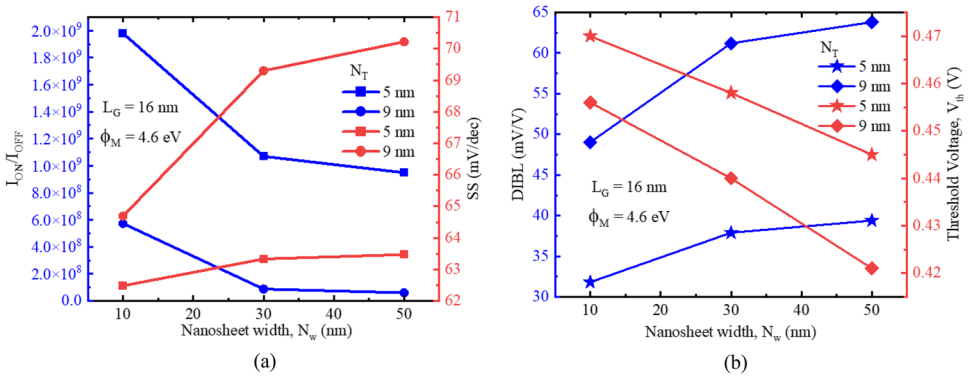


Fig. 6 (a) I_{ON}/ I_{OFF} and SS (b) DIBL and V_{th} as a function of N_W for various N_T values

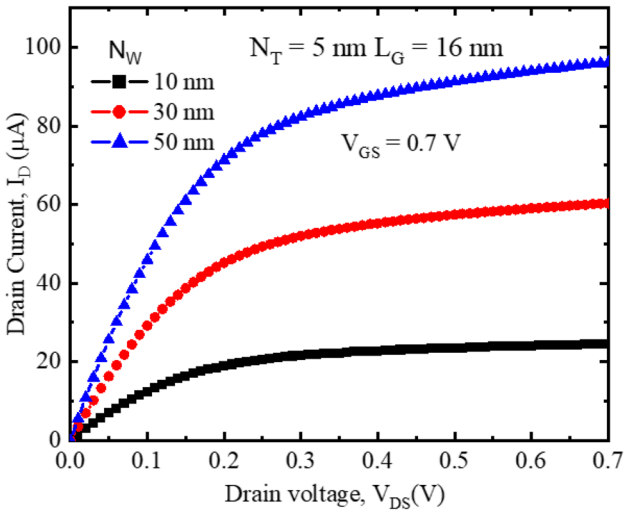


Fig. 7 Output characteristics for various N_W values as a function of drain voltage

3.3 Impact on DC Performance of NSFET with Scaling

In this section, the impact of scaling on the DC performance of NSFET is analysed for sub -7 nm technology nodes. The gate length is downscaled from 20 nm to 5 nm and the results are depicted in Fig. 8(a). The transfer characteristics are obtained by fixing the thickness to 5 nm and width to 10 nm for the nanosheet.

From Fig. 8(b), it is observed that as the channel length decreases, the on current is increased since the distance between source and drain is decreased. However, the OFF current also increased due to the SCEs.

Fig. 9(a) depicts the I_{ON}/I_{OFF} and SS as a function of the gate length. It can be seen that as the channel length is decreasing, the switching ratio has deteriorated. However, even at L_G of 5 nm, the switching ratio of 10^6 is maintained which ensures that NSFET is a suitable candidate for good logic applications and continued scaling [29, 48]. Moreover, as the gate length decreasing, the SS is increased and there is an increment of 31% is observed as the gate length is scaled from 20 nm to 5 nm. The increment in SS is due to an increment in leakage currents. DIBL and V_{th} are shown in Fig. 9(b). DIBL is another parameter that affects severely with scaling. As the gate length decreases, the impact of drain potential is more on the channel and leads to the increment of DIBL. From Fig. 9(b), it can be seen that the DIBL is increased and a growth rate of 339% is observed as the gate length ranging from 20 nm to 5 nm. The threshold voltage variations as a function of gate length are depicted in

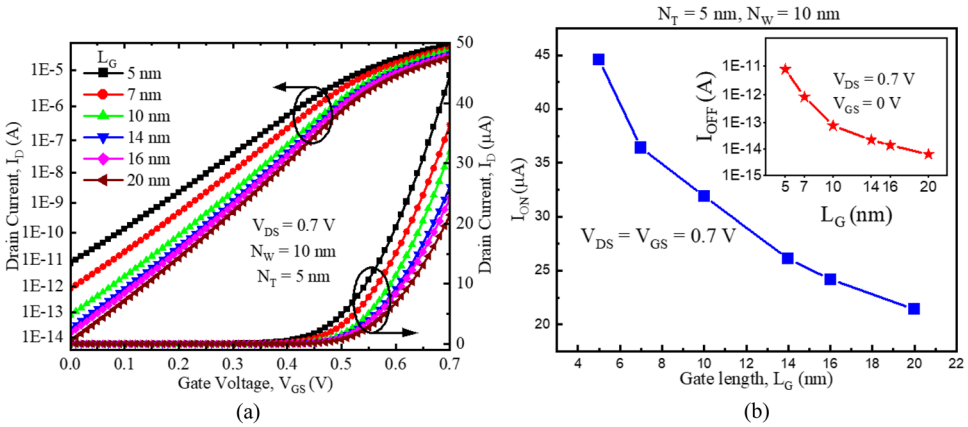


Fig. 8 (a) Transfer characteristics for various L_G values and (b) I_{ON} and I_{OFF} (inset) as a function of L_G

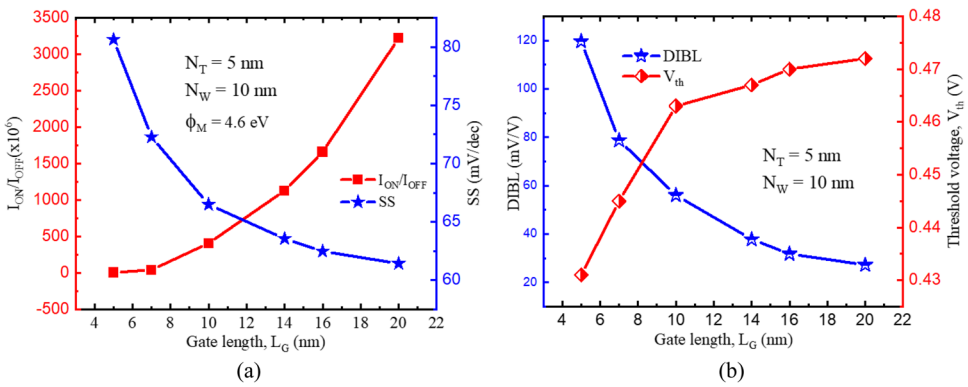


Fig. 9 (a) I_{ON}/I_{OFF} and SS (b) DIBL and V_{th} as a function of L_G

Fig. 9(b). The deterioration in threshold voltage is observed as the gate length is increasing due to the threshold voltage roll-off. As the gate length decreased from 20 nm to 10 nm, a reduction of 1.9% in threshold voltage is observed, whereas from 10 nm to 5 nm, a reduction of 7% is observed. It is obvious that for sub -10 nm, the threshold voltage roll-off is more due to increased SCEs.

The drain current variations with respect to drain voltage are depicted in Fig. 10. It can be seen that as the gate length decreasing, the drain current is improved. However the slope in the saturation region is increases with scaling which lowers the driving capacity of the device.

3.4 Impact of Temperature and Work Function Variations on NSFET

Nanoscale transistors are used in a wide variety of fields like communication, automobiles, medical equipment, analog and digital integrated circuits, sensing applications and power electronics. As per the requirement, the nano transistors are used at different temperatures and are crucial to analyze the performance of transistors at various ranges of temperatures [49].

Temperature dependency on drain current as a function of gate voltage is plotted in Fig. 11(a). The temperature is varied in the range of -43°C to 127°C. It is very much required to bias these circuits so that the performance or V-I characteristics are insensitive or independent towards temperature variations. IC designers are very much interested to know this inflection point of temperature. This biasing point is called the temperature compensation point (TCP) [50]. From Fig. 11 (a), the TCP is observed at $V_{GS} = 0.55$ V and $I_D = 3.48\times10^{-6}$ A. From Fig. 11(b), it is clear that as the temperature increases, increment in off currents is observed because of the dominance of impurity scattering. Moreover, a slight decrement in on current is observed with raise in temperature due to the mobility reduction.

I_{ON}/I_{OFF} and SS variations as a function of temperature are presented in Fig. 12(a). It is observed that there is deterioration in the switching ratio as the temperature increases because of the significant improvement in off current. Furthermore, the value of SS is less at low temperatures and ensures faster operation of the device [51]. Fig. 12(b) depicts DIBL and V_{th} variations with respect to temperature and is observed that as temperature increases, the rise in DIBL is observed because of the decrement in threshold voltage. Furthermore, threshold voltage deteriorated with the rise in temperature due to scattering phenomena [52]. A Threshold voltage roll-off of 9.7% is observed as temperature increased from -43°C to 127°C.

The I_D-V_{DS} characteristics for various temperatures are shown in Fig. 13. The characteristics are obtained at constant N_W and N_T of 10 nm and 5 nm respectively. It can be noticed that as the temperature increases, deterioration in drain current is observed due the reduction in mobility.

Work function is one of the important process parameter which plays a detrimental role in turning on and off of a device. Higher gate work function ensures that the device is fully depleted rapidly and that the device performs better in the off state [53].

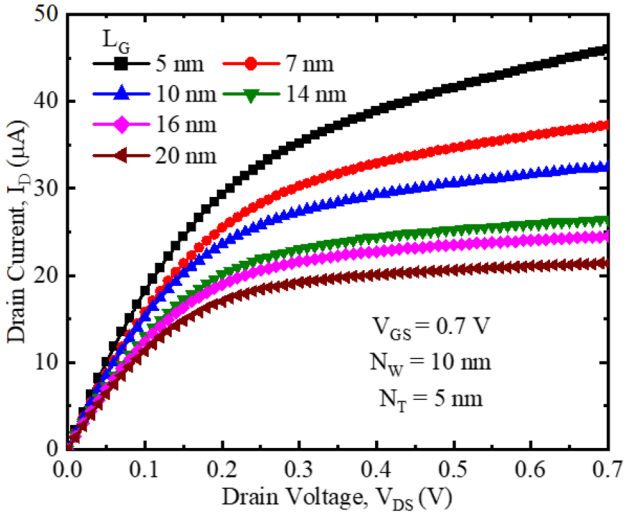
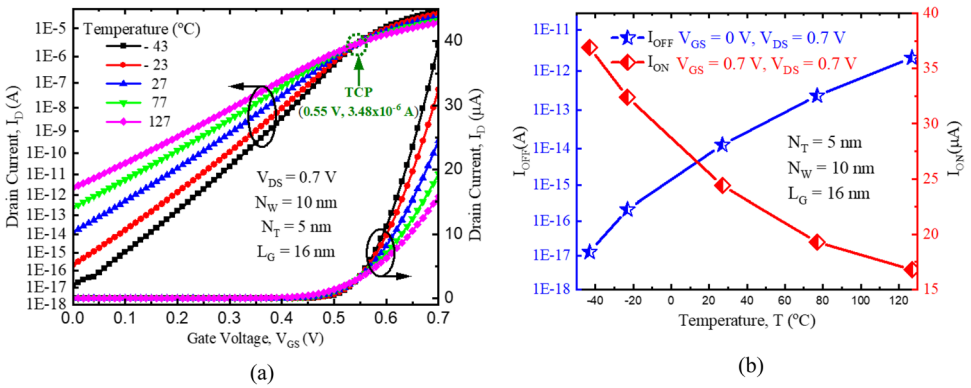


Fig. 10 Output characteristics for various L_G values as a function of drain voltage.



(a) (b)

Fig. 11 (a) Temperature variations (b) I_{ON} and I_{OFF} variations as a function of V_{GS}

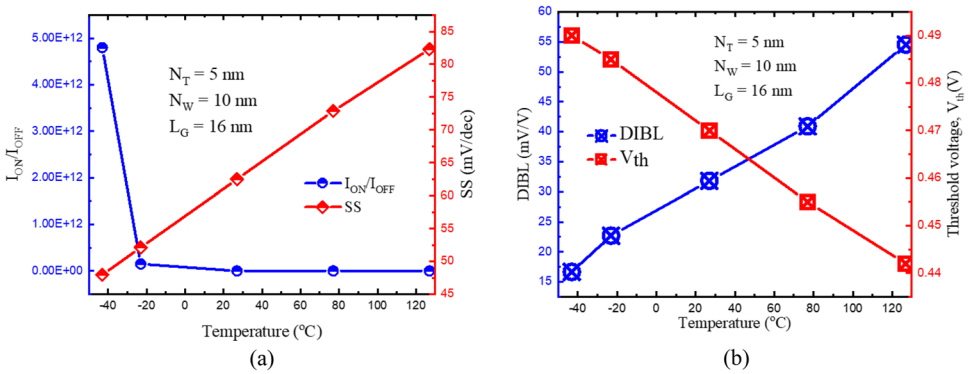


Fig. 12 (a) I_{ON}/I_{OFF} and SS (b) DIBL and V_{th} variations as a function of temperature

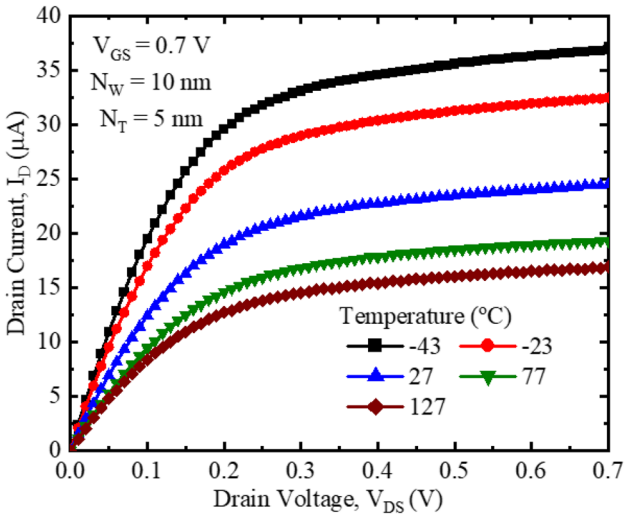


Fig. 13 Output characteristics for various temperature values as a function of drain voltage

Work function impact on drain current as a function of gate voltage is shown in Fig. 14(a). The work function of the device is varied from 4.3 eV to 4.7 eV. From Fig. 14(b) it can be inferred that for higher work function of the device, along with the deterioration in on current, significant reduction in off current is observed. An Increment in work function lowers the tunneling between gate and channel and also between gate and drain/source [54], which helps to reduce the leakage current.

Switching ratio variations with respect to work function are shown in Fig. 15(a). The switching ratio improved significantly with the rise in work function due to a huge reduction in off current. With the increment of work function, the SS gets decremented and ensures good sub threshold performance. Fig. 15(b) depicts the DIBL and threshold voltage variations as a function of the work function. DIBL is decreasing with the rise in work function and lesser DIBL indicates that electrostatic integrity of the gate is more on the device and less sensitive to drain voltage variations. A minimum DIBL of 30.30 mV/V is obtained for work function of 4.7 eV and there is a decrement of 28.6% in DIBL is observed when the work function varied from 4.3 eV to 4.7 eV. However, there is a huge decrement in threshold voltage with the fall in work function of the device. There is a decrement of 3.9x in threshold voltage as the work function is decreased from 4.7 eV to 4.3 eV, and leads to more SCEs. Moreover, the study tells that the devices with more work function will have high threshold voltages and makes the device sluggish.

From Fig. 16 it can be seen that for higher work function values, the slope of I_D -V_{DS} characteristics is less and ensuring lower output conductance value. Furthermore, it

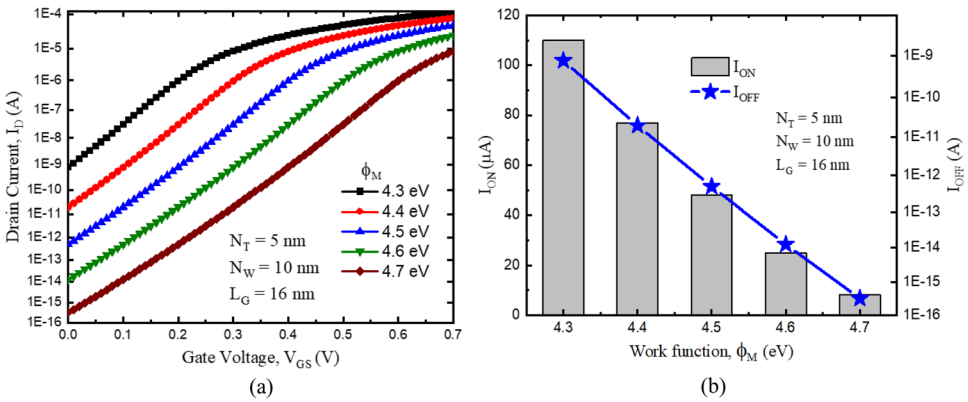
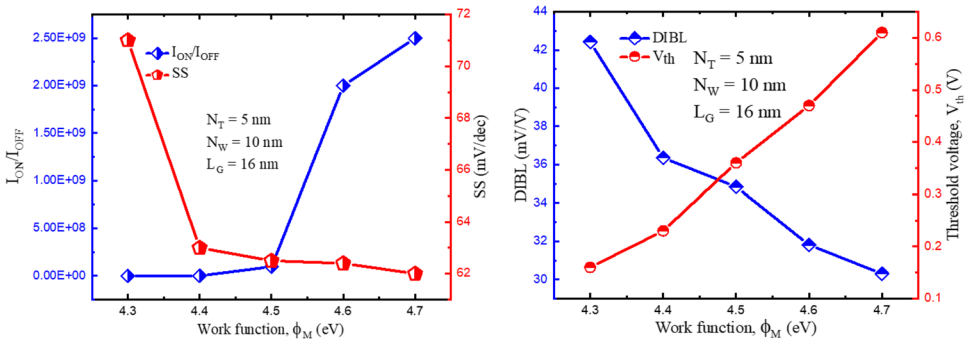


Fig. 14 (a) Drain current variations with work function (b) I_{ON} and I_{OFF} variations as a function of work function



(a) (b)

Fig. 15 (a) I_{ON}/I_{OFF} and SS (b) DIBL and V_{th} variations as a function of work function

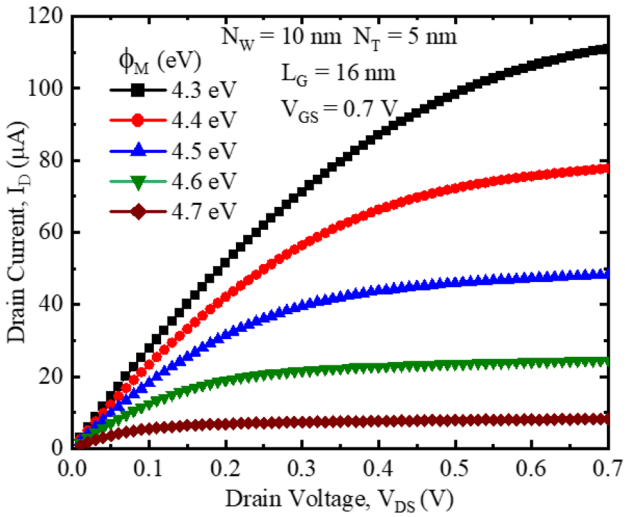


Fig. 16 Output characteristics for various work function values as a function of drain voltage

is noticed that slope for $\Phi_M = 4.7eV$ is less compared to $\Phi_M = 4.3eV$.

4 Conclusion

In this paper, the detailed DC performance of 3D vertically stacked NSFET is analyzed by varying the thickness and width of the nanosheet. It is observed that there is an increment in both on current and off current as the width and thickness values are increased. However, the switching ratio, DIBL, and SS are degraded as the dimensions of NSFET are increasing. Moreover, the performance of NSFET is analysed with scaling of gate length to ensure the device feasibility for lower technology nodes. Also, the temperature analysis is performed for a wide range of temperatures to identify the TCP point, which is more essential for biasing the device in various real time applications. Finally, the impact of work function on device transfer characteristics is analysed. These results will give deep insights into the performance of NSFET with different device parametric variations.

Acknowledgements The authors thank to the department of Electronics and Communications Engineering, NIT Warangal for providing the TCAD Tools.

Availability of data and material Not applicable.

Author Contributions N. Aruna Kumari: Methodology, Writing- Original draft preparation, Formal Analysis, Software, Investigation, Visualization, Data Curation.
P. Prithvi: Supervision.

Declaration

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Conflict of Interest The author has no conflicts of interest to declare that are relevant to the content of this article.

Consent to Participate Not applicable.

Consent for Publication Not applicable.

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