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ORIGINAL PAPER

Optimization of Design Space for Vertically Stacked Junctionless Nanosheet FET for Analog/RF Applications

Sresta Valasa [1] · Shubham Tayal [1] · Laxman Raju Thoutam [1]

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Abstract

This paper investigates the various device dimensions such as gate length (L_g), nanosheet thickness (T_{NS}), and nanosheet width to optimize the design space for vertically stacked Junctionless Nanosheet Field Effect Transistor (JL-NSFET). The optimization has been carried out by considering several analog/RF parameters that include On-current (I_{ON}), Off-current (I_{OFF}), Transconductance Efficiency (g_m/I_d), Subthreshold Swing (SS), Drain Induced Barrier Lowering (DIBL), I_{ON}/I_{OFF} ratio, Transconductance (g_m), gate capacitance (C_{gg}), Output conductance (g_{ds}), and Cutoff-frequency (f_T), Intrinsic gain (A_v) are explored here. It is found that the downscaling of L_g from 16 nm to 8 nm resulted in an increase in SS and DIBL. However, scaling down of T_{NS} (W_{NS}) from 10 nm to 5 nm (from 18 nm to 10 nm) resulted in a decrease in SS by ~30.5% (~16.39%) and in DIBL by ~44.23% (~78.59%) respectively. The short channel effects (SCE) are greatly suppressed by upscaling of L_g and downscaling of T_{NS} and W_{NS}. The transconductance (g_m) is improved by decreasing the L_g and T_{NS} but a significant degradation is found for W_{NS}. Further, the gain (A_v) is improved by an amount of ~22.86% by upscaling the L_g and ~ 7.07%, ~31.75% with the downscaling of T_{NS} and W_{NS} respectively. The gate capacitances (C_{gg}) are reduced with the downscaling of L_g and W_{NS}, however the same is increased for T_{NS}. Moreover, the cutoff frequency (f_T) is improved with scaling down of L_g and T_{NS} in comparison with the W_{NS}.

Keywords Junctionless · Short channel effects · Gate length (L_g) · Thickness (T_{NS}) · Width (W_{NS})

1 Introduction

Over last few decades, the traditional bulk planar MOSFETs have been substantially downscaled, while numerous approaches have been proposed from 90 nm to 32 nm technology nodes to optimize the CMOS performance [1]. Yet, rigorous scaling down of planar Si-MOSFETs culminated in loss of channel controllability, and the resulting short channel effects (SCE) deteriorated the DC/AC performance characteristics considerably [2, 3]. Around 2012, at 22-nm node, FinFETs have been preferred as a solution to circumvent SCEs and also facilitated continual scaling down in device dimensions [4–6]. Further these FinFETS's have been successfully downscaled to the 10 nm node by escalating the aspect ratio and optimizing the layout [7–9]. FinFETs began to supersede planar MOSFETs in many system-on-chip applications in terms of area, efficiency, and power. However, various technical constraints such as quantized device width, high parasitics and capacitances, corner effect should be addressed prior continued scaling in FinFETs [10, 11]. Thinner fins are also a requisite to maintain superior electrostatics, however it reduces carrier mobility and instigates higher variations in threshold voltage [12, 13]. To overcome the limitations associated with the FinFETs, the Gate All Around (GAA) structure has been proposed [14]. Owing to its excellent gate control, GAA nanowire (NW) FETs were presumed as the tenacious competitors potentially to replace FinFETs. However, implementation of GAA NWFETs necessitates a significant transition in fabrication procedures [15].

The GAA nanosheet (NS) FETs are devised as an interim approach amongst the aforementioned architectures. NSFETs

✉ Sresta Valasa
shreshtavalasa@gmail.com

Shubham Tayal
shubhamtayal999@gmail.com

Laxman Raju Thoutam
tlaxmanraju@gmail.com

[1] Department of Electronics and Communication Engineering, SR University, Warangal, India

offer relatively greater performance over FinFETs and NWFETs while utilizing simple fabrication processes [16–21]. NSFETs offer higher electrostatic integrity, optimized power performances, and improved transistor density per chip by increasing effective width of the channel with enough current drivability in the given footprint [22–24]. This additionally ensures exceptional electrostatics with the GAA structure [25]. Also, NSFETs provide faster switching than NWFETs owing to the reduced parasitic capacitance for a given footprint [26]. Furthermore, NSFETs can alter the drain currents by adjusting the NS width, enabling a CMOS-compatible layout design [27, 28]. The width of the NS can be optimized to meet the required current drivability for any device over a single wafer while maintaining a low-cost area [29]. This has a profound benefit over the FinFET, which allows only discrete I_{ON} variation while adjusting the number of fins [30]. Nevertheless, there are certain design constraints involved with the NSFETs. Formation of sharp junctions at such deep technology nodes is notably challenging for nanosheet devices to achieve [31]. To address these fabrication issues, junctionless FETs are required to continue scaling in nanostructures [32].

The doping profile of junctionless transistors is consistent along all the source-channel-drain region. This is typically an on-device that utilizes bulk conduction rather than surface conduction in conventional MOSFETs. Therefore, to turn it off, the channel must be entirely depleted [8, 33]. To deplete the channel, a negative bias must be provided at the gate terminal. However, the same can be generated without using a negative gate bias by establishing a work function between the metal gate and the silicon semiconductor [34, 35].

Moreover, the present NSFETs have wide cross sections, at which the impact of subband separation is minimal. This may not be the case in upcoming years, wherein the nanosheets are anticipated to become highly confined [36–38]. In current NSFET devices, the impact of threshold voltage shifts owing to bandgap variation and centroid shift are clearly evident [14]. These effects show a significant impact on DC and analog/RF performance of the device. Further, the DC and analog/RF performance of the device degrade due to the short channel effects (SCE). The improvement in these DC and analog/RF characteristics of these devices is a requisite and can be achieved by the stacked channels' greater immunity due to enhanced performance, as well as the reduced distance between the NSFETs and the lower effective oxide thickness [39, 40].

Consequently, this paper investigates the DC and analog/RF performance of JL-NSFET. The impact of various parameters of JL-NSFET like gate length (L_g), nanosheet thickness (T_{NS}), and nanosheet width (W_{NS}) has been explored.

2 Device Structure and Simulation Technicalities

Figure 1 illustrates the 3-dimensional schematic of a vertically two stacked JL-NSFET simulated using the Sentaurus TCAD tool [41]. The JL-NSFET is heavily doped with arsenic (n-type) equal to 1×10^{19} cm^{-3}.

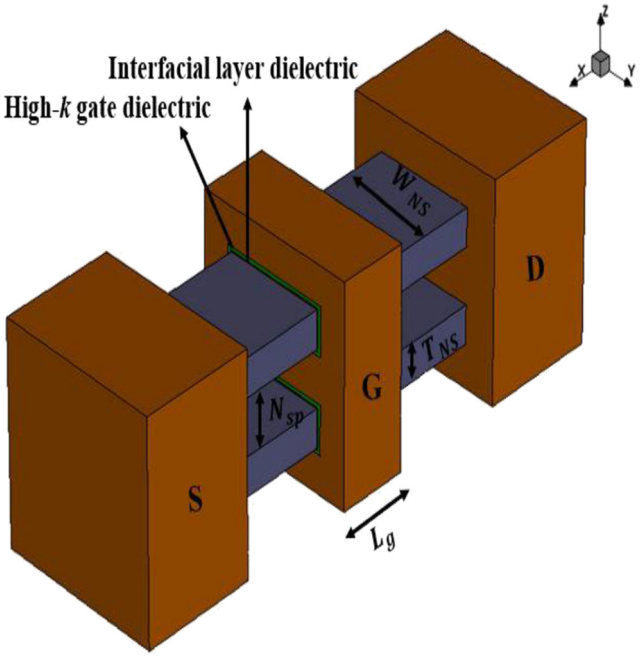

Fig. 1 3D view of JL-NSFET

Table 1 Device specifications of JL-NSFET

Device specifications	Values
Gate length (L_g)	8–16 nm
Silicon thickness (T_{NS})	5–10 nm
Width of the nanosheet (W_{NS})	10–18 nm
Nanosheet spacing (N_{sp})	6 nm
Work function (ϕ_{ms})	4.8 eV
Contact resistivity [18]	7 Ω.μm^2
Sheet silicide resistivity [18]	7.5 Ω/sq.
Gate Oxide Thickness	0.7 nm
Doping concentration	1×10^{19} cm^{-3}
No. of nanosheets	2
Temperature	300 K

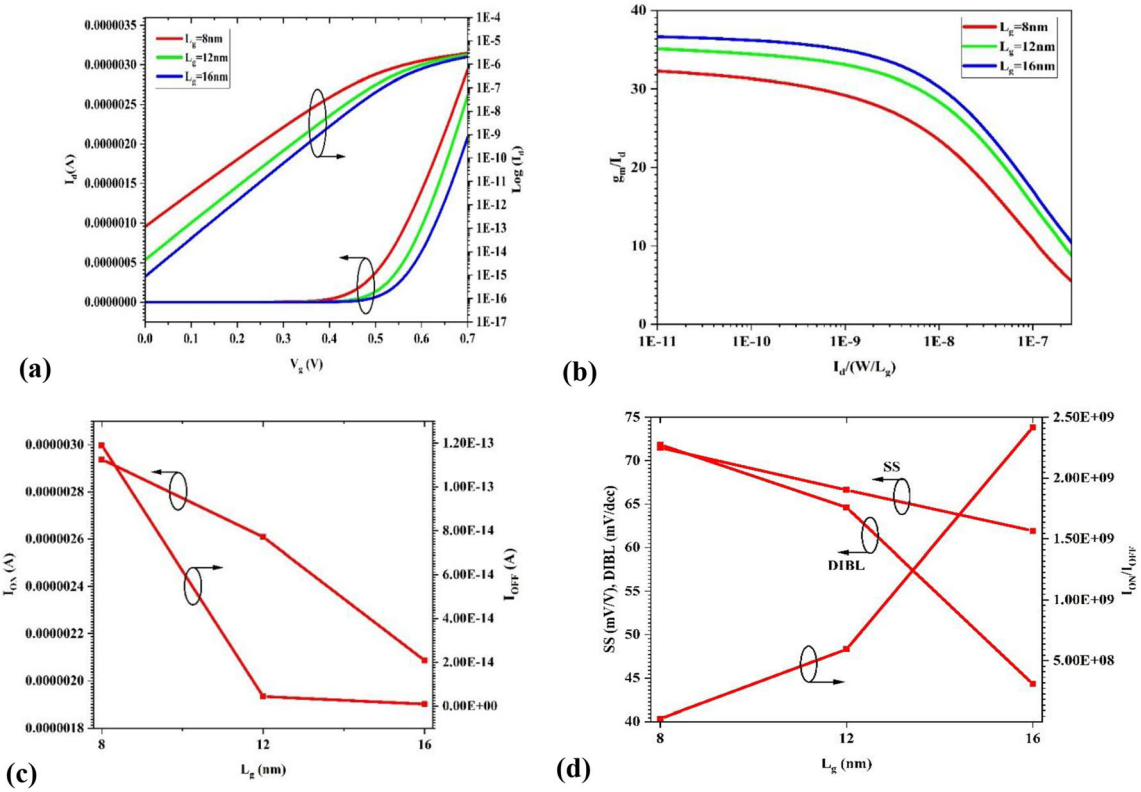

Fig. 2 DC characteristics of the JL-NSFET with respect to L_g variation **a** I_d-V_g transfer curve characteristics **b** g_m/I_d vs $I_d/(W/L_g)$ **c** On-current (I_{ON}) and Off-current (I_{OFF}) **d** SS, DIBL, and I_{ON}/I_{OFF} ratio

A work function (ϕ_{ms}) of 4.8 eV is adapted to eliminate the poly depletion effects. The device gate length (L_g), thickness of the silicon sheet (T_{NS})and width of the nanosheet (W_{NS}) is varied in the order of 8-16 nm, 5-10 nm, 10-18 nm respectively to study the effective device performance.

The device specifications used for analyzing the performance of the designed JL-NSFET are listed below in Table 1.

The gate oxide thickness has been fixed at 0.7 nm to assure that the device produces better electrostatic integrity. The spacing between the nanosheets is set at 6 nm [11]. The contact resistivity (sheet silicide resistivity) of 7 $\Omega.\mu m^2$ (7.5 Ω/sq.) is employed in the estimation of gate parasitics to ensure that there is zero electrostatic degradation [18] and is given by Eq. (1)

$$R_{SD} = \frac{1}{12}\underbrace{\rho}_{\substack{sheet\\silicide}}\frac{2n(T_{NS}+W_{NS})}{L_G} + \frac{\overbrace{\rho}^{\substack{contact\\resistivity}}}{2n(T_{NS}+W_{NS})\,L_G} \quad (1)$$

where n = no. of nanosheets

Several simulation models are included to study the performance of the device. To analyze the heavy doped JL-NSFET characteristics, the Fermi dirac statistics model is employed. To account for the radiative generation, and recombination effects, the SRH generation/recombination band to band tunneling and auger models are used. Surface roughness and acoustic phonons are characterized using the Lombardi mobility models. The Slotboom bandgap narrowing model is used to explore bandgap energy narrowing in relation with the doping levels. Further, the quantum density gradient model is also adapted for considering the quantum confinements.

3 Results and Discussion

3.1 Effect of Gate Length (L_g) Variation

This subsection explores the effect of gate length (L_g) variation on several dc and analog/RF parameters such as I_d-V_g transfer curve characteristics, On-current (I_{ON}), Subthreshold Swing (SS), Off-current (I_{OFF}), Drain Induced Barrier Lowering (DIBL), I_{ON}/I_{OFF} ratio, Transconductance (g_m), Intrinsic gain (A_v), Output conductance (g_{ds}), gate capacitance (C_{gg}), Cutoff- frequency (f_T), and Transconductance efficiency (g_m/I_d). To discover

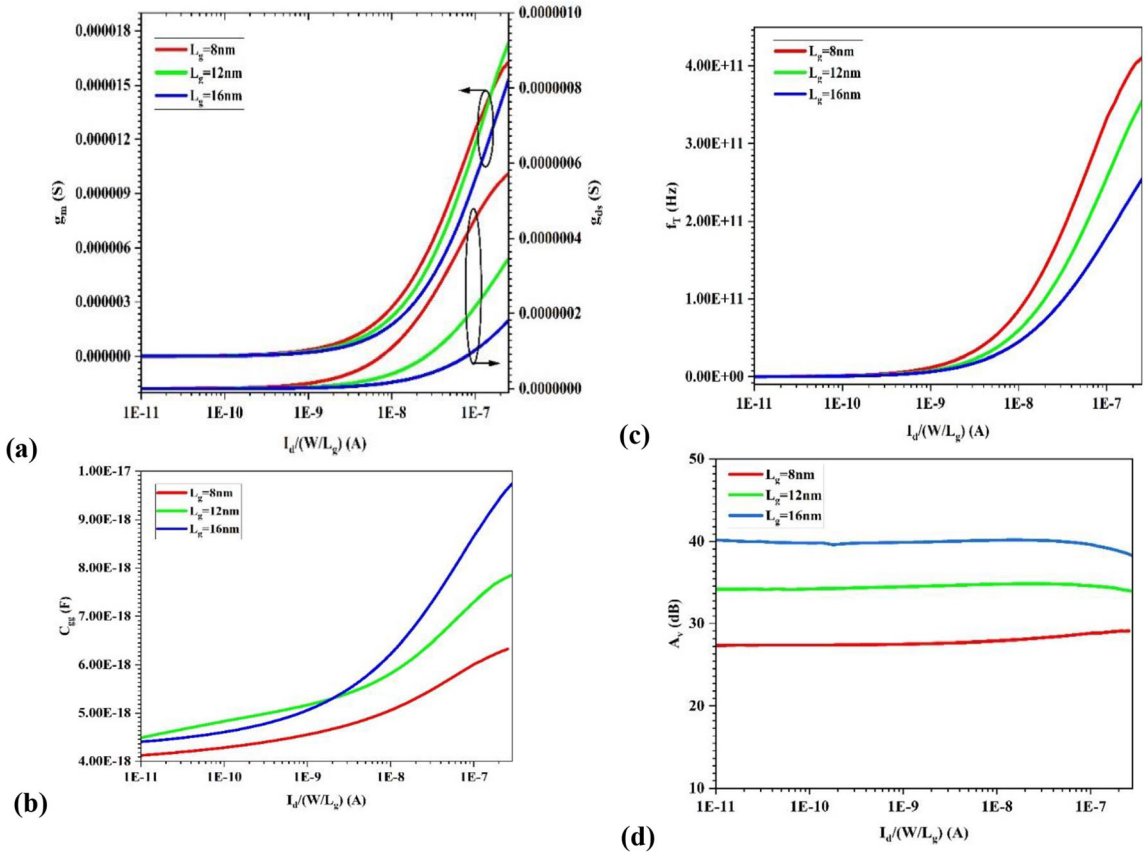

Fig. 3 Variation of analog/RF parameters with respect to $I_d/(W/L_g)$ for various gate lengths (L_g) **a** g_m and g_{ds} **b** C_{gg} **c** f_T (d) A_v

the behavior of the JL-NSFET with respect to L_g variation, the gate lengths L_g = 8 nm, 12 nm, and 16 nm have been used. The thickness (T_{NS}) and width of the nanosheet (W_{NS}) are fixed at 5 nm and 18 nm respectively.

Figure 2 showcases the several DC characteristics of the designed JL-NSFET. The drain current (I_d) with respect to gate voltage (V_g) for various gate lengths (L_g) in both linear as well as logarithmic scale is depicted in Fig. 2a. It is noticed that scaling up of L_g results in the decrease in drain current. The Transconductance efficiency (g_m/I_d) plays a prominent role in the analog/RF circuit design and is described as the possible gain per unit amount of power consumption [42]. Larger g_m/I_d values indicate improved input drivability and reduced power consumption in capacitive load circuits. The g_m/I_d as a function of $I_d/(W/L_g)$ is presented in Fig. 2b and it is observed that g_m/I_d improves with increase in L_g. The on currents (I_{ON}) and off currents (I_{OFF}) as a function of L_g is visualized in Fig. 2c. The results demonstrate that the increase in the L_g results in the decrease in both I_{ON} and I_{OFF}. This decrease in I_{ON} with the upscaling of L_g can be understood with the drain current equation of junctionless transistors [35] which is mathematically given as

$$I_D \cong q\mu N_D \frac{T_{NS} W_{NS}}{L} V_{DD} \tag{2}$$

Consequently, an improvement in I_{ON}/I_{OFF} ratio is experienced as the L_g increases as espied in Fig. 2d. As the increase in I_{OFF} is much more than that in I_{ON} (2.086×10^{-6} to 2.938×10^{-6}) at reduced L_g, the I_{ON}/I_{OFF} ratio of the device reduces at reduced L_g. However, the JL-NSFET exhibits excellent performance for all L_g's with a ratio greater than 10^6 that is best suitable for digital logic design applications. The SS has a substantial influence on the static power dissipations in low standby power areas and thus must be low [43, 44]. It is observed that when the L_g increases from 8 nm to 16 nm, the SS decreases indicating a shift towards the ideal value of 60 mV/dec and thus ensuring the better gate control of the device. The DIBL also reduces with the upscaling in L_g due to the reduction in I_{OFF} [35]. The improvement in SS, and DIBL with the increase in L_g indicates the reduction in short channel effects.

Furthermore, the impact of transconductance (g_m), gate capacitance (C_{gg}), output conductance (g_{ds}), cut-off frequency

(f_T), and intrinsic gain (A_v) for different L_g as a function $I_d/(W/L_g)$ is plotted in Fig. 3. From Fig. 3a, it is seen that both the g_m and g_{ds} increases linearly with an increase in $I_d/(W/L_g)$ for all L_g. It is also noticed that g_m and g_{ds} decrease with the increase in L_g. The reduction in g_{ds} with L_g might be attributed to the lower DIBL effect at higher L_g (Fig. 2d). It is also noticed that C_{gg} (Fig. 3b) increases with the increase in L_g owing to the increase in effective channel area and relative inversion charge density.

Further, from Fig. 3c, it is noticed that the Cut-off frequency $\left(f_T = \frac{g_m}{2\pi C_{gg}}\right)$ gets degraded with the increase in L_g due to the increase in C_{gg} at higher L_g. Additionally, Fig. 3d elucidate that the intrinsic gain $\left(A_v = 20log_{10}\frac{g_m}{g_{ds}}\right)$ increases with scaling up of L_g. This might be due to the lower g_{ds} values resulted with the increase in L_g.

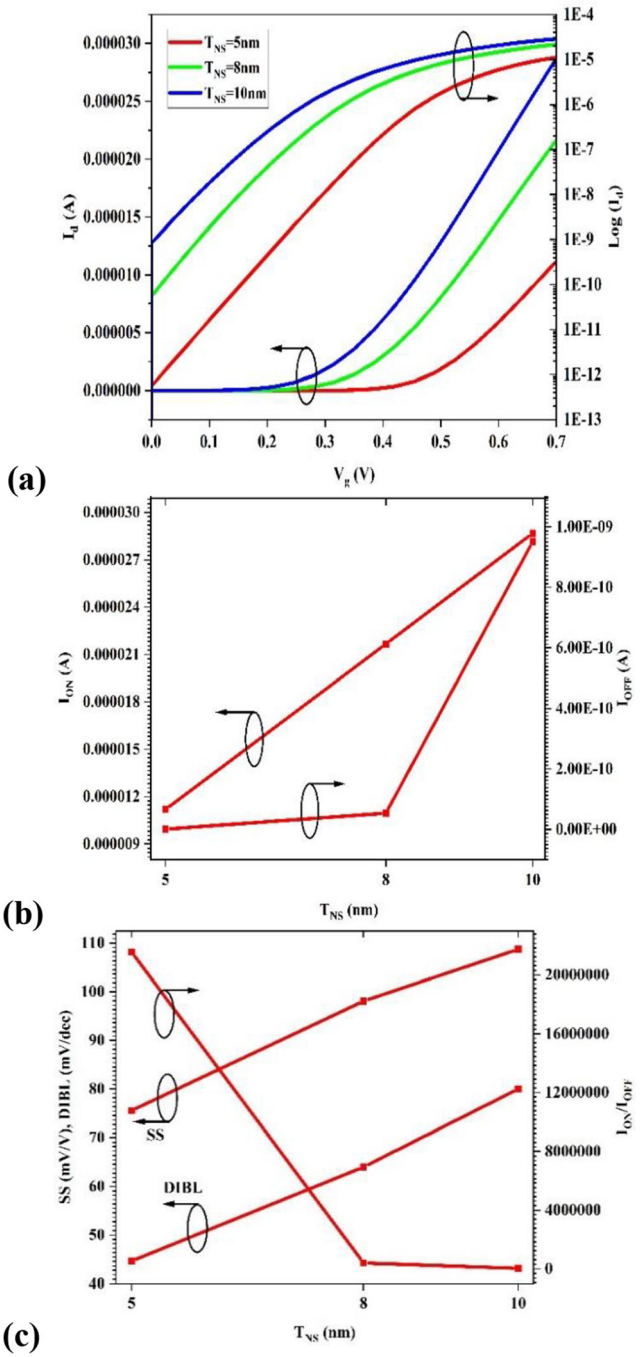

Fig. 4 DC characteristics of the JL-NSFET with respect to T_{NS} variation **a** I_d-V_g transfer curve characteristics **b** On-current (I_{ON}) and Off-current (I_{OFF}) **c** SS, DIBL, and I_{ON}/I_{OFF} ratio

3.2 Effect of Nanosheet Thickness (T_{NS})

The thickness of nanosheet (T_{NS}) is a critical parameter that affects the device performance. The T_{NS} is varied from 5 nm to 10 nm with the L_g and W_{NS} fixed at 10 nm and 18 nm respectively. This subsection explores the impact of nanosheet thickness (T_{NS}) on several dc and analog/RF parameters such as I_d-V_g transfer curve characteristics, I_{ON}, I_{OFF}, SS, DIBL, I_{ON}/I_{OFF} ratio, g_m, g_{ds}, C_{gg}, f_T, A_v.

Figure 4a illustrates the I_d-V_g characteristics curve for various T_{NS} of the nanosheet. It is realized that the drain current (I_d) decreases through the downscaling of T_{NS}. From Fig. 4b it is observed that the I_{ON} reduces with the downscaling of T_{NS} from 10 nm to 5 nm. The reason behind the decrease in I_{ON} with T_{NS} can be given by Eq. (2) $\left(I_d \propto T_{NS}\frac{W_{NS}}{L}\right)$ and may be attributed to the rise in the electric field (which results in the field dependent degradation due to the scattering phenomenon), and the rise in quantum confinement (that causes the boost in effective mass thereby reducing the density of states and hence resulting in mobility degradation) [16, 34, 45].

The decrease in I_{OFF} is due to the increase in quantum confinement effects with the downscaling of T_{NS}. This can be accounted to increase in bandgap and potential barrier height due to increase in subband energies and spacing between the subbands [34]. Consequently, an increase in I_{ON}/I_{OFF} ratio is noticed as T_{NS} is down scaled from 10 nm to 5 nm as shown in Fig. 4c. I_{ON}/I_{OFF} increases as the decrease in I_{OFF} (9.518×10^{-10} to 5.1818×10^{-13}) supersede the decrement in I_{ON} (2.86852×10^{-5} to 1.11779×10^{-5}) when T_{NS} is scaled down from 10 nm to 5 nm. It is also noticed that there is an improvement in both SS and DIBL with the downscaling T_{NS}.

Furthermore, the analog/RF performance as a function of $I_d/(W/L_g)$ for different T_{NS} is explored here. An interesting behavior for g_m, g_{ds}, C_{gg}, and A_v are observed with the downscaling of T_{NS}. From Fig. 5a, it can be noticed that as the T_{NS} is scaled down, g_m and g_{ds} increase for 5 nm. However, the 10 nm thickness reported an increase in g_m and g_{ds} compared to the 8 nm thickness. This might be due to the effect of the

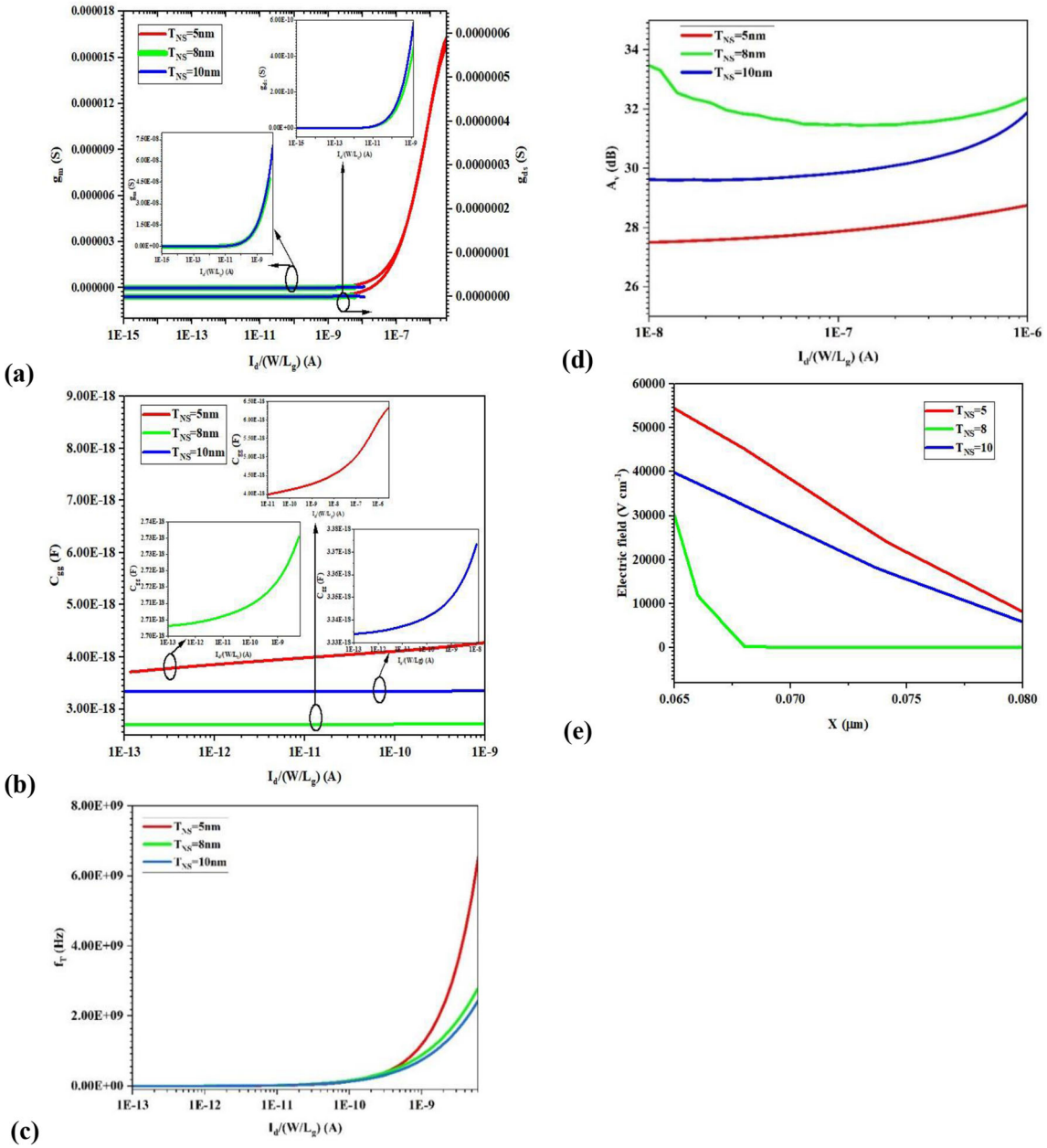

Fig. 5 Variation of analog/RF parameters with respect to $I_d/(W/L_g)$ for different nanosheet thickness (T_{NS}) **a** g_m and g_{ds} **b** C_{gg} **c** f_T **d** A_v **e** electric field along the lateral direction (X)

increase in electric field for 10 nm thickness compared to 8 nm thickness (Fig. 5e).

Subsequently, a similar trend is observed for C_{gg} too as depicted in Fig. 5b. Higher value of C_{gg} is noted for 5 nm thickness, whereas a greater increase in C_{gg} for 10 nm thickness is visualized compared to the 8 nm thickness. The higher f_T values are noted with the scaling down of T_{NS} as illustrated in Fig. 5c. This might be due to higher g_m values at lower T_{NS}. It is also espied from Fig. 5d that the intrinsic gain (A_v) is maximum at T_{NS} = 5 nm. This may be attributed to relative high increase in g_m in comparison with the degradation in g_{ds} for T_{NS} = 8 nm compared to T_{NS} = 5 nm and 10 nm. This might be attributed to the lower g_m values with the downscaling of T_{NS}. Thus, from the above analysis it can be said that for analog performance T_{NS} = 8 nm should be preferred, however for RF performance T_{NS} = 5 nm should be preferred.

3.3 Effect of Nanosheet Width (W_{NS})

In this subsection, the impact of nanosheet width (W_{NS}) on the performance of JL-NSFET is investigated. The W_{NS} is varied from from 10 nm to 18 nm. The T_{NS} and L_g are kept constant at 5 nm and 8 nm respectively for the analysis purpose. Various dc and analog/RF parameters such as I_d-V_g transfer

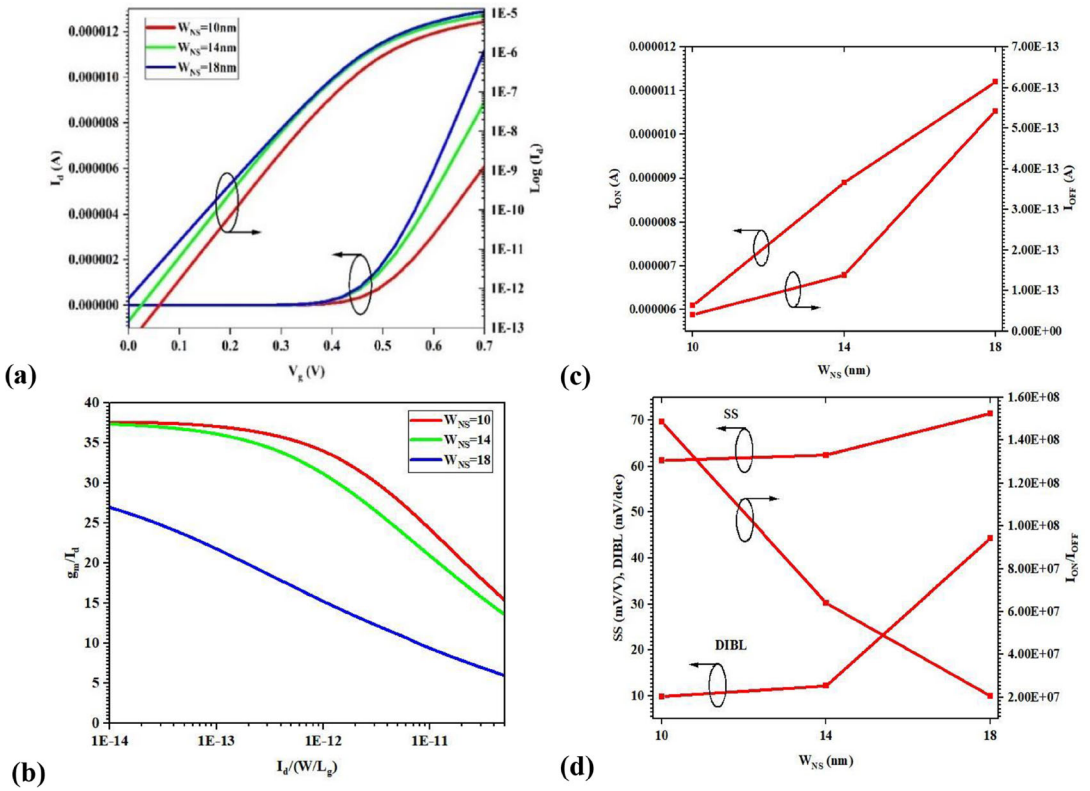

Fig. 6 DC characteristics of the JL-NSFET with respect to W_{NS} variation **a** I_d-V_g transfer curve characteristics **b** g_m/I_d vs $I_d/(W/L_g)$ **c** On-current (I_{ON}) and Off-current (I_{OFF}) **d** SS, DIBL, and I_{ON}/I_{OFF} ratio

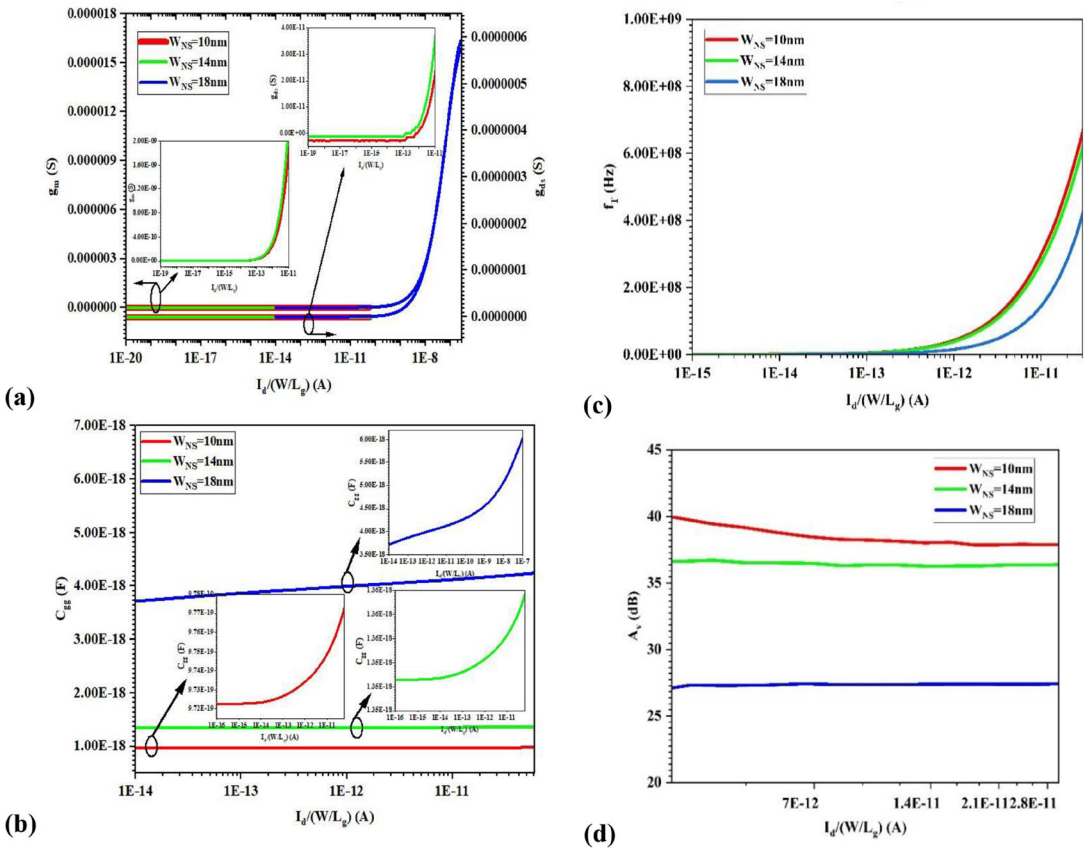

Fig. 7 Variation of analog/RF parameters with respect to $I_d/(W/L_g)$ for different nanosheet width (W_{NS}) **a** g_m and g_{ds} **b** C_{gg} **c** f_T (d) A_v

curve characteristics, g_m/I_d, I_{ON}, I_{OFF}, SS, DIBL, I_{ON}/I_{OFF} ratio, g_m, C_{gg}, g_{ds}, f_T, and A_v are explored here to optimize the design space for JL-NSFET.

The I_d-V_g transfer characteristics curve in linear scale for two stacked JL-NSFET is presented in Fig. 6a. The g_m/I_d improves with the downscaling of W_{NS} as shown in Fig. 6b. From Fig. 6c it is noticed that as the W_{NS} is down scaled from 18 nm to 10 nm the driving capability of I_{ON} is reduced and the I_{OFF} reduces significantly. The reduction in I_{OFF} (5.431×10^{-13} to 4.093×10^{-14}) contribute to the net increase in I_{ON}/I_{OFF} ratio as portrayed in Fig. 6d. The SS and DIBL are improved greatly with the downscaling of W_{NS}.

Further, the analog/RF performances as a function of $I_d/(W/L_g)$ are also examined in this subsection. From Fig. 7a, it is picturized that as the W_{NS} is scaled down from 18 nm to 10 nm, the reduction in g_m is experienced because of the decrease in the drain current (I_d). The g_{ds} also reduces effectively with the scaling down of W_{NS} ensuring a good electrical performance in terms of the intrinsic dc gain (A_v) (Fig. 7d) of the JL-NSFET. Moreover, the C_{gg} also reduces as the W_{NS} is downscaled as depicted in Fig. 7b that in turn improves the f_T (Fig. 7c) with the downscaling of W_{NS}. This might be due to the reduction in C_{gg} with the downscaling of W_{NS} from 18 nm to 10 nm. Consequently, a lower W_{NS} (=10 nm) should be preferred for improved analog/RF performance of JL-NSFET during designing.

3.4 Effect of Nanosheet Spacing (N_{sp})

This subsection discusses the effect of spacing between the nanosheets. The effect of Nanosheet Spacing (N_{sp}) on drain current (I_d) is depicted in Fig. 8. It is found that the N_{sp} negligibly effect the transfer characteristics of JL-NSFET. This in turn will give negligible change in electrical parameters such as I_{on}, I_{off} and threshold voltages (V_{th}). The same has been already observed for conventional nanosheet FET also [11].

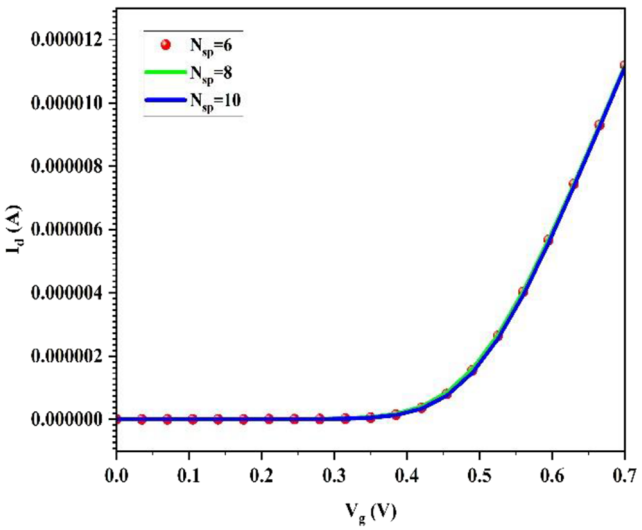

Fig. 8 Effect of spacing (N_{sp}) between the NS on the I_d of JL-NSFET

4 Conclusion

In this article, the study of several DC and analog/RF parameters are carried out for optimizing the design space in terms of gate length (L_g), thickness (T_{NS})and width (W_{NS}) for the JL-NSFET. The analysis revealed that the scaling down of L_g results in an increase the SS, DIBL, and output conductance (g_{ds}) and decrease the I_{ON}/I_{OFF} ratio, gain (A_v), transconductance efficiency (g_m/I_d) affecting the device performance. However, the transconductance (g_m) and cutoff frequency (f_T) are improved significantly. The scaling down of nanosheet thickness (T_{NS}) reported the suppression in SS, DIBL and increase in g_m, f_T, and I_{ON}/I_{OFF} ratio but resulted in a decrease in I_{ON}, A_v, g_m/I_d, increase in g_{ds}, C_{gg} at 5 nm thickness showing a significant influence on the performance for 5 nm thickness. The effect of the increase in electric field for the 10 nm thickness made to improve g_m at a higher rate in comparison with that of 8 nm thickness. Moreover, the downscaling of nanosheet width (W_{NS}) provided a decrease in SS, DIBL, f_T, and C_{gg} greatly compared to the T_{NS}, and improved g_m/I_d, g_{ds}, A_v, I_{ON}/I_{OFF} ratio. Thus, the JL-NSFET is the best device for analog applications if designed at L_g = 16 nm, T_{NS} = 8 nm, and W_{NS} = 10 nm and for RF applications at L_g = 8 nm, T_{NS} = 5 nm, and W_{NS} = 10 nm.

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Code Availability Not applicable.

Author Contributions All the works (Conceptualization, Methodology, Writing Original Draft, Software, Validation and Investigation, Formal analysis, Resources, Data Curation, Writing Review and Editing) in this paper have done together by Sresta Valasa, Shubham Tayal, Laxman Raju Thoutam.

Data Availability Not applicable.

Declarations

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The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Consent to Participate Not applicable.

Consent for Publication Not applicable as the manuscript does not contain any data from individual. Conflicts of Interest/Competing Interests The authors declare that there is no conflict of interest reported in this paper.

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