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ORIGINAL PAPER

Design and Temperature Assessment of Junctionless Nanosheet FET for Nanoscale Applications

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Abstract

Nanosheets are the revolutionary change to overcome the limitations of FinFET. In this paper, the temperature dependence of 10 nm junctionless (JL) nanosheet FET performance on DC and analog/RF characteristics are investigated for the first time using extended source/drain and with high-*k* gate stack. The detailed DC performance analysis like transfer characteristics (I_D-V_{GS}), output characteristics (I_D-V_{DS}), drain induced barrier lowering (DIBL), subthreshold swing (SS) and I_{ON}/I_{OFF} ratio are evaluated from 200 K to 350 K. We also analyzed the temperature effect on the ON-OFF performance metric (Q), dynamic power, and power consumption. Furthermore, to understand the device performance on various process parameters like doping and work function variations are presented at 300 K. The proposed device exhibits good I_{ON}/I_{OFF} switching behavior with I_{OFF} reaching less than nA for all temperatures. The cutoff frequency (f_T) is determined to be in the THz range the Q ranges between 1.5 to 2.2 μS-dec/mV for temperatures between 200 K to 350 K at L_G of 10 nm. Moreover, the scaling effect of nanosheet at various gate lengths (L_G = 5 to 20 nm) are also presented. From simulation analysis we notice that analog/RF performance parameters of a JL nanosheet FET are less sensitive to temperature variations. At extremely scaled L_G the JL nanosheet FET exhibits lesser power consumption, power and decreases with increase in temperature. Thus, the proposed JL nanosheet FET demonstrates as a strong potential contender for low power and high frequency applications at nano-regime.

Keywords Nanosheet FET · Temperature · Analog/RF · Scaling effects · High-K metal gate · Process variation

1 Introduction

Nanoscale devices are extremely temperature sensitive and has a significant impact on their performance. Due to a wide range of applications in electronic fields like military, automobile, nuclear sector, satellite communication, space, infrared detectors, and terrestrial systems which are highly temperature dependent [1–3]. In most of the aforementioned applications, the basic building blocks are logic gates, static RAM cells and operational amplifiers. Miniaturization is the primary driving force for CMOS transistors to reach more density and high performance for IC applications. But on the other side, deep scaling invites adverse short channel effects (SCEs) and severe second order effects which are diminishing the technological outreach. In order to tackle these SCEs multi-gate transistors are viable option for future technological nodes.

One such device is FinFET in which SCEs have been reduced by wrapping the channel from three sides (Tri-gate structure). But in the contrary, the FinFETs are facing several challenges in terms of device performance, layout, patterning, and effective cost to continue scaling [4–6]. Since all dimensional parameters are decreasing such as height, width, thickness fin structures are required for optimum performance and process. However, for sub-10 nm technology nodes more robust structure that can control the channel from all directions is highly essential in order to control the channel to avoid SCEs. The gate-all-around (GAA) structures like nanowire, and nanosheets are the suitable candidates that can replace FinFET at sub-10 nm regime. But the limiting factors of GAA nanowire transistor is lower drive current (I_D) due to lower effective channel widths [7].

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To continue scaling and to have high performance devices, nanosheet transistors are suggested. Since nanosheet FET is not limited by fin pitch, fin quantization, and have optimum effective width. The nanosheet also offers a larger channel area by vertically stacking the channels in the same metal gate area. The stacked nanosheets get 30% more effective width compared to FinFETs within the same footprint [8, 9]. For nano-scale devices it is very difficult to manufacture sharp

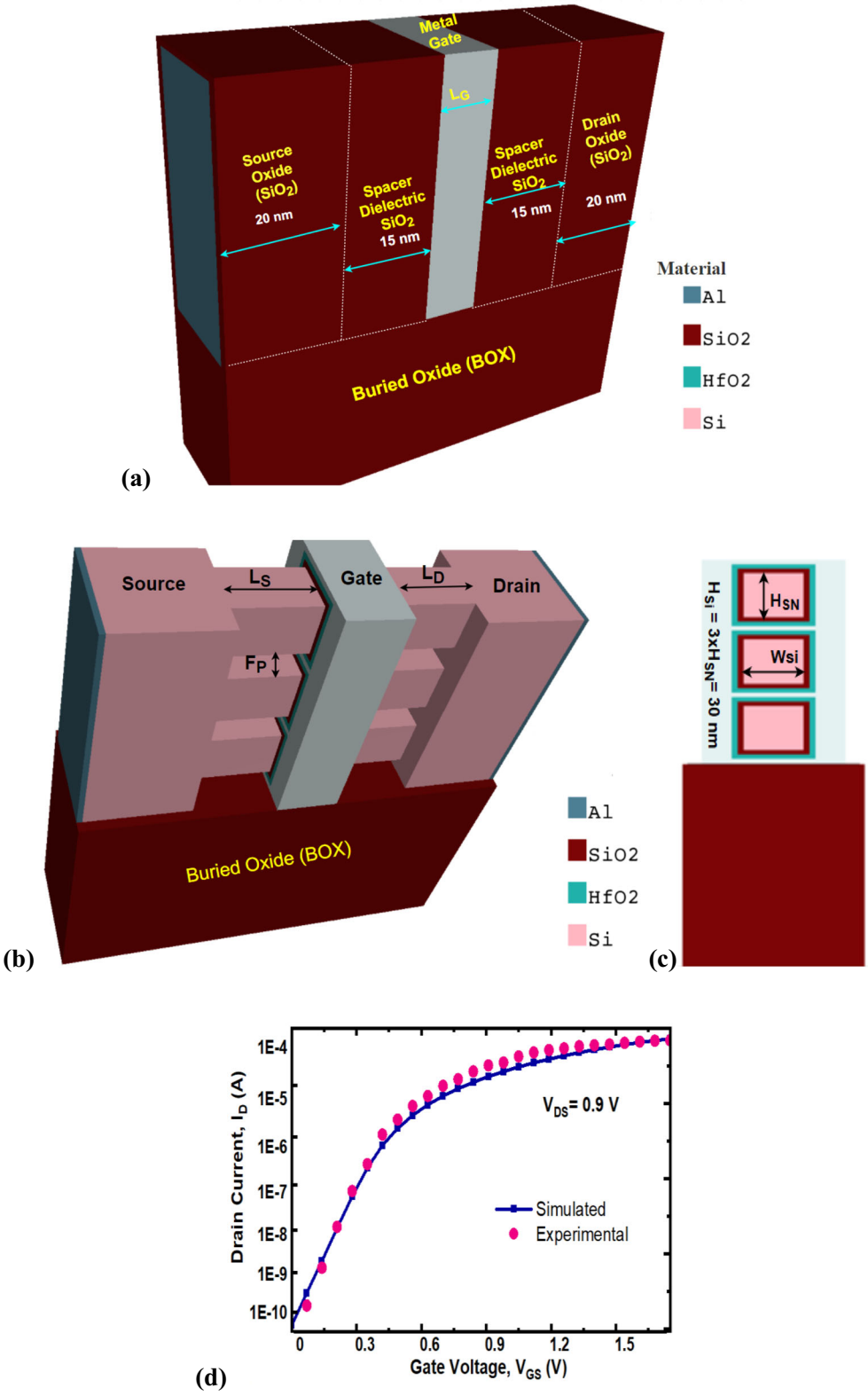


Fig. 1 (a) The schematic view of JL nanosheet FET with isolation oxide and spacer dielectric (b) 3D View of JL nanosheet FET without spacer dielectric and outer isolation oxide (c) 2D cross sectional view of JL nanosheet FET (d) Calibration with experimental data [8]

Table 1 Device parameter description

Parameter	JL Nanosheet FET
Gate Length (L_G)=Fin width (W_{Si})=Channel height (H_{SN}).	10 nm
Gate oxide thickness (t_{OX}) - SiO_2	0.5 nm
Gate high-*k* dielectric oxide thickness – HfO_2	1.28 nm
EOT (Equivalent Oxide Thickness)	0.75 nm
Spacer dielectric	SiO_2
Source/drain Length (L)	20 nm
Length of source/drain (L_S /L_D) spacer	15 nm
Source/channel/drain doping	1×10^{19} cm^{-3}
Vertical Fin Pitch (F_P)	6 nm
Gate work function	4.8 eV

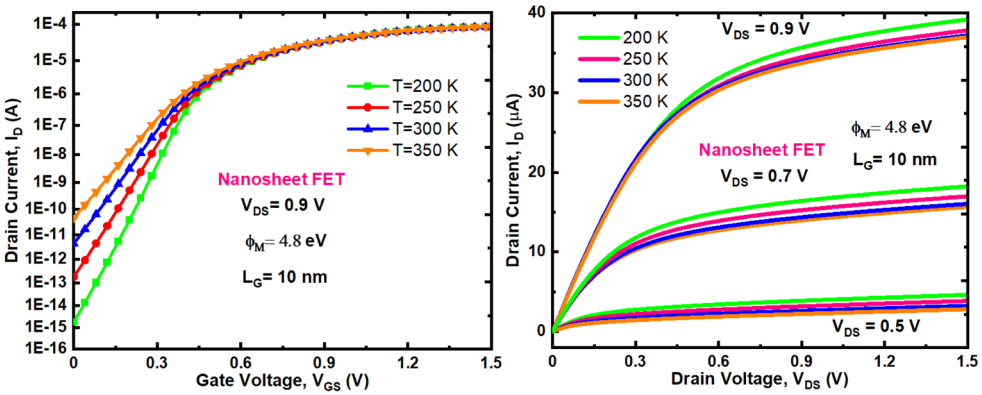
junctions and have fabrication difficulties. To counter these manufacturing obstacles, Junctionless nanosheet FETs are prerequisite to continue scaling at nano-regime. The JL structures are formed through uniform doping throughout the silicon fin [10, 11]. This uniform doping behaves like a resistor whose resistivity can be controlled by gate bias. Moreover, to hold industry expectations and to have benefits of reduced geometry of Si below 45 nm technology fully depleted Silicon-on-insulator (SOI) is a method that accomplishes all goals while simplifying the manufacturing process. Moreover, unlike other technologies, SOI does not alter the fundamental geometry of the transistor. In this work, we have adopted SOI JL nanosheet FET because of lower parasitic capacitances, higher switching speed, and less power consumption [12]. To enhance the performance of 3D nanosheet FET, high-*k* gate stack is used by reducing the oxide thickness. Although the oxide thickness is less, the high-*k* gate dielectric enhances the electrostatic integrity and controllability [13, 14].

In this paper the simulation of JL nanosheet FET is carried out by high-*k* gate stack to have good electrostatic gate control and the whole device is isolated with SiO_2. Section 2 presents the device dimension details and physical models used for simulation. The result analysis of section 3 presents the DC simulation characteristics of 10 nm JL nanosheet FET. Section 4 presents the analog/RF performance and power characteristics of JL nanosheet FET with temperature variation. The section 5 presents the impact of gate length (L_G) variation and process parameter on device performance at 300 K.

2 Device Structure and Simulation Setup

The device structure is generated through Genius 3D device simulator by Cogenda [15]. The 3D and 2D view of JL nanosheet FET are depicted in Fig. 1(a–c). The JL nanosheet FET with gate length (L_G) = 10 nm, each fin width (F_W) = 10 nm, and channel height (H_{SN}) = 10 nm (with total fin height (H_{Si}: 3 × 10 nm = 30 nm) is generated. The device with a uniform doping concentration of 1×10^{19} cm^{-3} is maintained to avoid junction formation at nanoscale dimensions.

The gate stack with SiO_2 of 0.5 nm and HfO_2 of 1.28 nm to get equivalent oxide thickness (EOT) of 0.75 nm is considered to have good electrostatic integrity [16] and the metal gate work function of 4.8 eV is fixed for all the device simulations. An optimized spacer distance of 15 nm is maintained between



(a) (b)

Fig. 2 (a) Transfer (I_D-V_{GS}) (b) Output (I_D-V_{DS}) characteristics of JL nanosheet FET with variation of temperature

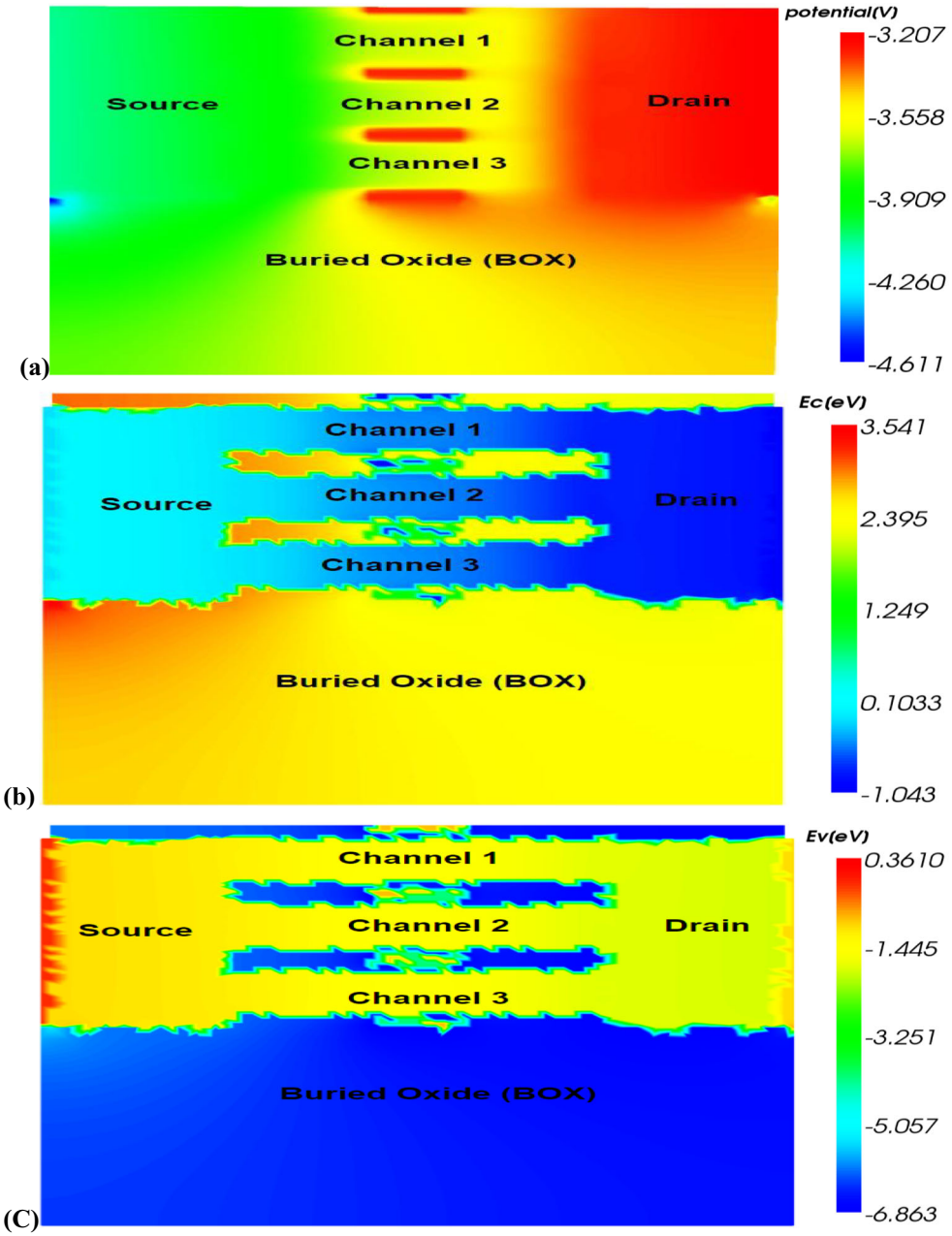


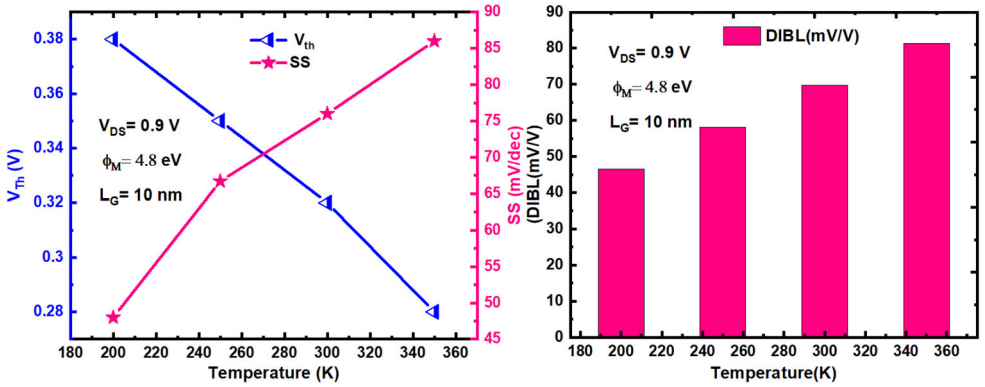
Fig. 3 (a) Potential distribution (b) Conduction band energy (C) Valence band energy of JL nanosheet FET at 300 K with $V_{DS} = 0.9$ V and $V_{GS} = 1.5$ V (ON state)

source/drain and gate terminals to have good subthreshold behavior. Initially uniform doping concentration of 1×10^{19} cm^{-3}, and L_G are set to10 nm respectively for temperature variations.

The physical models used in the simulation are Fermi Dirac statistics to account for heavily doped JL nanosheet FET. To account for generation and recombination phenomena SRH recombination model is activated. For various scattering

Table 2 Electrical characteristics of JL nanosheet FET for various temperatures

Temperature (K)	DIBL (mV/V)	*SS* (mV/dec)	I_{ON} (A)	I_{OFF}(A)	I_{ON}/I_{OFF} Ratio
200	46.5	48	8.65×10^{-5}	1.78×10^{-15}	4.85×10^{10}
250	58.13	66.7	8.51×10^{-5}	1.81×10^{-13}	4.70×10^{8}
300	69.76	76	8.54×10^{-5}	4.38×10^{-12}	1.94×10^{7}
350	81.39	86	8.64×10^{-5}	4.6×10^{-11}	1.87×10^{6}



(a) (b)

Fig. 4 The JL nanosheet FET subthreshold characteristics (a) Threshold voltage (V_{th}) and subthreshold swing (SS) (b) Drain induced barrier lowering (DIBL) with variation of temperature

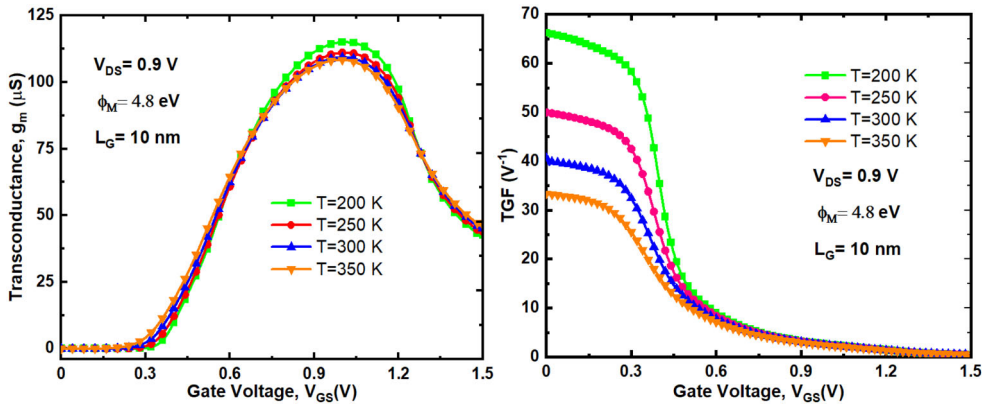
phenomena like surface roughness and acoustic phonons, Lombardi mobility model is incorporated. The bandgap narrowing model is involved due to the higher doping of JL nanosheet FET. The quantum density gradient model for quantum correction effect is also included. The geometrical parameters and materials used for device simulation are depicted in Table 1. The TCAD device physics is well calibrated with experimental results used for demonstration of nanosheet FET and is depicted in Fig. 1(d). The V_{th} is extracted at 100 nA × (W_{eff}/L_G), where W_{eff} is the effective device width [$W_{eff} = n \times (2 \times H_{SN} + W_{Si})$], where 'n' is the number of sheets.

3 Simulation Results and Discussion with Temperature Variations

The device transfer characteristics in log scale with various temperatures are shown in Fig. 2(a) With an increase in temperature the OFF-state leakage current (I_{OFF}) increases with marginal variation in I_{ON}. This increase in I_{OFF} is due to diffusion current and SRH recombination's which are temperature dependent factors. The intrinsic carrier concentration (n_i) is a dependent factor of temperature and mathematically expressed as [17].

$$n_i = exp\left(-E_g/2kT\right) \tag{1}$$

Where 'k' is the Boltzmann constant and 'T' is the absolute temperature. It can be noticed from Fig. 2(a) that at $V_{GS} = 0.6$ V the temperature variation is almost negligible i.e., the temperature coefficient (TC) is zero. The leakage current increases with a rise in temperature due to reduction in V_{th}. However, because of the highly doped channel region in JL system, ionized impurity scattering controls mobility in addition to lattice scattering. Mobility which is limited by ionized impurity scattering, is well known to vary as $T^{3/2}$. As a result, both effects partially counterbalance each other to a larger extent. Hence, the resultant mobility of carriers in the JL device becomes almost constant, irrespective of temperature [17]. It illustrates the monotonic increase in I_D with V_{GS}, almost independent of temperature for the JL device.



(a) (b)

Fig. 5 The analog characteristics of JL nanosheet FET (a) Transconductance (g_m) (b) Transconductance generation Factor (TGF) with variation of temperature

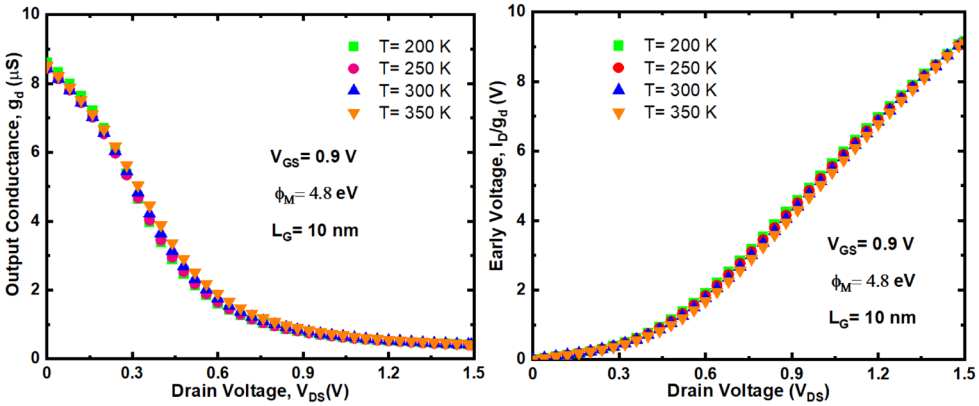


Fig. 6 The output characteristics of JL nanosheet FET (a) Output conductance (g_d) (b) Early voltage (V_{EA}) with variation of temperature

The I_D-V_{DS} characteristics are depicted in Fig. 2(b) and is noticed that lower temperature increases I_D. An increase in temperature leads to the breakage of silicon lattice bonds generating electron and hole pairs. This generation mechanism leads to a raise in carrier concentration. However, this phenomenon is minimal at a lower temperature. If the temperature raises beyond room temperature the diffused drain current increases and hence degrades mobility reducing the drift current even further. Figure 3(a) shows the potential distribution of JL nanosheet FET in ON state (V_{GS} = 1.5 V, V_{DS} = 0.9 V). The potential distribution is more towards the drain and is minimal towards the channel and source side, due to optimized usage of spacer and thus reduces SCEs. Figure 3(b) and (c) shows the conduction and valence band energy contour distributions. Both of them have high energy at source and energy falls in the channel and drain sides due to band bending phenomena occurred by high V_{DS}.

The V_{th} is a significant criterion for indicating a device's ability to switch ON and is desirable to accomplish this transition from OFF to ON at V_{GS} as low as possible. From Fig. 4(a) increase in temperature, V_{th} decreases and hence subthreshold swing (SS) increases. Moreover, at lower temperatures, the decrease of SS assures faster device to turn ON and lower OFF-state current and thus suitable for the design of superior switches and low power applications [18]. From Fig. 4(b) it is noticed that the drain induced barrier lowering (DIBL) effect is more at 350 K and eventually decreases when the device temperature reaches 200 K. As shown in Table 2, the I_{OFF} decreases with a decrease in temperature, and the I_{ON} will be in constant comparatively due to flat band voltage i.e., zero vertical electric field [19]. The I_{ON}/I_{OFF} ratio is higher for 200 K and is least for 350 K. The variation in I_{ON}/I_{OFF} ratio is due to change in I_{OFF} only.

The DIBL and subthreshold swing (SS) evaluates the device efficiency towards subthreshold performance. The DIBL and SS are given by the following expressions [20].

$$\text{DIBL (mV/V)} = \left|\frac{(V_{th1}-V_{th2})}{(V_{DS1}-V_{DS2})}\right| \tag{2}$$

$$\text{SS (mV/dec)} = \left[\frac{\partial \log_{10}(I_D)}{\partial V_{GS}}\right]^{-1} \tag{3}$$

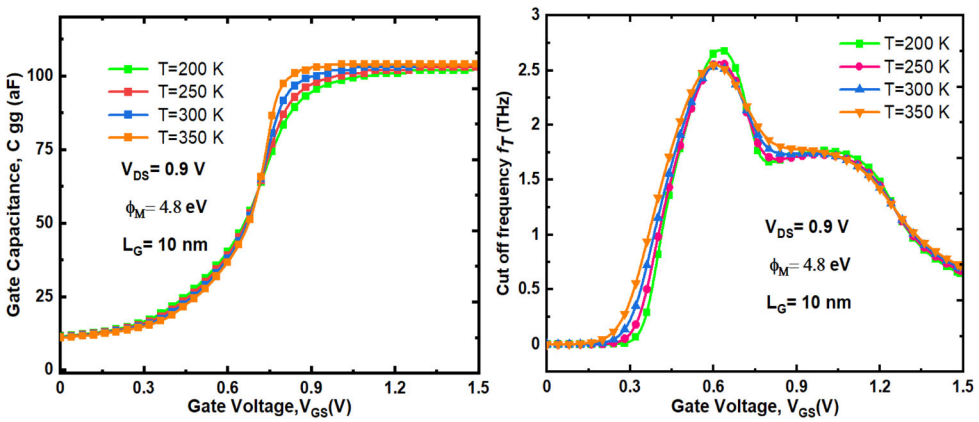


Fig. 7 The JL nanosheet FET characteristics (a) Gate capacitance (C_{gg}) (b) Cutoff frequency (f_T) with variation of temperature

Table 3 Analog and RF characteristics of JL nanosheet FET

Temperature (K)	TGF (V^{-1})	g_m (μS)	g_d (μS)	V_{EA} (V)	C_{gg} (aF)	f_T (THz)
200	66.25	115.08	8.6	9.14	96.5	2.68
250	49.98	111.13	8.43	9.15	98.4	2.54
300	40.70	109.39	8.4	9.11	99.5	2.53
350	33.24	108.44	8.4	9.11	102	2.51

where V_{th1} is taken at V_{DS1} of 0.04 V and V_{th2} is taken at V_{DS2} of 0.9 V.

4 Analog and RF Performance Metrics

The density of transistors and performance in terms of speed improve as the feature size of an integrated circuit decreases, leading to an idea of system-on-chip (SOC), where analog/RF communication circuits are integrated with digital logic and memory circuits. Hence it is fundamental to investigate the device performance for analog/RF circuit applications. Moreover, to utilize any device for high frequency applications, the parasitic capacitance associated with the device must be as low as possible, since parasitic capacitance establishes a path between the input and output nodes, causing signal distortion and circuit oscillations. Furthermore, the parasitic capacitances play a detrimental role in deciding analog/RF behavior and they have an inverse relation with the speed of operation and power dissipation.

The g_m is an important parameter for building operational and transconductance amplifiers. The g_m also specifies bandwidth, DC gain of an amplifier, and noise performance. To evaluate g_m the mathematical expression can be given as $g_m = \partial I_D / \partial V_{GS}$ [21] at constant V_{DS}. Figure 5(a) depicts the temperature variation of g_m with respect to the gate bias. The g_m value increases with decrease in temperature due to a raise in I_D. The improvement in g_m is observed in the weak moderate inversion region and it falls at higher gate bias due to mobility reduction. The g_m reaches to highest peak value of 115 μS at temperature of 200 K and with increase in temperature, g_m decreases due to downfall in I_D. The improvement of g_m at lower temperatures is due to higher conduction band energy, which intern also enhances the gain of the device. The g_m shows marginal increment with effect to temperature for JL nanosheet FET.

The transconductance generation factor (TGF) is the property of a device that converts DC power into AC frequency. Higher the g_m of a device more will be the TGF, higher TGF for device indicates better analog performance. The mathematical expression for TGF can be given as TGF = g_m/I_D [22] and its variation with V_{GS} is depicted in Fig. 5(b). The TGF value is higher with a decrease in temperature and it decreases with raise in temperature. Since the reduction in I_D is more significant in the weak-moderate inversion region than increase in g_m with temperature, leading to an enhancement of g_m/I_D ratio. Moreover, there is a negligible impact of TGF, as anticipated at higher V_{GS} with temperature.

The output conductance (g_d) is an important figure of merit to calculate the intrinsic gain of a device. The output conductance is represented as $g_d = \partial I_D / \partial V_{DS}$.

The output conductance variation with respect to temperature is depicted in Fig. 6(a) and noticed that increase in temperature, g_d decreases and leads to a reduction of output resistance which ensures the better driving capability of the devices. Both V_{EA} and g_d have minimal impact with respect to temperature variation.

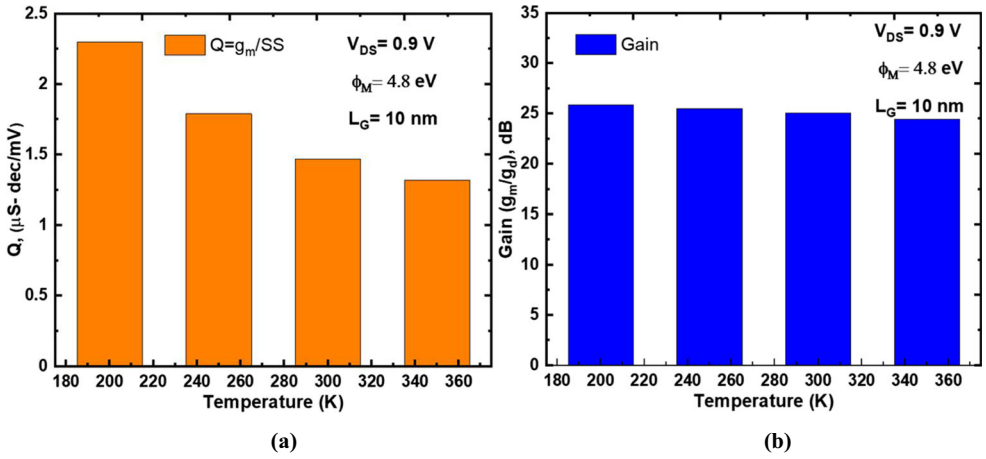
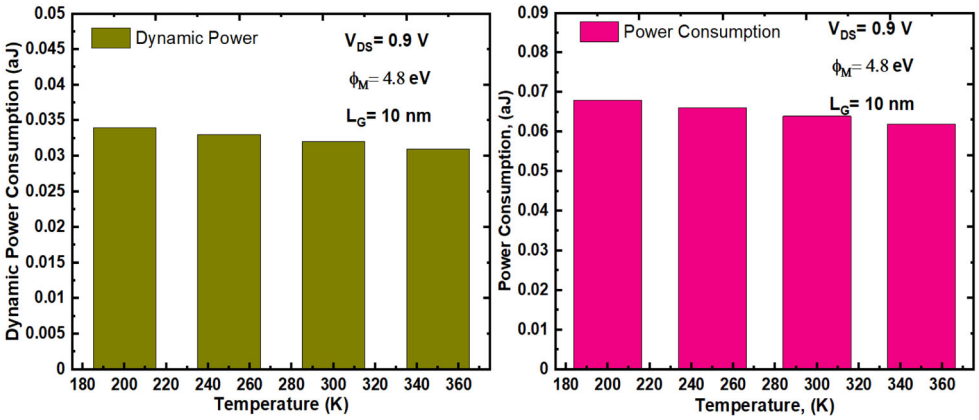


Fig. 8 The JL nanosheet FET characteristics (a) ON-OFF performance (Q) (b) Gain (A_V) with variation of temperature



(a) (b)

Fig. 9 The JL nanosheet FET characteristics (a) Dynamic power (DP) (b) Power consumption (PC) with variation of temperature

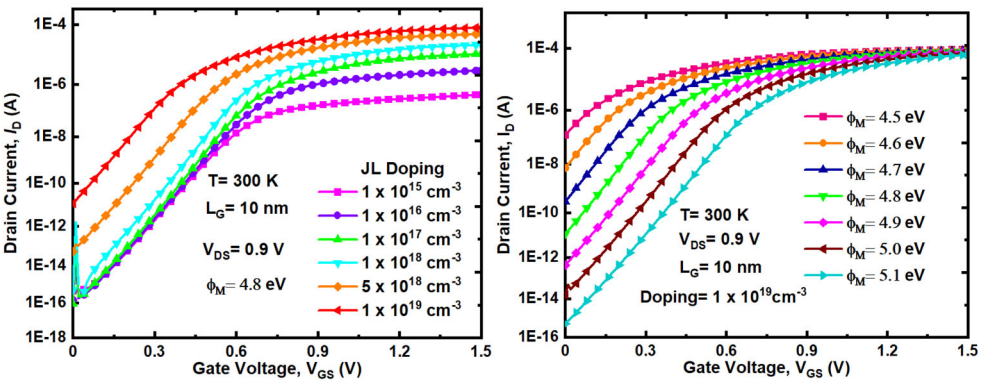
The early voltage V_{EA} ($\approx {}^{I_D}/_{g_d}$) is another important parameter for analog performance evaluation. Higher V_{EA} ensures higher output resistance [23]. From Fig. 6(b), at moderate gate bias V_{EA} is comparatively higher at T = 200 K. The device achieves V_{EA} of ~9 V for all temperatures and ensures good analog perspective. From the results it is noticed that JL nanosheet FET exhibits marginal increment in V_{EA} for temperature variations due to marginal variation in g_d.

The gate capacitance (C_{gg}) is the capacitance combination between source and drain terminals i.e., $C_{gg} = C_{gs} + C_{gd}$ [24]. The C_{gg} is an important metric to evaluate the parameters like cutoff frequency (f_T) and delay (τ). The response of C_{gg} for various temperature as a function of V_{GS} is depicted in Fig. 7(a). From the results, it is noticed that with temperature raise, the C_{gg} values increases due to reduction in energy bandgap lowers the energy barrier which simultaneously increases the charge carriers in the channel. Since the raise of charge carriers in the channel results in higher density of charge carriers under the gate region which increases the total gate capacitance [25].

The cutoff frequency ($f_T = g_m/2\pi\, C_{gg}$) is the frequency at which the current gain is unity and it indicates high frequency operation capability to obtain optimum gain [26]. From Fig. 7(b) the f_T value increases with decrease in temperature. The marginal increment of f_T as a function of temperature is due to marginal variation in g_m and C_{gg}. Table 3 lists the analog and RF FOMs of the device at nano-regime and noticed that the improved analog and RF characteristics with low temperatures are attributed to better carrier mobility and V_{th} due to high fermi potential and volume inversion respectively. Furthermore, reduced phonon scattering and enhanced velocity overshoot effect at a lower temperature is also responsible for better mobility and thus have better V_{th} and analog/RF performance [27].

Figure 8(a) depicts the ON-OFF performance metric 'Q' evaluates the device switching capacity and measures the qualitative behavior of the device. The expression for 'Q' is defined as Q = g_m/SS [28] and is detrimental in evaluation of device performance for mixed-signal applications. The 'Q' value is higher with lower temperature.

The gain (A_V) evaluates the overall performance of a device and the effect of temperature with respect to gain is depicted in Fig. 8(b). The expression for gain is given as $A_V = g_m/g_d$. The A_v is higher with 200 K and comparatively lower with 350 K due to g_m.



(a) (b)

Fig. 10 The JL nanosheet FET characteristics (a) Doping variation (b) Work Function (WF) variation

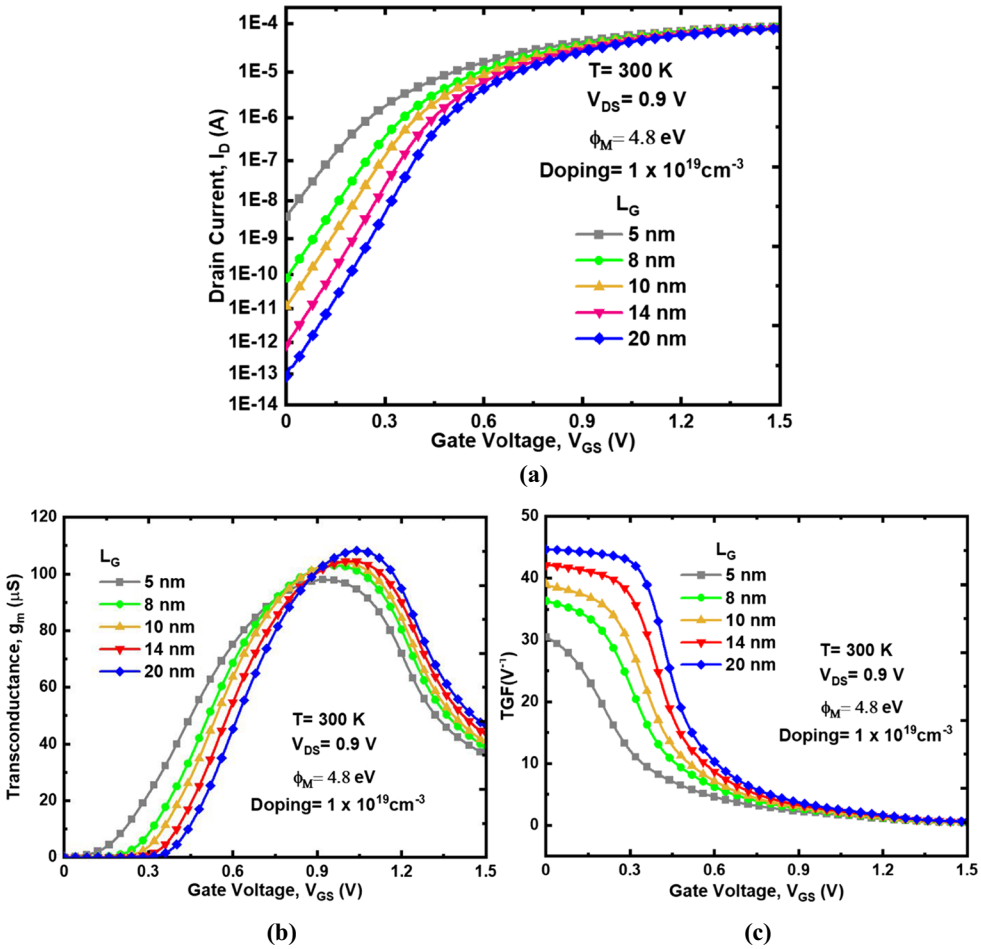


Fig. 11 The JL nanosheet FET characteristics (a) Gate length (L_G) scaling in log scale (b) Transconductance variation (g_m) (c) Transconductance generation factor (TGF) variation

The dynamic power and power consumption at V_{DD} = 0.9 V of 10 nm JL nanosheet FET is shown in Fig. 9(a) and (b). The expression for dynamic power (DP) is given as ($C_{OX}V_{DD}^2$) and the power consumption (PC) is given as $\left(\frac{1}{2}C_{OX}V_{DD}^2\right)$ per W at V_{DD} of 0.9 V [29] where C_{OX} is the intrinsic capacitance i.e., without any parasitic capacitances. Both DP and PC decrease with an increase in temperature at L_G = 10 nm. Both DP and PC are essential to estimate the device flexibility for low power and high-performance applications.

5 Process Parameter and Scaling Impact on Device Performance

5.1 Impact of Doping and Work Function

Figure 10(a) depicts the doping variations of JL nanosheet FET at fixed work function of 4.8 eV, V_{GS} = 1.5 V, and V_{DS} = 0.9 V. Lower doping concentration exhibits lower leakages but with a decrease of I_{ON}, higher doping shows moderate I_{OFF} but with enhanced I_{ON}.

Table 4 Performance comparison of JL nanosheet FET with different gate lengths at 300 K

Parameters at 300 K	L_G (nm)				
	5	8	10	14	20
V_{th} (V)	0.14	0.25	0.3	0.35	0.39
SS (mV/dec)	82.7	81.8	76.6	74.4	70.2
DIBL (mV/V)	162	104	69.76	50	46.5
I_{ON}/I_{OFF}	2.2×10^4	1×10^6	1.9×10^7	9.7×10^7	9.4×10^8
Transconductance, g_m (μS)	98	103	104.2	104.5	108.2
TGF (V^{-1})	30.49	36.38	39.11	42.08	44.62

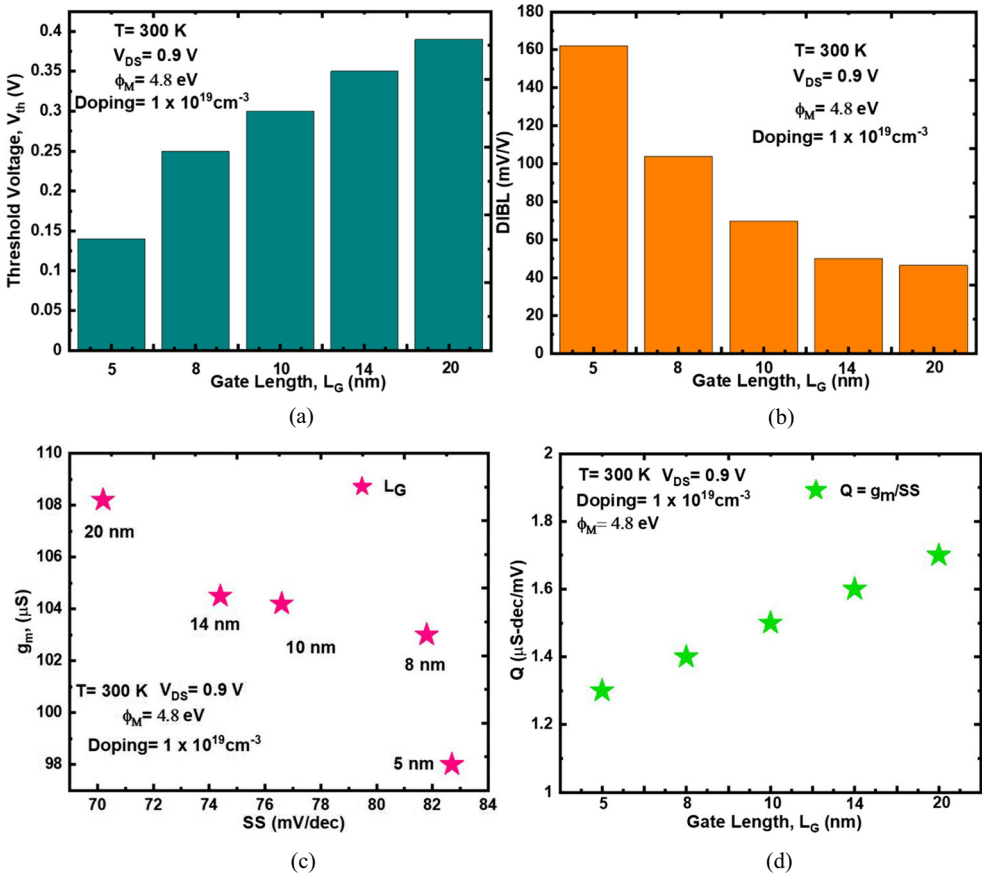


Fig. 12 The JL nanosheet FET characteristics (a) Threshold voltage (V_{th}) (b) DIBL (c) g_m and SS (d) ON-OFF performance metric (Q)

With an increase in doping both I_{ON} and I_{OFF} increases. At a doping concentration of 1×10^{19} cm^{-3} the device exhibits the highest I_{ON} and lower V_{th} and hence is suitable for low power digital and analog applications, whereas at lower doping the device achieves higher V_{th}, lower I_{OFF}, and I_{ON}. Furthermore, higher channel doping may result in decreased mobility due to higher coulomb scattering rates [30]. An increase in doping also leads to a reduction of bandgap and responsible for the impact ionization rate. Hence, the doping should be optimized for the improvement of device performance application perspective. The work function (WF) variation of JL nanosheet FET is depicted in Fig. 10(b) and noticed that increase in WF, the device leakage decreases and V_{th} increases. The WF range between 4.7 eV to 4.8 eV ensures moderate ON-OFF characteristics at 10 nm L_G. The increase in the WF leads to a significant decrement of I_{OFF} and marginal reduction of I_{ON}. Higher gate work function makes the device fully deplete quickly and ensures improved device performance in the OFF state. Also, an increase in WF reduces the gate to channel tunneling and significant reduction of the gate to source/drain extension tunneling in OFF state due to rise of electron tunneling barrier [31]. Although leakage factor decreases with higher WF the V_{th} also increases which leads to more time for the device to turn ON.

5.2 Impact of Gate Length Variation

The investigation of L_G variation of JL nanosheet FET from 20 nm down to 5 nm is carried for the evaluation of different short channel characteristics like V_{th}, DIBL, and SS. Figure 11(a), shows the transfer characteristics of JL nanosheet FET with various gate lengths (L_G). Scaling L_G increases leakage due to a shortage of gate control. Furthermore, high leakages are dominant in nano-regime and occupy a significant portion of power dissipation due to reduction of electrostatic integrity on the channel.

From Fig. 11(a) it is observed that with L_G scaling the device exhibits more I_{OFF} due to reduced gate control and direct band-to-band tunneling. However, the I_{OFF} does not fall below nA which is much lower than anticipated except at 5 nm L_G. The variation for g_m and TGF is depicted in Fig. 11(b) and (c). Both TGF and g_m shows significant decrement with L_G scaling owing to a reduction in I_D due to minimization of gate control over channel region and it is highest at 20 nm L_G. The DC characteristics like SS, DIBL, and analog and RF characteristics like g_m, TGF, Q are analyzed and presented in Table 4 for various L_G at 300 K. From Table 4 it is observed that the device exhibits decent performance in all L_G's with an I_{ON}/I_{OFF} ratio higher than 10^6 which is permissible for logic applications except at 5 nm L_G.

The short channel performance estimation of JL nanosheet FET is examined in Fig. 12(a) and (b) . The V_{th} decreases with a decrease in L_G due to the shortage of distance between source and drain and reduction of gate control. With increase in L_G the SCEs gets minimised and exhibits better performance due to better gate control and improved gate electrostatics. From the result analysis it is inferred that the device achieves better V_{th} with greater than 240 mV for all L_G's except at 5 nm. From Fig. 12(b), it is observed that DIBL increases with L_G scaling due to increased drain potential over the channel. The device exhibits moderate DIBL up to 10 nm L_G, but below 10 nm L_G the higher DIBL is noticed due to diminished gate control over the channel. The variation of g_m as a function of SS is depicted in Fig. 12(c) and found that, higher SS with scaling L_G is primarily attributed due to reduced gate control. Furthermore, the reduction of g_m with scaling L_G is due to reduced I_D. The variation of Q with L_G is depicted in Fig. 12(d) and noticed that Q value significantly decreases due to reduction of SS with L_G scaling. The device achieves maximum Q value of 1.7 μS-dec/mV at 20 nm L_G with 300 K.

6 Conclusion

The temperature simulation of analog and RF and power consumption analysis are performed on JL nanosheet FET. The results analysis reveals that analog and RF parameters like transconductance (g_m), TGF, gate capacitance (C_{gg}), and cut-off frequency (f_T) degrade with rise in temperature. The temperature dependence of analog and RF parameters of JL nanosheet FET is minimal. The dynamic power (DP) and power consumption (PC) decrease with rise in temperature. The switching performance metric (Q) and gain (A_v) decrease with increase in temperature. The JL nanosheet FET not only ensures optimum realization of digital logic but also analog and RF metrics with THz operational band frequency regime and ensures further scaling. The reduction of DP and PC ensures device driving capability for low power and high frequency applications at nano-regime. The scaling effect of nanosheet FET with various L_G's is performed and found that SCEs get minimized and exhibit better performance due to better gate control and improved gate electrostatics at higher L_G.

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Declarations

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